Abstract—Energy harvesting is the need of today’s world, especially for biomedical applications like Body sensor networks and remote area monitoring wireless sensor networks. The input energy level is very low in case of Energy harvesting. It is, therefore, important that the boost converter should be able to handle very low input voltages. This paper presents two different types of DC/DC converters based on inductive type converting stages in which one scheme uses CMOS technology while the other one is based exclusively on FinFET. With 120mV input, FinFET based converter can achieve 2.9V output. Moreover, it can also provide more than 1V output from an input of just 85mV. The values of inductors and the transistors area required with FinFET are much lower than MOSFET. Hence, the proposed FinFET based solution can be easily realized in IC form. All Boost converter schemes are investigated extensively using HSPICE simulations.

Index Terms—Charge pump, diode, energy harvesting, ring oscillator, switch.

I. INTRODUCTION

THIS decade is mainly dedicated to energy harvesting. Energy harvester extracts energy from the external environment [1]-[13]. The quality of energy which is extracted from the environment is very low i.e. low voltages, low currents, or both. It is also having fluctuations which have to be regulated first before giving it to the integrated circuit (IC). Therefore, it is unsuitable to supply standard ICs directly from an energy harvesting source. Usually ICs have charge pumps to carry out DC/DC conversion, and to increase voltage per stage. Several charge pump circuits have been reported in the recent literature [14]-[16].

Nowadays, energy harvesting circuits are getting more and more attention for powering ultra-low power circuits like wireless sensor networks (WSNs) for monitoring applications and implantable biomedical sensors, in which battery replacement is very difficult [17]-[20].

The bottleneck in WSNs is the power source. Conventional batteries limit the performance and lifetime of the system. It also increases the expenditure on maintenance, manufacturing cost and system volume. Therefore, it is very important to get rid of the battery in a WSN system to cut down its cost, system volume, and to increase its performance and lifetime. As WSNs require very low power, they can be effectively powered through energy harvesting [21]-[25].

As most of the consumer electronic products such as mobile phones, laptops, etc. still require more than 2.5 volts for their proper operation and therefore, voltage levels achieved in energy harvesting are very low compared to this level. Therefore, this paper presents two designs of DC/DC converters in different technologies namely CMOS and FinFET to achieve highest output voltage for a given input. This paper proposes for the first time that the use of FinFET instead of MOSFET not only improves the performance of the converter but also significantly reduces the required value of the inductance and the areas of transistors. The circuits proposed in this paper provide as high as 2.9V output from an input of 120mV. It is also shown that the circuit can give more than 1V with an input of less than 90 mV. This is important because a thermopile exposed to a small temperature gradient can deliver only 100mV [1].

This paper is organized into six sections. Section II presents state of the art step up converters for energy harvesting applications. In Section III, architecture of basic inductive type DC/DC converter is presented. Section IV contains proposed topologies of DC/DC converters. Section V presents simulation results of all circuits presented in Section IV followed by conclusion in Section VI.

II. STATE OF THE ART

Energy harvesting is one of the most important research domain in the present decade, as it provides clean energy extracted from the energy present in the environment. Clean energy is the need of today’s world because everyone is worried about global warming as a result of combustion of conventional energy sources. As IC technology provides low threshold devices, design of circuits which work at low input voltage is also possible. Since energy harvesting provides a low input voltage, so even today, designing of step up converter is very challenging. Few circuits are available in the literature, which can work at a voltage lower than 300mV.

The first charge pump circuit was presented by Dickson [26], which works on the principle of charge transfer by the diode connected MOS transistor. It provides the output voltage given by (1).

$$V_{out} = (N + 1) \times (V_{dd} - V_{TH})$$  \hfill (1)
where $V_{out}$ is the output voltage of the charge pump; $N$ is the number of stages present in the charge pump; $V_{dd}$ is the input voltage; $V_{TH}$ is the threshold voltage of the diode connected MOS. The threshold voltage drop is a big issue in these circuits. As the technology is scaled down, threshold voltage scaling is lagging behind supply voltage scaling. Therefore, the impact of the threshold voltage loss becomes much more pronounced in scaled technology.

Many architectures have been reported in the literature to enhance the performance of charge pumps and to reduce the threshold voltage loss [14]-[16]. But these architectures are not suitable for energy harvesting because of the low input voltages involved. Here also, the problem is with the threshold voltage loss of MOS used. As the number of stages has increased, the threshold voltage loss becomes even more pronounced. Capacitive DC/DC converters require very large number of stages to enhance low voltages.

Since the inductor can now be integrated in standard ICs [27], inductive up-converters have also come into picture. But inductive converters require ideal clock for their proper operation, because at very low input voltage, they provide very low energy efficiency. A circuit based on hybrid inductive and capacitive architecture has been proposed in [28]. It provides 1.2V from an input voltage of 200mV, but requires very large value inductors typically 33-47µH.

Charge pump based architecture is presented in [29] which can deliver 1V output from an input of 300mV. A DC/DC converter is reported in [30] which can work on 0.6V but it requires an external voltage of 2V. A circuit reported in [39] can work on 20mV input but requires an additional 0.65V for its operation. In [31], a circuit is presented which can work on 35mV input. It has an advantage that it does not require any external voltage but need a mechanical switch for its proper operation.

Recently, a DC/DC up-converter based on purely inductive components has been proposed in [32] which can enhance the input voltage of 120mV to 1.2V. It uses a large 27µH inductor in the first stage and 1.8µH inductor in the second stage.

Some of the DC/DC converters are also fabricated in fully depleted Silicon-On-Insulator (SOI) technology to reduce leakage currents and to enhance the performance of the system. Therefore, they can easily provide ultra-low voltage operation which is a must for an energy harvesting system [33]. These new technologies like SOI, FinFET, CNFET, etc. are a little bit expensive than standard CMOS process but they are highly promising.

## III. ARCHITECTURE OF INDUCTIVE TYPE DC/DC CONVERTER

Inductive type architectures of DC/DC converters can reduce the number of stages compared to the capacitive type. Therefore, this paper mainly focuses on inductive type architecture and presents modified version of the architecture given in [32]. It also demonstrates that the same architecture can give enhanced output voltage with much lower values of inductors using FinFET technology.

The elementary form of the circuit used in this paper is presented in [34]. It has one inductor, one diode, one switch, one load capacitor to store the output and one load resistance.

The boost converter is having two phases. In the first phase, the switch (S) is closed and the current flows from the voltage source ($V_s$) through the inductor and it stores energy. In this phase, the output stage is isolated because the diode (D) becomes reverse biased. In the second phase, when ‘S’ is open, the current in the inductor cannot die down instantaneously, a voltage spike larger than $V_s$ is generated at the end of the inductor which is connected to S and D, thereby making the diode forward biased. Therefore, the current is forced to flow through D and the load resistance (R) [35], [36].

Here D must be a Schottky diode as Schottky diode offers low forward voltage and high switching speed and can be a better alternative than a Si diode for an energy harvesting system. But the implementation of Schottky diode is not possible in a CMOS process, and hence a transistor based implementation of D is required [37].

Therefore, the circuit in [34] can be modified by replacing S and D by a MOS switch and a diode connected MOS as shown in Fig. 1. If components are considered to be ideal, then the output voltage is given by (2).

$$V_{out} = \frac{V_{dd}}{(1 - \alpha)}$$

where ‘$\alpha$’ is the duty cycle of the clock connected to the gate of the MOS switch. From (2), it is clear that by increasing $\alpha$, the output voltage can be increased. If M1 of Fig. 2 is always OFF, $\alpha = 0$ then $V_{out} = V_{dd}$. On the other hand, if M1 in Fig. 2 is always ON, $\alpha = 1$ then $V_{out} = \infty$. But in reality, infinite output cannot be achieved because of non-idealities of the components in the circuit. Therefore, in practical circuits, M1 is turned ON and OFF so that $\alpha$ is very large to achieve a higher output voltage than $V_{dd}$. Non-idealities like parasitic resistance and capacitance of MOS transistors affect the circuit performance in an adverse manner. The rise and fall time of the clock also determines the circuit performance. If the rise and fall time of the clock are short, the MOS switches abruptly and the output voltage is larger compared to the case when rise and fall time of the clock is long.

In Fig. 2, the circuit to boost the output voltage by cascading two stages of Fig. 1 is shown [32]. This circuit requires very high values of inductors and very large sized transistors as mentioned in [32].

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![Fig. 1. Transistor Implementation of Basic Step-up Converter](image-url)
To reduce transistor size and component values, this paper proposes a FinFET based circuit of Fig. 2. In Fig. 2, the clock generator is based on a ring oscillator which is formed by odd number of inverter stages. The clock drives a D flip-flop which is followed by a NAND gate to produce 75% duty cycle clock. The duty cycle of 75% is optimum because on increasing the duty cycle, the clock power consumption increases and the final output decreases.

IV. PROPOSED TOPOLOGIES

To improve the output voltage and to reduce values of inductors used compared to [32], this paper proposed a modified CMOS based topology and also includes a FinFET based implementation of the circuit proposed in [32]. In Fig. 1, there are two effects which are working simultaneously to alter the final output. These include loading effect and drop across the diode connected transistor. These two effects also change the final output of Fig. 2.

A. Two important Effects

1) Loading effect

In Fig. 1, the voltage at the terminal of the inductor which is connected to the diode connected transistor depends on the resistance of the diode connected transistor. The resistance of the diode connected transistor must be very large to reduce the loading effect. To increase the resistance of the diode connected transistor, its length must be increased as given in (3) and presented in [38].

\[
r = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}
\]

where \( \mu_n \) is the mobility of the transistor, \( C_{ox} \) is the capacitance per unit gate area, \( W \) and \( L \) are the channel width and channel length of the transistor, \( V_{GS} \) is the gate to source voltage and \( V_{TH} \) is the threshold voltage of the transistor.

2) Drop across Diode Connected Transistor

As the length of the transistor is increased, the voltage drop across the transistor also increases. Therefore, the length of the transistor cannot be increased beyond a certain optimum value. This work investigates the optimum value of \( W \) and \( L \) of transistors to achieve the maximum output by keeping a balance between these two effects.

B. Proposed CMOS Topology

The CMOS topology proposed in this paper is shown in Fig. 3. It uses a diode connected transistor with its body grounded. This is a modified configuration of Fig. 1. In Fig. 1, one of the MOS bulk terminals is connected to ground and the other terminal is connected to a voltage higher than ground. Therefore, in this circuit, isolation is very important between the two bulk terminals. For that purpose, a FinFET is more effective than a MOSFET.

In Fig. 7, the source of the diode connected transistor will float at voltages higher than bulk voltage i.e. ground. Because of this, the threshold voltage of diode connected transistor increases due to body effect which is expressed in (4) [38].

![Fig. 2. Circuit proposed in [32]](image)

![Fig. 3. Proposed CMOS Topology](image)
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\[ V_{TH} = V_{TH0} + \gamma (\sqrt{2\phi_F + V_{SB}}) - \sqrt{2\phi_F} \]  

(4)

where \( V_{TH0} \) is the threshold voltage at zero \( V_{SB} \), \( \gamma \) is the body effect coefficient, \( V_{SB} \) is the source-bulk potential difference, and \( \phi \) is the surface potential of the bulk.

This scheme also has the advantage that the bulk of its diode connected transistor is always connected to ground which is a much better configuration than having bulk connected to some potential.

The increase in threshold voltage due to body effect results in larger drop across the diode connected transistor but the resistance of the diode connected transistor also increases as per equation (3), which minimizes the loading effect. In this case, the loading effect dominates the drop across the diode connected transistor and hence the final output reaches up to a higher level of 1.55V which is much larger compared to 1.2V [32].

C. Proposed FinFET based DC/DC Converter

With the technology scaling, problems introduced in CMOS like short channel effects (SCEs), larger leakage, etc. are increasing. As the technology further scales down below 32nm, there will be no viable option of continuing with the conventional CMOS process because of many SCEs such as \( V_{TH} \) roll off and Drain Induced Barrier Lowering (DIBL), increasing leakage currents such as subthreshold S/D leakage, Gate Induced Drain Leakage (GIDL), hot carrier effects, etc. These effects are degrading the performance of the device. FinFET appears to be the device of choice below 20nm because of its reduced SCEs and relative ease of integration into existing CMOS process.

The term FinFET was given by the University of California, Berkeley researchers to describe a non-planar, double gate transistor built on an SOI substrate. The basic structure of the FinFET is shown in Fig. 4. The introduction of FinFET has opened up a new era in nanotechnology. Simulations show that FinFETs can easily be scaled down to 10nm.

A FinFET is a double gate FET in which the channel is a semiconducting Fin of width \( w \) and height \( h \), where \( w < h \). FinFET devices include a depleted body that provides a number of advantages over CMOS such as nearly ideal turn OFF in subthreshold, giving lower \( I_{OFF} \), allowing lower \( V_{TH} \), no loss in drain current from body effect, low voltage operation, higher current density, and reduced SCEs. FinFETs are easier to scale down to smaller physical dimensions and low operating voltage than CMOS.

Circuits based on FinFET can be implemented in two ways. The first is a shorted gate type FinFET in which both the gates are shorted together to minimize the power consumption. The other one is independent gate type FinFET in which back gate is used to control the threshold voltage of the transistor. This work uses only shorted gate type FinFETs.

In this proposal, the circuit proposed in [32] has been implemented by replacing conventional transistors with FinFETs. FinFETs provide better gate control because of which rate of change of inductor current is much larger than in a conventional transistor based DC/DC converter. Clock signals are nearly ideal as compared to clock signals generated by conventional transistors. Because of these ideal clock signals, transistor switches can be turned OFF abruptly as compared to [32]. Therefore, in this proposed scheme, voltage spikes at the inductor are much larger than [32], and hence final output also reaches to a much larger value of 2.9V.

The voltage across the inductor depends on the rate of change of current through the inductor and is given by (5).

\[ V_L = L \frac{di}{dt} \]  

(5)

where \( L \) is the inductance, and \( i \) is the current through the inductor. The final output depends on the voltage across the inductor. So, if the rate of change of current through the inductor is higher, the voltage across it also becomes larger and hence the final output increases. Therefore, in this proposal, the rate of change of current through the inductor is very high as compared to the scheme in [32], so, the final output becomes very large compared to [32]. Moreover, the values of inductors used are much lower compared to [32].

V. RESULTS

This section presents simulation results of all the proposed schemes. All circuits are simulated using HSPICE. All conventional transistors used in this work are simulated in 180nm process for the sake of fair comparison with [32] while all FinFETs are based on the 32nm process. In all circuits, the threshold voltage of each transistor must be very low for proper operation. All simulations are carried out using 120mV as input voltage. Some simulations are also performed at lower voltage for demonstrating the validity of the proposed schemes at lower voltages. All circuits have the same loading condition in the form of 10KΩ resistive and 30nF capacitive load. Inductor values for the CMOS proposed topology is 15µF for the first stage as it is driven from very low input voltage and 1µF for the second stage. These inductor values are low compared to [32]. Inductor values for FinFET is even lower i.e. 2µF for the first stage and 0.4µF for the second stage. These inductor values with FinFET will be further reduced for a 1V final output.

Fig. 5, shows the 75% duty cycle clock produced by conventional transistor based ring oscillator and Fig. 6, shows the 75% duty cycle clock produced by FinFET based ring oscillator. Clock frequency of the conventional transistor based ring oscillator is around 3MHz and the

Fig. 4. Basic Structure of FinFET
clock frequency in case of FinFET based ring oscillator is around 7 to 8MHz. The values of the inductors are highly dependent on the frequency of the clock. There is always an optimum value for the inductor at each stage to achieve highest final output. This paper also presented the optimum values of inductors in both the stages for each case.

It is easily evident from Fig. 5 and Fig. 6 that the 75% duty cycle clock produced from FinFET based ring oscillator has very low rise and fall time compared to conventional transistor based ring oscillator which is very important for achieving high voltage spikes of inductor voltage in Fig. 1, and hence the final output becomes larger.

Fig. 7 shows the voltage spikes at the inductor terminal of second stage in the first proposed topology of this paper. The maximum spike at the second stage shown in Fig. 7 is of 3.02V.

Fig. 8 shows the 75% duty cycle clock for the second stage in the CMOS proposed scheme of this paper shown in Fig. 3. It has better rise and fall time compared to the first stage. Clock has highest voltage equal to 298mV. Fig. 9 shows the output of the first stage. The output of the first stage achieves a maximum voltage of 301mV.

Fig. 10 shows the final output of the CMOS proposed scheme. The maximum voltage it achieves is 1.55V which is much larger than achieved in [32]. It is made possible by lowering the loading effect in the proposed scheme of [32]. This scheme also has the advantage that its diode connected transistors are always connected to ground which is a much better configuration than having bulk connected to potential other than ground.

The second scheme uses FinFETs in place of MOS transistors. Therefore, it has the advantage of higher mobility and better channel electrostatics because of which rate of change of inductor current in both stages is much larger than that of conventional DC/DC converter. The ring oscillator based on FinFETs produces nearly ideal clock signals as shown in Fig. 6. These two reasons are responsible for much larger final output than the conventional one.
Fig. 10. Final output of CMOS based scheme

Fig. 11 shows the inductor current in final stage of FinFET based DC/DC converter while Fig. 12 shows the inductor current in final stage of conventional one.

From Fig. 11 and Fig. 12, it can be easily seen that the rate of change of inductor current in case of FinFET based circuit is much larger than the conventional one. Therefore, the voltage spikes at the inductor terminal in FinFET based circuit are much larger compared to the conventional one according to (5) and hence, the final output is also larger.

Fig. 13 shows the voltage spikes at the inductor terminal of final stage of FinFET based DC/DC converter. The maximum voltage at the inductor terminal of final stage, shown in Fig. 13, is 3.85V.

Fig. 14 shows the 75% duty cycle clock for the second stage of a FinFET based DC/DC converter. The maximum value it achieves is 449mV, which is much larger than that of conventional circuit. When this clock is applied to the second stage, the final output becomes much larger than previous schemes. Fig. 15 and Fig. 16 show the output of first stage and final output of FinFET based circuit. At the first stage, the circuit provides a voltage level of 462mV and the final output of this circuit is 2.9V.

Fig. 11. Inductor current at final stage of FinFET based converter

Fig. 12. Inductor current at Final stage of conventional converter

Fig. 13. Voltage Spikes at inductor terminal of Final stage of FinFET based converter

Fig. 14. 75% duty cycle Clock for Final stage of FinFET based circuit

This paper also explores FinFET based DC/DC converter for much lower voltages. Fig. 18 shows the output of FinFET based DC/DC converter for 85mV input voltage. It achieves up to 1.11V from this very low input. Today many of the ICs can easily work on 0.9V. For those ICs, it is a good converter even if the harvested energy has very low voltage level.
TABLE I and TABLE II show the comparison of area of switching transistors and inductor values required in both stages of this work with the one proposed in [32] respectively. From the table, it is evident that the values of inductors as well as area of transistors in case of FinFET based converter proposed are much lower than the one presented in [32]. As the chip area is very costly and inductor consumes very large chip area, therefore, the main contribution of this work is to achieve higher output voltage with lower values of inductance and areas of transistors.

TABLE III shows the comparison of the performance of the presented circuits with other state-of-the-art circuits. Some of the presented circuits are implemented in 180nm CMOS process and others are implemented using 32nm FinFETs and can provide more than 1V from an input of less than 90mV. Two circuits also provide 2.9V from an input of 120mV. Also, one can see from the table that the converter in [39] requires an external voltage of 0.65V and three external components (an inductor and two capacitors); the converter in [31] does not use external voltage, but it requires a mechanical switch and an external inductor.

### TABLE I
**COMPARISON OF AREA OF SWITCHING TRANSISTORS OF [32] AND THIS WORK**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[32]</th>
<th>This Work with CMOS</th>
<th>This Work with FinFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>First Stage Switch Transistor Area (W×L)</td>
<td>9.5mm×1.5µm</td>
<td>10mm×1.5µm</td>
<td>300µm×32nm</td>
</tr>
<tr>
<td>Second Stage Switch Transistor Area (W×L)</td>
<td>4mm×240nm</td>
<td>10mm×240nm</td>
<td>300µm×32nm</td>
</tr>
</tbody>
</table>

### TABLE II
**COMPARISON OF INDUCTOR VALUES OF [32] AND THIS WORK**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[32]</th>
<th>This Work with CMOS</th>
<th>This Work with FinFET for 2.9V output</th>
<th>This Work with FinFET for 1V output</th>
</tr>
</thead>
<tbody>
<tr>
<td>First Stage Inductor (µH)</td>
<td>27</td>
<td>15</td>
<td>2</td>
<td>0.4</td>
</tr>
<tr>
<td>Second Stage Inductor (µH)</td>
<td>1.8</td>
<td>1</td>
<td>0.4</td>
<td>0.1</td>
</tr>
</tbody>
</table>

### TABLE III
**COMPARISON OF STATE-OF-THE-ART CIRCUITS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[28]</th>
<th>[29]</th>
<th>[30]</th>
<th>[39]</th>
<th>[31]</th>
<th>[32]</th>
<th>Proposed work with CMOS</th>
<th>Proposed work with FinFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.18µm</td>
<td>0.09µm</td>
<td>0.35µm</td>
<td>0.13µm</td>
<td>0.35µm</td>
<td>0.18µm</td>
<td>0.35µm</td>
<td>0.18µm</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>200mV</td>
<td>300mV</td>
<td>600mV</td>
<td>20mV</td>
<td>35mV</td>
<td>120mV</td>
<td>120mV</td>
<td>120mV</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>1.2V</td>
<td>1V</td>
<td>2V</td>
<td>1V</td>
<td>1.8V</td>
<td>1.2V</td>
<td>1.55V</td>
<td>2.9V</td>
</tr>
<tr>
<td>External Voltage</td>
<td>None</td>
<td>None</td>
<td>2V</td>
<td>0.65V</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>External Component</td>
<td>2 Inductors</td>
<td>None</td>
<td>2V Buffer Capacitor</td>
<td>1 Inductor 2 Capacitors</td>
<td>1 Inductor 1 Switch</td>
<td>2 Inductors</td>
<td>2 Inductors</td>
<td>2 Inductors</td>
</tr>
</tbody>
</table>

VI. CONCLUSION

In this paper, two types of DC/DC converters have been successfully designed and simulated. FinFET based converter can easily give more than 1V from an input voltage of 85mV and also provides 2.9V output from 120mV input, as most of the consumer electronics products like mobile phones are still working in 2.5V to 3.7V range.
Moreover, the values of inductors used and the transistor areas required with FinFET are much lower than existing converters and hence ideal for IC implementation. All proposed structures are suitable for energy harvesting applications.

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