Frequency Synthesizer Based on Pulse Swallowing

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Abstract - This article presents a design of new principle of the fractional frequency synthesizer based on pulse swallowing. This principle can be used for spurious phase modulation suppression when pulses are periodically removed from pulse train. The new synthesizer can be used also as a universal building block in phase locked loop frequency synthesizers. The mathematical analysis and simulations of the system are also presented.

Key-Words – comparator; fractional frequency synthesis; frequency divider; generator; lowpass filter; pulse removing; simulation

1 Introduction

The aim of frequency synthesis is to generate an arbitrary frequency from a given standard frequency or frequencies. Today, the frequency synthesizers are also an essential part of any modern transceiver system. They generate clock and oscillator signals needed for up and down conversion. The fine frequency resolution, low spurious signals, accuracy and stability are most important for these devices. The two most popular structures of radio-frequency synthesizers are the fractional-*N* frequency synthesizer and the integer-*N* frequency synthesizer.

Although fractional-*N* synthesizer owns a great performance in frequency resolution and settling time, its division number depends on accumulator carrier which may lead to spur noise closing to the wanted signal due to the periodically produced characteristic. Consequently, compared with the integer-*N* frequency synthesizer, a more complicated modulator is needed to alleviate the influence of noise for fractional - *N* synthesizer [1 - 7].

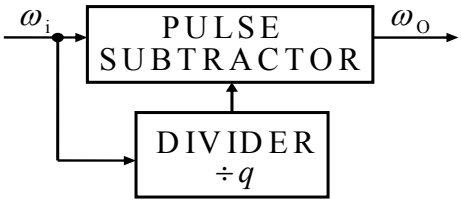

Fig. 1. The block diagram of pulse swallowing. Each *q*-th pulse is removed.

One of the simplest solutions for generating desired frequency from reference frequency is pulse-swallowing integer-*N* frequency synthesizer (see Fig. 1). Suppose a pulse train in which pulses are placed in regular distances T_i (frequency ω_i) on time axis. If we remove each *q* pulse, then one period is missing and phase undergoes a step change equal 2π, that is,

$$\varphi(t) = \omega_i t - 2\pi V(t_k) \tag{1}$$

where $V(t_k)$ is the step function occurring at instances

$$t_k = kqT_i \tag{2}$$

where *k*=…-1, 0, 1, 2, …, and the average frequency ω_O may be expressed as

$$\omega_O = \omega_i \frac{q-1}{q} \tag{3}$$

The simulation of input pulses, pulse omission of each 8th pulse (*q*=8), equally distributed output pulses and spurious phase modulation is shown in Fig. 2. [8, 9, 10].

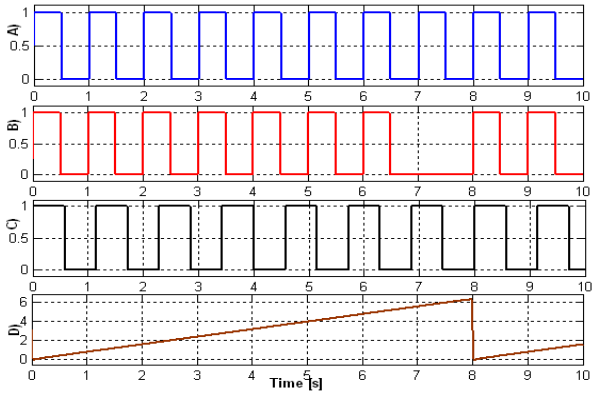

Fig. 2. Pulse swallowing principle. A) input pulses, B) pulse omission of each 8th pulse (*q*=8), C) equally distributed output pulses and D) spurious phase modulation.

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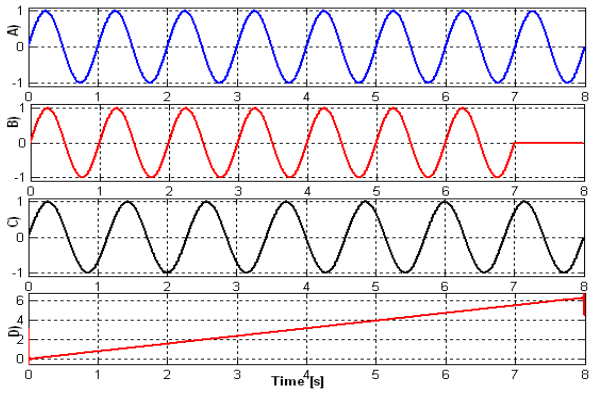

Fig. 3. The time diagram of sine wave signals for calculation of frequency spectrum. A) input, f_i=1 Hz B) one period omission of each 8th pulse (q=8), C) desired sine wave signal f_O=0.875 Hz according (3) and D) spurious phase modulation.

For frequency spectrum calculation, the sine wave signals were used (see Fig. 3). The frequency spectrum of signal with period omission (q=8) and continuous sine wave signal with desired frequency f_O=0.875 Hz is shown in Fig. 4.

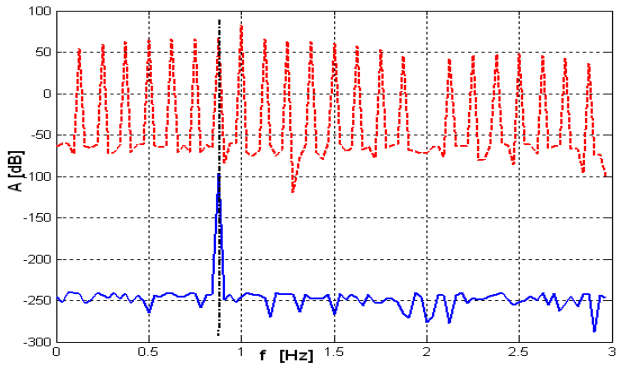

Fig. 4. The frequency spectrum of period swallowing (each 8-th period), top and spectrum of continuous sine wave signal f_O=0.875 Hz, shifted bottom.

The frequency spectrum has bad spectral purity and therefore new frequency synthesizer was developed.

2 Frequency synthesizer principle

The block diagram of fractional frequency synthesizer is presented in Fig. 5. Suppose, that synthesizer is controlled by microcontroller by Ctr1 (control of pulse swallowing) and Ctr2, calculated average value of signal from generator G. Other parts are SW - switch, V_R - reference voltage, Ctr2 - average value of signal with periodic pulse omission, I - integrator, A - amplifier, LP - low-pass filter, C - comparator, f/2 - frequency divider, f_O - output frequency.

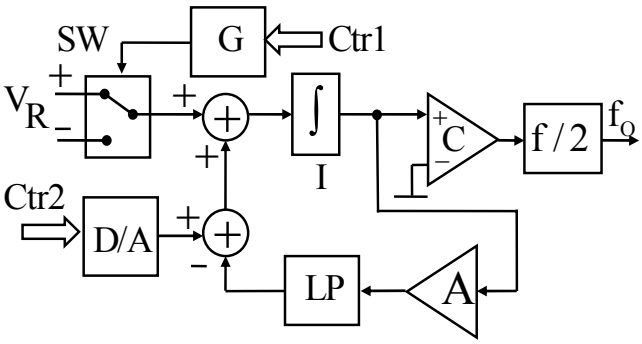

Fig. 5. The block diagram of fractional frequency synthesizer. Ctr1 - pulse swallowing control, G - generator with pulse swallowing possibility, SW - switch, Vr - reference voltage, Ctr2 - average value of signal with periodic pulse omission, I - integrator, A - amplifier, LP - low-pass filter, C - comparator, f/2 - frequency divider, f_O - output frequency.

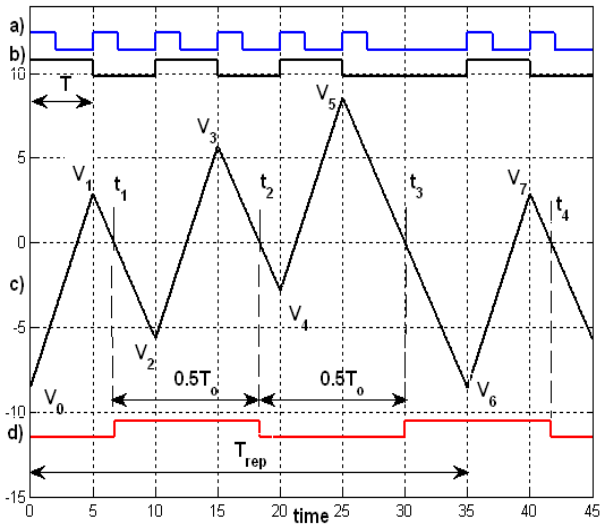

Fig. 6. The time diagram of signals in fractional frequency synthesizer based on pulse swallowing and charge balancing. a) Generator clock signal with pulse omission possibility, period T, b) signal a) divided by 2, c) integrator output, d) output signal f_O. T_{rep} - repeated period, output period T_O. $V_0 \div V_7$ voltage on integrator output, $t_1 \div t_4$ times of integrator voltage leading edge zero crossing.

The synthesizer output signal is derived according example presented in Fig. 6. for $V_R = \pm 2$ V and initial integrator voltage V_0. Suppose, that we have input signal (with period $T = 5$) with omission every 7th pulse (pulse is deleted in time $t = 30$, signal a) in Fig. 6). The number of pulses without omission pulses is N_P and number of deleted pulses is D_P. The inverted mean voltage V_M on the output of switch SW (for $V_R = \pm 2$ V) is given by eq. (4), for $N_P = 7$ and $D_P = 1$ (for signal b), Fig. 6)

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$$V_M = V_R \frac{D_P T}{N_P T} = V_R \frac{D_P}{N_P} = V_R \frac{1}{7} = \frac{V_R}{7} = \frac{2}{7} = 0.2857 \quad (4)$$

The voltage V_M is calculated by means of D/A converter and its digital value is Ctr2. The mean voltage V_M on D/A output is added to voltage on output of the switch SW. Therefore for voltage $+V_R$ the voltage slope on integrator output is

$$k_+ = V_R + V_M \quad (5)$$

and for voltage $-V_R$ the voltage slope is

$$k_- = -V_R + V_M \quad (6)$$

Integrator output voltages $V_1 \div V_6$ are given by

$$\left.\begin{aligned}
V_1 &= V_0 + k_+ T = V_0 + (V_R + V_M)T \\
V_2 &= V_1 + k_- T = V_1 + (-V_R + V_M)T = V_0 + 2V_M T \\
V_3 &= V_2 + (V_R + V_M)T = V_0 + 3V_M T + V_R T \\
V_4 &= V_3 + (-V_R + V_M)T = V_0 + 4V_M T \\
V_5 &= V_4 + (V_R + V_M)T = V_0 + 5V_M T + V_R T \\
V_6 &= V_5 + (-V_R + V_M)2T \\
&= V_0 + (5V_M + V_R - 2V_R + 2V_M)T \\
&= V_0 + (7V_M - V_R)T \\
&= V_0 + (7V_M - V_R)T = V_0 + (7\frac{U_R}{7} - V_R)T = V_0
\end{aligned}\right\} \quad (7)$$

From the eq. (7) can be calculated that $V_6 = V_0$, $V_7 = V_1$ …, all is repeated periodically. The maximal voltage on integrator output is

$$\begin{aligned}\Delta V_{MAX} &= V_5 - V_6 = V_5 - V_0 = V_0 + (5V_M + V_R)T - V_0 \\ &= (5V_M + V_R)T\end{aligned} \quad (8)$$

and for $V_M = V_R/7$ according (4).

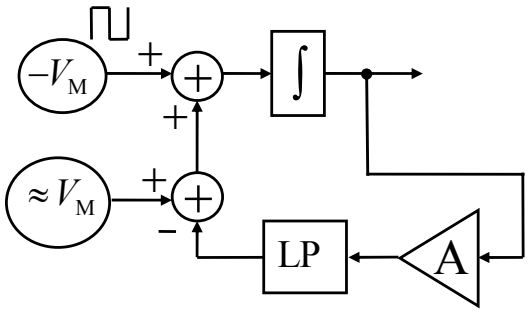

Fig. 7. The equivalent feedback loop of synthesizer. $-V_M$ mean value of pulsed voltage on switch output, $\approx V_M$ dc voltage from D/A converter, LP low pass filter, A amplifier.

The feedback loop consists of amplifier with gain A and low-pass filter LP. The loop holds zero average value on integrator output, see equivalent circuit in Fig. 7 (feedback loop balance some inaccuracy and differences between $-V_M$ and $\approx V_M$). Time t_1 (Fig. 6) can be determined when cross zero voltage of line from V_1 to V_2, where V_1 is

$$\begin{aligned}V_1 &= V_0 + k_+ T = V_0 + (V_R + V_M)T \\ &= \left(-\frac{6}{7}V_R + V_R + \frac{V_R}{7}\right)T = \frac{2}{7}V_R T\end{aligned} \quad (9)$$

and after some manipulation

$$t_1 = T + \frac{T}{3} \quad (10)$$

and similarly t_2 and t_3 (Fig. 6)

$$t_2 = 3T + \frac{2T}{3} \quad (11)$$

$$t_3 = 5T + T = 6T \quad (12)$$

and first half output period $0.5T_O$ is

$$0.5T_O = t_2 - t_1 = 3T + \frac{2T}{3} - \left(T + \frac{T}{3}\right) = \frac{7}{3}T \quad (13)$$

and second half output period $0.5T_O$ is

$$0.5T_O = t_3 - t_2 = 6T - \left(3T + \frac{2T}{3}\right) = \frac{7}{3}T \quad (14)$$

From eq. (13) and (14), frequency synthesizer output frequency is derived

$$\begin{aligned}f_O &= \frac{1}{T_O} = \frac{1}{0.5T_O + 0.5T_O} = \frac{1}{\left(\frac{7}{3} + \frac{7}{3}\right)T} = \frac{3}{14T} \\ &= \frac{3}{14} f_{CLK} = \frac{3}{14}\left(\frac{1}{5}\right) = 0.042857\end{aligned} \quad (15)$$

where is f_{CLK} generator frequency ($f_{CLK} = 1/T = 0.2$ in this example). From previous results the output frequency f_O can be derived

$$f_O = \frac{1}{4}\left(\frac{N_P - D_P}{N_P}\right)\frac{1}{T} = \frac{1}{4}\left(\frac{N_P - D_P}{N_P}\right) f_{CLK} \quad (16)$$

and for $N_P = 7$, $D_P = 1$ and f_{CLK}=0.2 Hz, the f_O is

$$f_O = (1/4)*[(7-1)/7]*0.2 = 0.042857 \quad [\text{Hz}] \quad (17)$$

The frequency spectrum of square wave signal simulation according previous equations is presented in Fig. 8 (for $N_P = 7$, $D_P = 1$ and f_{CLK}=0.2 Hz, amplifier gain A = 0.0045 and

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low-pass filter is 6th order Butterworth filter with corner frequency 0.04 [rad]), [11 - 15].

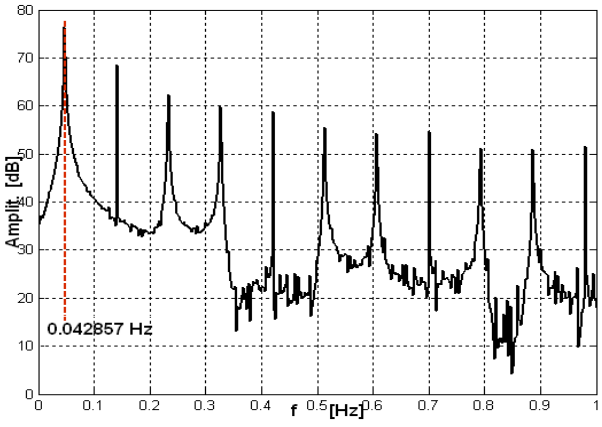

Fig. 8. The frequency spectrum of square-wave output signal of the synthesizer for $N_P = 7$, $D_P = 1$ and f_{CLK}=0.2 Hz The amplifier gain is A=0.0045 and low-pass filter is 6th order Butterworth filter with corner frequency 0.04 [rad].

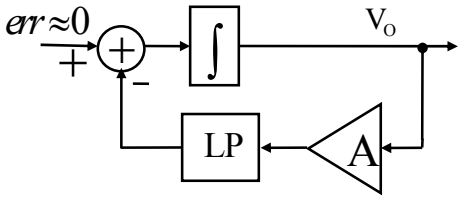

Fig. 9. The equivalent feedback loop for synthesizer stability evaluation.

3 Stability of the loop and filters

Because the synthesizer contain the feedback loop, it is important to solve stability. The simplified feedback loop is shown in Fig. 9. Input signal (err ≈ 0) is difference of the mean value $-V_M$ (switch output) and $\approx V_M$ (D/A converter output). The closed feedback loop can be described by transfer function

$$\frac{V_O}{err} = \frac{\frac{1}{s}}{1+\frac{1}{s}AF_{LP}(s)} = \frac{1}{s+A\frac{N(s)}{D(s)}} = \frac{D(s)}{sD(s)+AN(s)} \qquad (18)$$

where $N(s)$ and $D(s)$ are numerator and denominator of low-pass filter transfer function respectively and A is value of amplifier gain. For system stability the real parts of the roots of closed loop denominator must be negative. The stability and behavior of the closed loop is controlled by gain A of the amplifier. The step response of closed loop for amplifier gain A and several types of 6th order low-pass filters (Bessel, Butterworth, Chebyshev and elliptic) with corner frequency 0.04 [rad] are presented in Fig. 10-13 and bode diagram for closed loop with elliptic filter in Fig. 14.

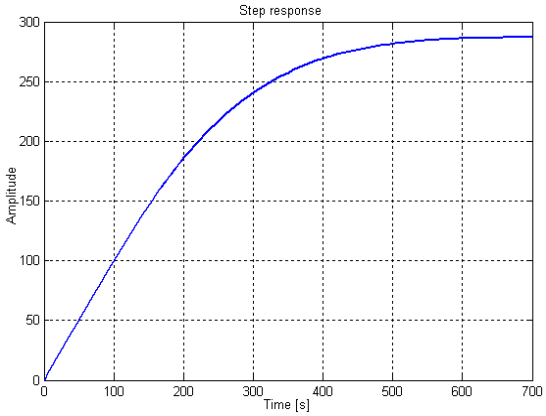

Fig. 10. Closed loop step response for Bessel 6th order analog filter with corner frequency 0.04 [rad], gain A= 0.0035

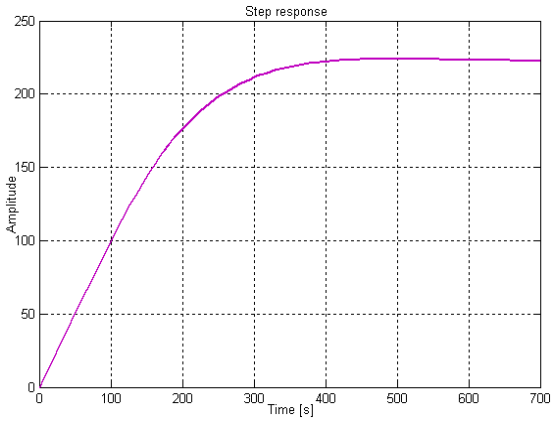

Fig. 11. Closed loop step response for Butterworth 6th order analog filter with corner frequency 0.04 [rad], gain A= 0.0045.

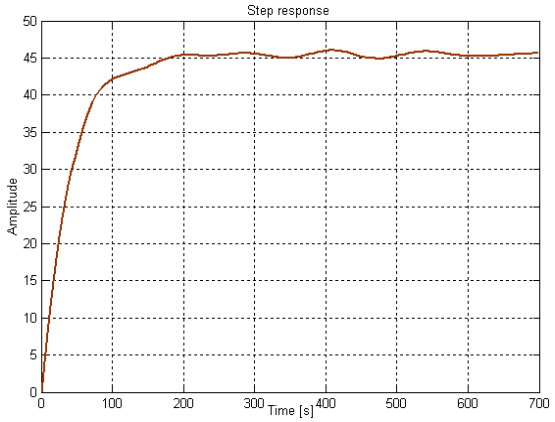

Fig. 12. Closed loop step response for Chebyshev type2, 6th order analog filter with corner frequency 0.04 [rad], gain A= 0.022.

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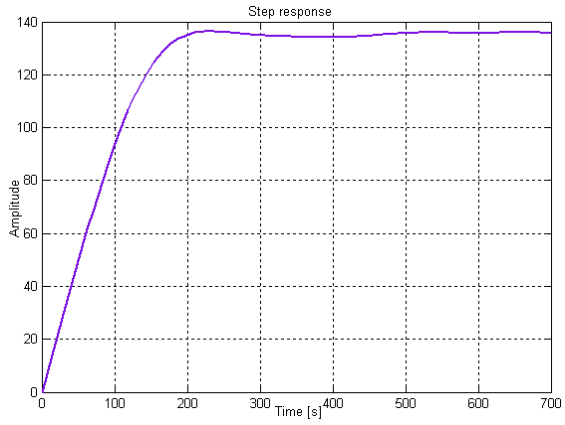

Fig. 13. Closed loop step response for elliptic 6th order analog filter with corner frequency 0.04 [rad], gain A= 0.0078

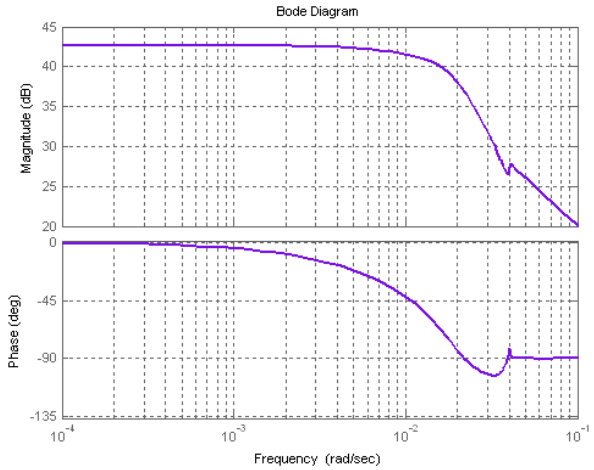

Fig. 14. The Bode diagram of closed loop for elliptic 6th order analog filter with corner frequency 0.04 [rad], gain A= 0.0078

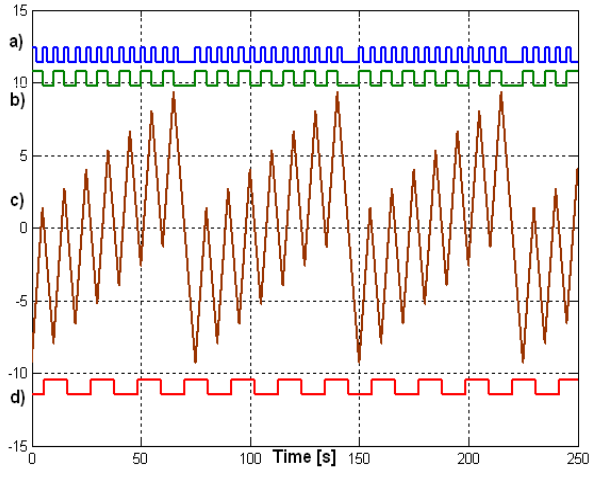

Fig. 15. The time diagram of signals in fractional frequency synthesizer based on pulse swallowing and charge balancing. a) Generator clock signal with pulse omission, b) signal a) divided by 2, c) integrator output, d) output signal f_O = 0.04666 [Hz], for N_P = 15, D_P = 1 and f_{CLK}=0.2 Hz.

The state space description of closed loop system is described as

$$\dot{x} = Ax + Bu; \quad y = Cx + D \tag{19}$$

where numerical values of matrices A, B, C, D (for 7th order system according Fig. 9 with 6th order elliptic filter) are

$$A = 10^{-2}\begin{bmatrix} -4.56 & -3.27 & -0.85 & -0.5 & -0.33 & -0.32 & -0.6 \\ 12.5 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 12.5 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 6.25 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 3.125 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1.56 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0.4 & 0 \end{bmatrix}$$

$$B = [2\ 0\ 0\ 0\ 0\ 0\ 0]^T \tag{20}$$

$$C = 10^{-2}[50\ 18\ 13\ 6.6\ 8\ 9.3\ 41];\ D = [0]$$

The zero-pole-gain of closed loop system (F_{CL}) described by eq. (19) and (20) is

$$F_{CL}(s) = k_{CL}\frac{(s-z_1)(s-z_2)\cdots(s-z_6)}{(s-p_1)(s-p_2)\cdots(s-p_7)} \tag{21}$$

where k_{CL}=1 and zero-pole values are:

$$\left.\begin{aligned} z_{1,2} &= -0.0008 \pm 0.0402i \\ z_{3,4} &= -0.0049 \pm 0.0370i \\ z_{5,6} &= -0.0170 \pm 0.0197i \end{aligned}\right\} zeros$$

$$\left.\begin{aligned} p_{1,2} &= -0.0008 \pm 0.0403i \\ p_{3,4} &= -0.0059 \pm 0.0366i \\ p_{5,6} &= -0.0095 \pm 0.0171i \\ p_7 &= -0.0131 \end{aligned}\right\} poles \tag{22}$$

4 Frequency synthesizer simulations

The simulation result was derived for N_P = 15, D_P = 1 and f_{CLK}=0.2 Hz, amplifier gain A=0.0078 and 6th order elliptic low-pass filter with corner frequency 0.04 [rad] (see closed loop response, Fig. 13). The output frequency, according (16) is

$$\begin{aligned} f_O &= \frac{1}{4}\left(\frac{N_P - D_P}{N_P}\right) f_{CLK} \\ &= \frac{1}{4}\left(\frac{15-1}{15}\right) 0.2 = 0.04666 \end{aligned} \tag{23}$$

Signal derived by simulation are displayed in Fig. 15. This figure shows input signal a), b) input

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signal divided by 2 (on rising edge), c) integrator output, d) output signal. All signals are displayed in steady state.

The relative output frequency f_O for f_{CLK}=4, D_P=1 and D_P=2 and N_P=⟨5÷30⟩ is presented in Fig. 16.

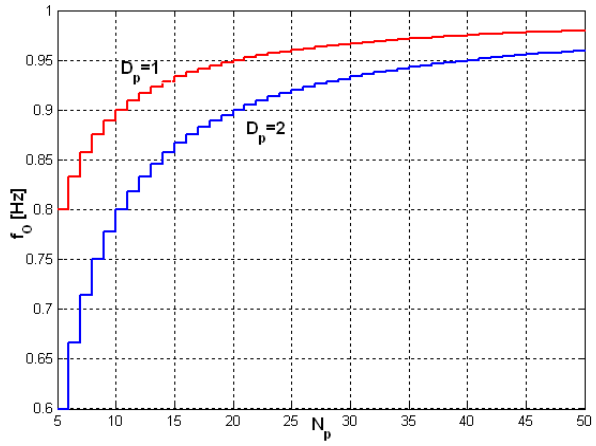

Fig. 15. Output frequency as function of N_P for f_{CLK}=4, D_P=1 and D_P=2.

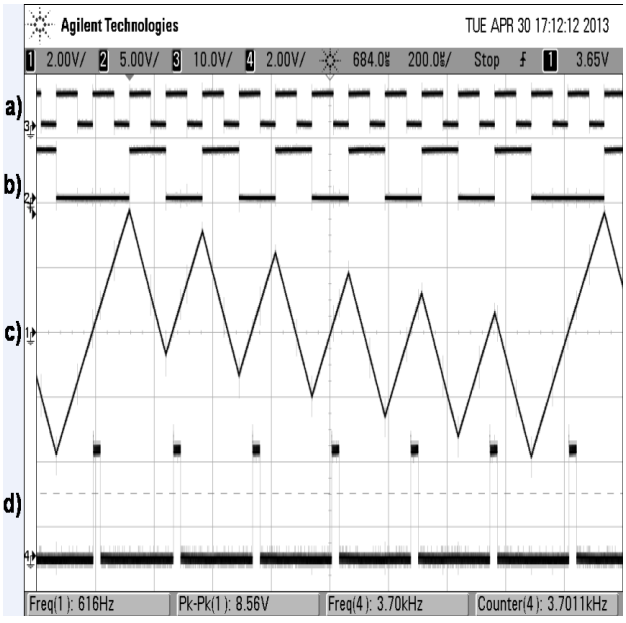

Fig. 16. The time diagram of signals measured in frequency synthesizer. a) Input clock signal, b) signal with pulse omission (input clock frequency with pulse omission divided by 2), c) integrator output, d) output signal f_O = 3.7011 kHz, for N_P = 13, D_P = 1 and f_{CLK}=8.0191 kHz.

5 Measurement results

The simplified (low frequency) version of pulse swallowing frequency synthesizer was constructed and measured. The result of measuring confirmed theory and simulations. The first example is shown in Fig. 16. It is important to note that inverting integrator was used and output signal frequency was not divided by 2, therefore equation for output frequency is given by

$$f_O = \frac{1}{2}\left(\frac{N_P - D_P}{N_P}\right) f_{CLK} \qquad (24)$$

therefore for N_P = 13, D_P = 1 and f_{CLK}=8.0191 kHz, the frequency of output pulses is f_O = 3.7011 kHz.

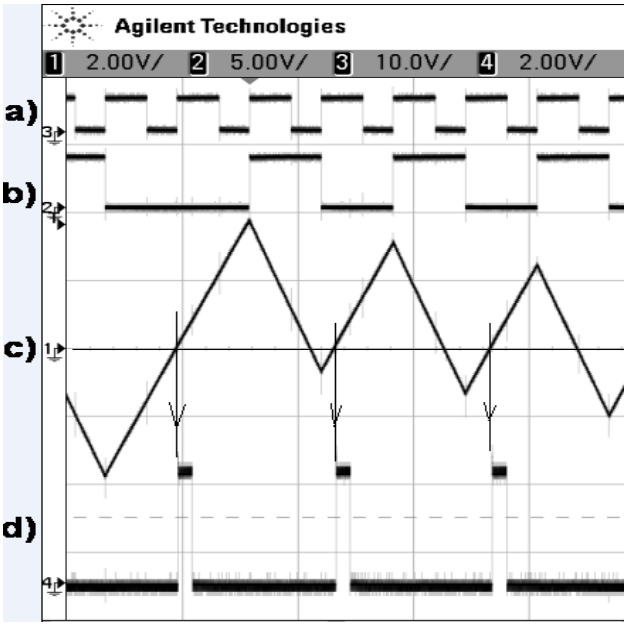

Fig. 17. Zoom of Fig. 16. Principle of output signal generation – pulses on rising edge of signal c), crossing the zero level.

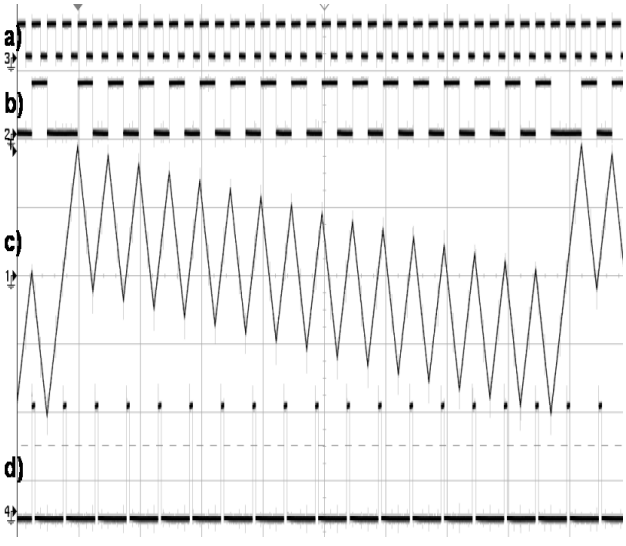

Fig. 18. The time diagram of signals measured in frequency synthesizer. a) Input clock signal, b) signal with pulse omission (input clock frequency with pulse omission divided by 2), c) integrator output, d) output signal f_O = 3.888 kHz, for N_P = 33, D_P = 1 and f_{CLK}=8.0191 kHz.

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The output signal (see Fig. 16 d) are generated when rising edge of integrator signal cross the zero level, all is displayed in Fig. 17.

The example for values N_P = 33, D_P = 1 and f_{CLK}=8.0191 kHz is shown in Fig. 18. Frequency of output signal, according eq. (24) is f_O = 3.888 kHz.

6 Conclusions

A detailed look at the concept of new fractional frequency synthesizer based on pulse omission technique and charge balancing has been presented in this paper. The new synthesizer can be also used as a universal building block in different types of frequency synthesizers (e.g. phase locked loops). The main advantage of this fractional synthesizer is simple generation of fractional frequency which is close to reference frequency. Analysis and simulation results of the new fractional synthesizer were also shown. The theory and simulation were confirmed by construction of synthesizer. The real signals were measured on this synthesizer.

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