Voltage control oscillator design for software-define radio in wideband

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Abstract: In recent years, needs of mobile communication systems that covered global areas have increased very much. To achieve this application the software-defined radio (SDR) is a good method. One of important requirements of SDR is RF hardware that can work in wide band. One of necessary parts of RF hardware is voltage controlled oscillator that is must designed in wide band range. In this paper concept of VCO design is researched and after that simulation of that design is investigated. The phase noise of this design is so good too.

Key-Words: Software-defined Radio, Voltage Controlled Oscillator, Phase Noise

1 Introduction

The use of the mobile telephony is frequently coverage throughout the world and ease of interfacing with different systems and standards. To direct such changes, mobile systems must have changeable hardware and reprogrammable software. Such radios, known as Software Defined Radios (SDR) can be placement effective using software radio structures in that the radio change itself based on the system it will be interfacing with and the uses of it will be aiding [1, 2]. Implementation of the SDR would want either the replace of RF into baseband at the antenna or the design of a completely inflection radio frequency (RF) front-end for work in a wide range of frequencies [4]. The intelligent antenna system in SDR conflict the multipath effects and co-channel overlap [3]. Dissertation the signal with an analog to digital converter (ADC) in the IF range specify the last stage in the conventional model in which obstacle like carrier offset and imaging are encountered. One of the problems in SDR design is: for the reconfigurable RF front end, the structure and circuits should be designed for a far range of requirements in carrier frequency, channel bandwidth and noise yield. Meeting the yield parameters over a far range of frequency is not evident. The sequent work involved theory, design, simulation, fabrication and test & optimization of VCO for wideband LO in SDR.

2 VCO Design theories

however several researchers before have published oscillator structures based on some form of small signal analysis, these methods require a blend of theoretical and experimental calculations and do not always lend themselves to the solicit result as setting of the ultimate device is unavoidable . Our approach includes simulation resulting in substantial savings in design time as well as setting time, laminated results very near to the favourable yield. The transistor selection is of main importance. For a frequency range of a few hundred MHz to several thousand MHz, VCOs are generally built based on BJTs. Because of their natural low noise. Equivalent to popular belief, f max is not the most certain quantity in the selection of the device. Here, f max is described as the frequency at that the unilateral gain decreases to unity, and the device ceases to oscillate. With a high f max the device is sensitive to oscillations outside the desired frequency range, and external pairing between the device leads may levitate. Needless to say, if cost is to be kept low, devices with very high f max are costly. f max should definitely be within the desired range of function, but power dissipation is also an important criteria in the selection of the device. Power waste is important, as VCO active devices work at high power levels. Also, attention should be taken to control the oscillation totally through the external circuitry.
with no possible spurious oscillations inside the device. A primitive simulation/construction of a non-oscillating circuit is necessary in order to prove that the device is free of unwanted counterfeit oscillations. The line of BJTs selected offers an ideal choice as they can typically be used up to 8 GHz and lend themselves to all forms of external positive feedback, while producing an average negative resistance of 50 to 400 ohms. Most of the accessible literature on oscillators describes the operation of oscillators using small signal S parameters. The main reason for this is that small signal S parameters are readily measurable and all transistor manufacturers supply them for their devices. The small signal design technique offers worth insight into the conditions that govern oscillator starting, while giving a rough prediction of the possible frequency range of work.

The drawback, is that only for the first few cycles after the device is turned on those estimates are credible. A complete derivation of the feedback network of the device, with an application of the Barkhausen criteria is a good way to describe the oscillation process. According to the Barkhausen criteria the product of the feedback path gain and feedback path gain is 1, but also the output wave should be added to the input while the phase shift is zero by the feedback loop, it means that the feedback has to be zero. The continuous balancing of these two values is the process that makes the device oscillates during that condition. While the amplitude of device oscillation increases, the gain is decreased in order to assure the Barkhausen criteria.

It is very complex to derive the equations of the feedback and forward loop gains of the device and much care has to be taken in two loops identification. A very good explanation for that mechanism is introduced by Rohde[5]. We will use a more simple method for describing the oscillation criteria in addition to the last criteria. This process is not pleasant because of its view about the operation of the device, its importance is due to ease of application. The increment in signal amplitude while building up from the internal noise level is explained by the considerations which are taken for the input resistance of the device. It can be noted from fig.1 that because the resistance of the active combined device is bigger than the load resistance this happens:

\[ | -R_{osc} | > R_r \text{ and } X_{osc} = -X_r \]  

(1)

The DC operating point of the device moves from one point to another point continuously while the amplitude of the oscillation increases, hence the transconductance (gm) and the input and output impedance changes. According to this situation a shift in the frequency is caused, this could also lead in a change in the harmonics of the output or in output power levels. The amplitude increment will stop as the following condition happens:

\[ | -R_{osc} | = R_r \text{ and } X_{osc} = -X_r \]

Alternatively when \( \Gamma_r, T_{osc} = 1 \)  

(2)

This condition denotes that the respective impedance and the active device have to be equal.

\( \Gamma_r \) and\( \Gamma_{osc} \) are the reflection coefficients which respectively are produced by \( R_r + jX_r \) and \( R_{osc} + jX_{osc} \). The device reaches to saturation conditions as steady state happens. A very important resistance is \( R_{osc} \), which the nonlinear I-V relationships of the transistor describe it well. It can be seen that the value of \( R_{osc} \) varies non-linearly around a I-V operation point because of a non-linear current source if an accurate look is taken at the common base transistor. The total current can be considered as the sum of all individual currents at all harmonic frequencies. It means that:

![Typical oscillator network as used for graphical/computer analysis](image)
When the oscillation is stopped, $I_{dc}$ is the DC current of the device. As the oscillation starts, $I_1, I_2, I_3$ can be stated as the first, second and third harmonics. The total transconductance of the device can be expressed as follows:

$$I_{total} = I_{dc} + I_1 + I_2 + I_3 + \ldots = \sum_{n=0}^{\infty} I_n$$

(3)

The transconductance can be expressed as:

$$G_{m_{total}} = g_{m0} + g_{m1} + g_{m2} + g_{m3} + \ldots = \sum_{n=0}^{\infty} g_{mn}$$

(4)

gm0 Denotes the value of transconductance at DC point and gm1, gm2 are the values at the first and second harmonics. You have to know that gm1 is equal to 0.7gm0 and is the most important part in equation 4. For keeping the oscillation criteria gm1 has to decrease while the oscillation amplitude increases and Gm_{total} is equal to a constant value for a DC input current. The reason of Rosc being a more positive value when the system starts to oscillate and becomes a more positive value when the system reaches to its equilibrium point, negative value is explained by the last one. The system cannot oscillate for all the time because the gm terms are decaying series. Here we use a common emitter or common base configuration that the feedback element is in series with parallel form.

![Fig2. Small signal model for the common-base configuration](image)

We chose the CB configuration as it can be seen in figure 2, because it oscillates more easily and represents an essential isolation from the output (collector) to input (emitter). The tank circuit connected at the emitter is represented by L and C. The R1 represents the load resistor at the collector. The Lb which will be explained later is an external inductor connected to base because it makes the oscillation easier. In this CB configuration it is assumed that the internal AC base resistance rb is much less than re the internal AC collector resistance, an supposition which is true because rb is less than 20 ohms while re, may well be in the ten megaohm confine. Suppose this, we can safely claim that there is a factor such that rm = a·rc. Here a is called the short circuit current product factor, a quantity header than or equal to unity, and rm is the transfer resistance of the BJT current producer. The importance of a in the definition of the oscillation situation is easily seen if we effort to find the input impedance of the last circuit. It can be easily proven that the input impedance is:

$$R_{in} = r_c + R_1$$

(5)

From 4 and 5 we can see that it is feasible for a common base configuration to develop a negative input resistance (since a > 1) if rb (or rb in series with some impedance) becomes sufficiently big. The last can be easily satisfied by the addition of an external device like the inductance Lb (Figure 2). In order to determine the stability of such a circuit let us assume that the admittance matrix of the composed device and base stub is Y consisting of parameters Yll, Yl2, Y21 and Y22. If the output terminal is terminated with a frequency-changing network Y_{load}, the input admittance is given by equation 7. After that if the input terminal is terminated by a frequency-changing network Y_{source}, and then the output admittance will be given by 8.

$$Y_{in} = y_{11} - y_{12} y_{22}/(y_{load} + y_{22})$$

(7)

$$Y_{out} = y_{22} - y_{12} y_{22}/(y_{source} + y_{11})$$

(8)

In equations 7 and 8, the stability of the device can be specify in two ways: the Linville stability factor (equation 9) or the condition in equation 10 which states than the Z (or Y) matrix of the complete circuit should be equal to 0.0

$$c = \frac{|y_{21} y_{12}|}{2Re(y_{11})Re(y_{22}) - Re(y_{21} y_{12})}$$

(9)

Where c > 1 for instability Or $|V| = |Z||I|$ where the defining of |Z| is equal to 0.0 for the onset of oscillation. We will use the second
style which gives us a little more insight into the work of the circuit. We add the output impedance $R_o$, the inductance $L_b$ and the varactor/inductor composition to the network. We get a network equal to the one in Figure 2. The following loop equation can then be result.

$$\begin{align*}
0 &= \left[ f(wL_e - 1/wC) + r_e + r_b + L_b \right] I_e + r_e + r_b + L_b \\
0 &= r_e + R_l + r_b + L_b \\
0 &= r_e + r_b + L_b \\
0 &= r_e I_e + I_e \\
0 &= 0
\end{align*}$$

(10)

The determinant of the above matrix must reduce to 0, so the last equation becomes:

$$j(wL_e - 1/wC)(r_e + R_l + r_b + L_b) + r_e(r_e + R_l) + (r_e + R_l + (1-a)r_e)(r_b + L_b) = 0$$

By setting the reactive part to 0.0 we can show that the oscillation frequency is:

$$f_0 = \frac{1}{(2\pi)} \sqrt{(1/LEC)}$$

(11)

Similarly, by setting the real part to 0 we can show that:

$$\alpha \geq \left[ 1 + \frac{R_l}{r_e} \right] \left[ 1 + \frac{r_e}{(r_b + L_b)} \right]$$

(12)

If $a > 1$ in 12 by properly choosing $R_l$ (i.e. the output matching circuit) and $L_b$ (the length of the micro strip inductor), we can ensure that the circuit will oscillate. Furthermore, by selecting the value of the capacitance/inductance at the emitter, we can set the circuit over a range.

### 3 Circuit simulations

A proper way for simulation of oscillating circuits is the nonlinear approach, which can be achieved by using Genesys from Agilent Technologies. The approach explain the active device with a nonlinear large signal S parameter model, and simulates the circuit using well defined aims for oscillation confine, fundamental and output harmonic power levels. The linearized approach explain in the section (5) include a simplistic method for the design of the unit. It tenders a prediction of the output oscillation confine but it has no insight into any of the circuit performance parameters associated with the nonlinear parts of the models. The first step in the simulation is to define the optimized base reactance at the defined frequency confine of work (Figure 2). This reactance is chosen to make certain that the transistor will oscillate at one frequency in the span of interest. The value of that inductance can be gain at by a simulation of the transistor in CB structure with the base stub present and including the parasitic, DC block capacitors and biasing circuit. The best choice for a stub length is one that achieves maximum amplitude for $S_{11}$ and $S_{22}$. In general, the longer the stub, the lower the frequency and vice versa. The optimum tool may be ideal for arriving at the correct value of the base inductance. Care should be taken to see that in the process of maximizing $S_{11}$ and $S_{22}$, $S_{21}$ is kept relatively stable, as that quantity will now roughly govern the linearity of the output power. To establish the qualification of oscillation, the following have to be:

$$\Gamma_1S_{11} = 1 \text{ and } \Gamma_1S_{22} = 1$$

(13)

We can continue the optimization by matching the output of the transistor, $S_{22}$, to the 50 ohm load. This is usually gained by maximizing $S_{11}$ while the output is conjugate matched. A typical output-matching circuit is a combination series/open stub. During the optimization process, the lengths of the series and open stubs are left to change freely while a goal of matching a 50 ohm load has been selected. Of course, this particular matching circuit is not the sole solution, just a simple choice out of many that the sketcher can use for effective matching to the load. Once the output has been matched, the input of the one port network, which now looks similar to the combined circuit in Figure 1, is drown. If the matching at the output was performed properly, the value of its reflection coefficient should still be much bigger than one. The output can either be plotted as $\delta S_{11osc}$ on the Smith chart in order to match any loops in the locus or in a tabulated form in order to match amplitude and phase to the reflection coefficient of the oscillator. Loops in the locus of the active device at this point may indicate a possibility for injection locking or spurious oscillations.

The resonator is made up of a network varactors and a stub which is short circuited to ground and acts as matching network to the transistor combination input. We simulated both sections of the circuit simultaneously. The results are
shown in a table that obviously shows the oscillation conditions for 500-1000 MHZ VCO.

Table 1. Various parameters as varactor is tuned

<table>
<thead>
<tr>
<th>F(GHz)</th>
<th>Mag. S11</th>
<th>Mag. S11_enc</th>
<th>&lt;S11</th>
<th>&lt;S11_enc</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.57</td>
<td>0.915</td>
<td>1.118</td>
<td>178.8</td>
<td>-179</td>
</tr>
<tr>
<td>0.74</td>
<td>0.925</td>
<td>1.993</td>
<td>150.7</td>
<td>-153</td>
</tr>
<tr>
<td>0.93</td>
<td>0.93</td>
<td>1.175</td>
<td>156</td>
<td>-156</td>
</tr>
</tbody>
</table>

Note that |S11| > |S11_enc| and <S11| = -<S11_enc|

4 Designing the hardware and test

In figure 3 a circuit diagram is shown which is a typical design. As it can be seen in figure 4 the printed circuit board which FR4 materials are applied in that and the components were put next together. The NEC’s NE85633 is used as a transistor its cut off frequency is 7 GHZ and its noise figure is 1.4db. We then tested the real VCO hardware. The device shows excellent phase noise characteristics, as it is shown in figure 5 typically at 650 MHZ: -96 dBc/Hz at 10 KHz from the carrier and -75 dBc/Hz at 1kHz. The changes in output power and the tuning voltage around the range for a 500-1000 MHz VCO is +/-2.5 db. The value of VSWR is 1.85:1 around the band or better. The tuning sensitivity is measured to be 50-70 MHz/V, and the measured value of absolute maximum tuning voltage is 25 Volts. The typical frequency pulling is 17 MHz peak to peak and 3 MHz per volt is the range of frequency pushing.

Table 2. Performance parameters of the VCO designed

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Tested Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency range</td>
<td>500-1000 MHz</td>
</tr>
<tr>
<td>Phase Noise</td>
<td>-96 dBc/Hz at 10 kHz offset</td>
</tr>
<tr>
<td>Amplitude</td>
<td>+13 dBm +/- 2.5 dB</td>
</tr>
<tr>
<td>Output VSWR</td>
<td>1.85:1</td>
</tr>
<tr>
<td>Tuning sensitivity</td>
<td>50-70 MHz/V</td>
</tr>
<tr>
<td>Frequency pulling</td>
<td>17 MHz</td>
</tr>
<tr>
<td>Frequency pushing</td>
<td>3 MHz/Volt</td>
</tr>
</tbody>
</table>

5 CONCLUSION

We described an accurate description of a method for designing a VCO, and we have demonstrated the results which have been
caused of applying this method to a wideband VCO model. The realized hardware covers the 500 to 1000 MHz frequency range and proper results have been achieved. There are good applications of this design and other designs based on this design in wideband front RF and in software-defined radio.

References: