Impact of the threshold voltage and transconductance parameters of NMOS transistors in NMOS inverter performance for static conditions of operation

MILAIM ZABELI, NEBI CAKA, MYZAFERE LIMANI, QAMIL KABASHI
Faculty of Electrical and Computer Engineering, Prishtina
Faculty of Applied Sciences, Mitrovica
University of Prishtina
10110 Prishtina, Fakulteti Teknik, Kodra e Diellit, p.n.
KOSOVA
{milaim.zabeli, nebi.caka, myzafere.limani, qamil.kabashi}@uni-pr.edu

Abstract: The objective of this paper is to show the influence of the parameters that characterize the NMOS transistors on the behavior of NMOS inverters in static operation mode, as well as set directive that should be followed during the design phase of NMOS inverters that enable designers to design inverters with the best possible performance, depending on operation conditions. Designing the NMOS inverter with the best possible features also enables the design of the logic circuits with the best possible performance, according to the operation conditions and designers’ requirements.

Key words: NMOS inverter, NMOS transistor, VTC characteristics, threshold voltage, critical voltages, noise margins, NMOS transconductance parameter.

1 Introduction
NMOS logic circuits represent the family of logic circuits which are realized with the highest packing density [1, 2, 3]. NMOS logic circuits contain only NMOS transistors, which enable to design circuits with smaller possible dimensions compared with other types of MOSFET transistors [3, 4]. The basic circuit in NMOS logic is NMOS inverter. Electrical and physical parameters that characterize the NMOS transistors determine the behavior of NMOS inverter, as for static conditions of operation, as well as dynamic conditions of operation [14]. The NMOS logic inverter is designed by interconnecting the two NMOS transistors; so that one of NMOS transistors plays the role of driver transistor and the other NMOS transistor play the role of nonlinear active load. NMOS inverters can be configured (designed) in several ways, but the configuration with depletion type of nonlinear active load achieves better performances compared with other configurations, so in particular will be discussed in the following [2]. The structure of NMOS logic inverter with depletion type of nonlinear active load is shown in Fig. 1.

![NMOS inverter configuration with depletion type NMOS load.](image)

Fig. 1 NMOS inverter configuration with depletion type NMOS load.

2 The role of the NMOS transistors parameters in characteristic properties of NMOS inverters.
Behavior of NMOS inverter with depletion-type NMOS load for static conditions of operation is described by the voltage transfer characteristic...
The characteristic properties that characterize the VTC characteristic are some critical voltage values at the input and output, as: \( V_{OH}, V_{OL}, V_{IL}, V_{IH} \) [2].

Critical voltage values are determined using combinations of operation regions (operation modes) of NMOS transistors, depending on the level of the output voltage values relative to the voltage values at the input of NMOS driver transistor (enhancement type NMOS). In Tab. 1 are shown the operating regions of NMOS transistors for critical voltage values at the input of driver transistor.

Tab. 1 Operating regions of NMOS transistors in NMOS inverter by critical voltage values.

<table>
<thead>
<tr>
<th>( V_{in} )</th>
<th>( V_o )</th>
<th>Operation region of driver transistor</th>
<th>Operation region of load transistor</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OL} )</td>
<td>( V_{OH} )</td>
<td>cut-off</td>
<td>linear</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>( \approx V_{OH} )</td>
<td>saturation</td>
<td>linear</td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>small</td>
<td>linear</td>
<td>saturation</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>( V_{OL} )</td>
<td>linear</td>
<td>saturation</td>
</tr>
</tbody>
</table>

NMOS transistors are constructed on the same substrate, therefore in NMOS transistor which acts as the load, the body effect must be taken in consideration [6, 7, 8, 9, 10, 11, 13].

\[
V_{t,l} = V_{t,0,l} + \gamma \left( \sqrt{2 \phi_F} + V_o - \sqrt{2 \phi_F} \right) \tag{1}
\]
\( V_{t,l} \) – threshold voltage of NMOS transistor as load,
\( V_{t,0,l} \) – threshold voltage of NMOS transistor as driver,
\( V_o \) – output voltage of NMOS inverter,
\( V_{in} \) – input voltage of NMOS inverter,
\( \phi_F \) – Fermi potential,
\( \lambda \) – body coefficient.

Using drain currents of NMOS transistors in NMOS inverter depending on the input voltage levels, respectively output voltage levels, and the necessary conditions to determine the critical values can be derived expressions for the critical voltage values at the input and output of NMOS inverter, as:

\[
V_{OH} = V_{DD} \tag{2}
\]

\[
V_{OL} = V_{OH} - V_{t,0,d} + \sqrt{(V_{OH} - V_{t,0,d})^2 - \frac{k_t}{k_d} V_{t,l}(V_{OL})^2} \tag{3}
\]

\[
V_{il} = V_{t,0,d} + \frac{k_t}{\sqrt{k_t k_d + k_d^2}} V_{t,l}(V_o) \tag{4}
\]

\[
V_{ih} = V_{t,0,d} + 2V_{t,l}(V_o) \sqrt{\frac{k_t}{3k_d}} \tag{5}
\]

\( k_t \) – transconductance parameter of NMOS transistor as load,
\( k_d \) – transconductance parameter of NMOS transistor as driver.

The values of output critical voltage \( V_{OL} \) are found using the numerical interaction between expressions (1) and (3), while the input critical voltage values \( V_{IL} \) and \( V_{IH} \) are found using the numerical interaction between expressions of the output voltage and the expressions for the critical values of voltage at the input. Interaction methods enable convergence of voltage critical values to the correct values. Also, static power dissipation which appears to output in low state (\( V_{OL} \)) depends on parameters of NMOS transistor as load [12].

\[
P_{DC} = \frac{k_t V_{DD} V_{t,l,1}^2}{4} \tag{6}
\]

Parameters that influence on the behavior of NMOS inverters for static conditions of operation are: the value of the threshold voltage of driver transistor, the value of the threshold voltage of load transistor, the ratio of the transconductance parameters of NMOS transistors and values of voltage source.

### 3 Results and Discussion

The impact of threshold voltage of NMOS-driver transistor and threshold voltage of NMOS-load transistor on the critical value of the output voltage \( V_{OL} \) when the ratio of NMOS transistors transconductance parameters has the value \( k_d / k_t = 1 \), \( \gamma = 0.126 V^{1/2} \), \( t_{ox} = 7.5 \) nm (the thickness of the oxide layer) and \( V_{DD} = 2.5 \) V are shown in Fig. 2 and Fig. 3.
Fig. 2 The dependence of the output voltage critical value \( V_{OL} \), as a function of the NMOS-load threshold voltage \( V_{t0,l} \), when \( V_{t0,d} = 0.5 \) V.

Presented results in Fig. 2 and Fig. 3 show that for the smaller absolute values of the load threshold voltage, as well as the smaller values of the driver threshold voltage, the output critical value \( V_{OL} \) is reduced to smaller values.

Impact of transconductance parameters ratio of NMOS transistors (by the driver-to-load ratio) in the output critical value \( V_{OL} \), when \( \gamma = 0.126 \) V\(^{1/2} \), \( t_{ox} = 7.5 \) nm, \( V_{t0,l} = -0.3 \) V, \( V_{t0,d} = 0.5 \) V and \( V_{DD} = 2.5 \) V is shown in Fig. 4.

From Fig. 4 it can be seen that for the higher value of the NMOS transconductance parameters ratio, the output critical voltage value \( V_{OL} \) is reduced to lower values with more significant impact on the band of small values.

The impact of the NMOS threshold voltage values and NMOS transconductance parameters ratio in input critical voltage values \( V_{IL} \) and \( V_{IH} \), where \( \gamma = 0.126 \) V\(^{1/2} \), \( t_{ox} = 7.5 \) nm and \( V_{DD} = 2.5 \) V are presented in Fig. 5, Fig. 6, Fig. 7, Fig. 8, Fig. 9 and Fig. 10.

Fig. 4 The dependence of the output critical value \( V_{OL} \), as a function of the NMOS transconductance parameters ratio \( k_d / k_l \).
Fig. 6 The dependence of the input critical voltage $V_{IL}$, as a function of the NMOS-driver transistor threshold voltage ($V_{t0,d}$), when the ratio of transconductance parameters $k_d/k_l = 2$ and $V_{t0,l} = -0.5$ V.

Fig. 7 The dependence of the input critical voltage $V_{IL}$ from NMOS transconductance parameters ratio ($k_d/k_l$), when $V_{t0,l} = -0.5$ V dhe $V_{t0,d} = 0.5$ V.

Fig. 8 The dependence of the input critical voltage $V_{IH}$, as a function of the NMOS-load transistor threshold voltage ($V_{t0,l}$), when the ratio of transconductance parameters $k_d/k_l = 2$ and $V_{t0,d} = 0.5$ V.

Fig. 9 The dependence of the input critical voltage $V_{IH}$ from NMOS-driver transistor threshold voltage ($V_{t0,d}$), when the ratio of transconductance parameters $k_d/k_l = 2$ and $V_{t0,l} = -0.5$ V.

Fig. 10 The dependence of the input critical voltage $V_{IH}$ from NMOS transconductance parameters ratio ($k_d/k_l$), when $V_{t0,l} = -0.5$ V dhe $V_{t0,d} = 0.5$ V.

The presented results from Fig. 5 to Fig. 10 show that for higher absolute values of the NMOS-load transistor threshold voltage, as well as the higher value of the NMOS-driver transistor threshold voltage, the input critical voltage values ($V_{IL}$ and $V_{IH}$) will have higher values, while for higher values of the NMOS transistors transconductance parameters ratio, the input critical voltage values will be lower, with more sensitivity in the low values band of the NMOS transconductance parameters ratio.

NMOS inverter noise margins for both logic voltage levels depend by input and output critical voltage values. The impact of the threshold voltage values and the ratio of NMOS transconductance parameters in noise margins are shown in Fig. 11, Fig. 12 and Fig. 13.
Fig. 11 The dependence of the noise margins for both logic levels ($NM_{L}$, $NM_{H}$), as a function of the NMOS-load transistor threshold voltage ($V_{t0,l}$), when $V_{t0,d} = 0.5 \text{ V}$ and $k_d/k_l = 2$.

Fig. 12 The dependence of the noise margins for both logic levels ($NM_{L}$, $NM_{H}$), as a function of the NMOS-driver transistor threshold voltage ($V_{t0,d}$) when $V_{t0,l} = -0.5 \text{ V}$ and $k_d/k_l = 2$.

Fig. 13 The dependence of the noise margins for both logic levels ($NM_{L}$, $NM_{H}$) from the NMOS transistors transconductance parameters ratio ($k_d/k_l$), when $V_{t0,l} = -0.5 \text{ V}$ and $V_{t0,d} = 0.5 \text{ V}$.

The presented results in Fig. 11, Fig. 12 and Fig. 13 show that for the lower absolute values of NMOS-load threshold voltage values, noise margins for high level ($NM_{H}$) will increase, while noise margin for low levels ($NM_{L}$) will decrease. For the lower values of NMOS-driver threshold voltage, noise margins for high level ($NM_{H}$) will increase, whereas it will decrease for the low level ($NM_{L}$). When value of NMOS transconductance parameters ratio increases, noise margins for the high level increase, whereas for the low level decrease.

In Fig. 14, Fig. 15 and Fig. 16 is shown the influence of the NMOS transistor threshold voltage values and the NMOS transistors transconductance parameters ratio in VTC characteristic shape. From presented characteristics show that for lower absolute values of NMOS-load transistor threshold voltage, and for lower values of NMOS-driver transistor threshold voltage, the VTC characteristic shift to the left, compared to the higher values and the slope of the VTC characteristic remains almost the same. While the value of NMOS transistors transconductance parameter ratio increases, the slope of the VTC characteristic rise and shows better switching performances.
Fig. 16 The VTC characteristic forms of NMOS inverter for some parametric values of NMOS transistors transconductance parameters ratio \((k_t = k_d/k_l)\) when: \(V_{t0,d} = 0.5\) V, \(V_{t0,l} = -0.5\) V, \(L = 0.18\) μm, \(W = 1\) μm and \(V_{DD} = 2.5\) V.

Conclusion

When during the design phase of NMOS inverter, the threshold voltage values of NMOS transistors and ratio of NMOS transistors transconductance parameters are controlled, or fit, NMOS inverter can be designed with high performance as for static conditions of operation, as well as for dynamic conditions of operations, depending on the designer requirements and operating conditions.

As for the output critical voltage value \(V_{OL}\), the transconductance parameter ratio of the NMOS transistors has a significant impact, compared to their threshold voltage values.

As for the input critical voltage value \(V_{IL}\), the transconductance parameter ratio of the NMOS transistors and the value of the NMOS-driver transistor threshold voltage have a significant impact.

As for the noise margin and the VTC characteristic slope, the ratio of NMOS transistors transconductance parameters has a dominant impact. When NMOS transistors transconductance parameters are matching, NMOS inverters can be designed with equal noise margin for two logic levels. Also for lower absolute value of NMOS-load transistor threshold voltage the static power dissipation results in lower value when NMOS inverter is in low output state \((V_{OL})\).

References:


