Comparison of 2k-Factorial and Taguchi Method for Optimization Approach in 32nm NMOS Device

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Abstract: - As silicon is now hit atomic resolution and reaching its physical and electrical limitation, producing a proper working transistor is tended to be harder and complicated. In this research, the effect of the process parameters variation on threshold voltage (V_{TH}) was investigated. The fabrication of the transistor device was performed using TCAD simulator, consisting of ATHENA and ATLAS modules. These two modules were combined with Taguchi method to optimize the process parameters. Initially, the comparison between two different statistical methods which is 2k-factorial designs, and Taguchi Method was being conducted. In this comparison, the effects of the process parameters variation on V_{TH} were studied. The most dominant or significant factors for S/N Ratio are halo implant energy, S/D implant dose and S/D implant energy. Meanwhile, the S/N Ratio values of V_{TH} after the optimization approaches for array L_8 is 23.8 dB. In L_8 experiments, V_{TH} value for NMOS device after optimizations approaches is +0.247V. The results obtained are closer to ITRS 2011 prediction. As conclusions, Taguchi Method was observed to be the most suitable method to be implemented in statistical modeling of 32nm NMOS device.

Key-Words: - Analysis of variance, Athena, Atlas, Taguchi Method, 2k-factorial

1 Introduction

CMOS circuits are traditionally designed in such a way that the manufactured circuits should meet the performance specifications such as speed and power consumption under all operating conditions. However, the statistical fluctuations in the semiconductor fabrication processes have resulted in undesirable variations in circuit performance [1]. The excessive spread of circuit performance can lead to a significant yield loss and hence can increase the unit cost of the product [2,3]. Therefore it is necessary to understand and model manufacturing process variations for the prediction of device and circuit performance and also to provide enough information for circuit designers in order to minimize the impact of parameter variation on the circuit performance and maximize the yield [4] .

One of the statistical methods for identifying semiconductor process parameters, whose variability would impact most on the device characteristics, is realized using Taguchi method [5]. Taguchi method has become a powerful tool for improving productivity during research and development. This is because the Taguchi method is a systematic application of design and analysis of experiments for the purpose of designing and enhancing product quality at the very early design stage [6]. A large number of experiments have to be executed when the number of the process parameters increases. In order to solve this problem, the Taguchi method implements a special design of orthogonal arrays to study the entire process parameter space with only a small number of experiments [5,7].

In the current study for the design of the experiment with a mixed matrix of 4 process parameters with 2 levels and 2 noise factors with 2 levels, there will be as many as 216 ($2^4 \times 2^2$) runs of testing if using the conventional full factorial design [8]. The testing of only 32 runs with the Taguchi method greatly reduces the number of tests and increases the efficiency. Using an orthogonal array to design the experiment could help the designers to study the influence of multiple controllable factors on the average of quality characteristics and the variations in a fast and economic way, while using a signal-to-noise ratio to analyze the experimental data could help the designers of the product or the manufacturer to easily find out the optimal parametric combinations [5,9].

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2 Material and Methods

P-type silicon with <100> orientation is used as the main substrate for this experiment. A 200Å oxide layer was grown on the top of the silicon bulk. This oxide layer is used as the mask for P-well implantation process. Then, the oxide layer was etched after the doping process was completed. It was followed by annealing process to strengthen the structure.

Next, Shallow Trench Isolation (STI) was developed to isolate neighbouring transistor. A 130 Å stress buffer was grown on the wafers with 25 min diffusion processes. Then, a 1350 Å nitride layer was deposited using the Low Pressure Chemical Vapour Deposition (LPCVD) process. This thin nitride layer was acted as the mask when silicon was etched to expose the STI area. Photo resistor layer was then deposited on the wafers, and unnecessary part will be etched using the Reactive Ion Etching (RIE) process. An oxide layer was grown on the trench sides to eliminate any impurity from entering the silicon substrate.

Chemical Mechanical polishing (CMP) was then applied to eliminate extra oxide on the wafers. Lastly, STI was annealed for 15 min at 900°C temperature. A sacrificial oxide layer was then grown and etched to eliminate defects on the surface. The gate oxide was grown and a Boron Difluoride (BF2) threshold-adjustment implant was done in the channel region through this oxide. The polysilicon gate was then deposited and defined followed by the halo implantation.

In order to get an optimum performance for NMOS device, indium was doped. Halo implantation was followed by depositing sidewall spacers. Sidewall spacers were then used as a mask for source/drain implantation. Arsenic atom was implanted at a desired concentration to ensure the smooth current flow in NMOS device. Silicide layer was formed and then annealed on the top of polysilicon.

The next step in this process was deposited of Boron Phosphor Silicate Glass (BPSG) layer. This layer will be acted as Pre-metal Dielectric (PMD), which is the first layer deposited on the wafer surface when a transistor was produced. This transistor was then connected with aluminum metal. After this process, the second aluminum layer was deposited on the top of the Intel-Metal Dielectric (IMD) and unwanted aluminum was etched to develop the contacts [10]. Once the devices were built with ATHENA, the complete devices can be simulated in ATLAS to provide specific characteristics such as the ID versus VGS curve. The threshold voltage (VTH) can be extracted from that curve [11].

2.1 2k-factorial Orthogonal using L8 Array Method

Electrical characteristic for NMOS device is done by obtaining the value of threshold voltage (V_{TH}). The value of response, V_{TH} is recorded for observing the dependability of the V_{TH} towards oxide growth temperature, V_{TH} implant energy, pocket-halo implant dose and compensate implant dose. The value of response, V_{TH} is used for the significant determinant whether the device is working well or not.

Table 1 shows the process parameters and their appropriate levels for the experiment. Process parameters that have been selected are oxide growth temperature, V_{TH} implant energy, pocket-halo implant dose and compensate implant energy. In this research, an L_8 (2^4) orthogonal array which has eight experiments are used. The experimental layout for the process parameters using the L_8 (2^4) orthogonal array is shown in Table 2.

Table 1. Process Parameters and their Levels

Symbol	Process Parameter	Unit	Level 1	Level 2
A	Oxide Growth Temp	^oC	808	810
B	V_{TH} Implant Energy	keV	5	6
C	Pocket Halo Implant Dose	atom cm^{-2}	2.73e13	2.75e13
D	Compensate Implant Dose	atom cm^{-2}	2.50e13	2.60e13

Table 2. 2k-factorial Experimental Layout using L_8 (2^4) orthogonal array

Exp. No.	Process Parameter			
	A	B	C	D
1	1	1	1	1
2	1	-1	1	-1
3	-1	1	1	-1
4	-1	-1	-1	-1
5	-1	1	-1	1
6	1	1	-1	-1
7	1	-1	-1	1
8	-1	-1	1	1

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2.2 Taguchi Orthogonal using L8 Array Method

Electrical characteristic for NMOS device is experimented by obtaining and controlling the value of threshold voltage, V_{TH}. The value of threshold voltage, V_{TH} is recorded for observing the dependability of the V_{TH} towards oxide growth temperature, V_{TH} implant energy, pocket-halo implant dose and compensate implant dose. The value of response, V_{TH} is used to determine whether the device is working well or not. The process parameters and their appropriate levels for the experiment using taguchi method can be referred in Table 1. For this method, two noise factors which are sacrificial oxide temperature and annealing process temperature are being used. These noise factors are varied for two levels in order to obtain four readings of V_{TH} for every row of experiment. The values of noise factors at different levels are listed in Table 3.

In this research, an L_8 (2^4) orthogonal array in taguchi method which has eight experiments are being used. The experimental layout for the process parameters using the L8 (24) orthogonal array is shown in Table 4. It is important to notice that the distribution of orthogonal array is slightly different compared to 2k-factorial method.

Table 3. Noise Factors and their Levels

Symbol	Noise factor	Unit	Level 1	Level 2
M	Sacrificial Oxide Temp	^oC	950	952
N	Anneal Process Temp	^oC	850	852

Table 4. Taguchi Experimental Layout using L_8 (2^4) orthogonal array

Exp. No.	Process Parameter			
	A	B	C	D
1	1	1	1	1
2	1	1	2	2
3	1	2	1	1
4	1	2	2	2
5	2	1	1	2
6	2	1	2	1
7	2	2	1	2
8	2	2	2	1

3 Result and Analysis

The electrical characteristics result of the first set of experiment done by using ATHENA and ATLAS module was discussed. Later, the optimization result of NMOS device by using 2k-factorial and Taguchi method approach were also shown in this section.

3.1 Analysis of 32nm NMOS device

Fig. 1 shows clearly on the doping concentration across the 32nm NMOS transistor. The figure also shows the tabulation of silicon, silicon dioxide, polysilicon, silicon nitride, cobalt nitride and aluminum. Doping concentration is one of the factors that will determine the electrical characterization of the transistor [9]. A good doping concentration will ensure the transistor working well with excellent gate control and fewer leakages current [11].

Fig. 2 shows the graph of drain current (I_d) versus gate voltage (V_G) at drain voltage V_D= 0.05V and voltage V_D=1.0V for NMOS device. The nominal value of threshold voltage for this device is 0.289 V [12].

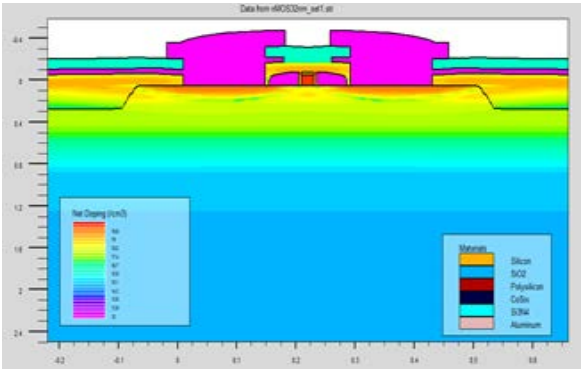

Fig. 1. Contour Mode of 32nm NMOS device

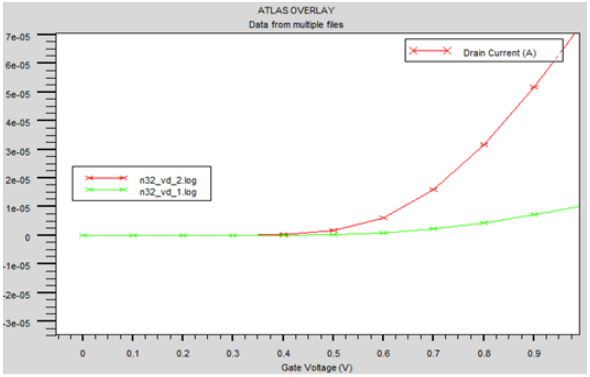

Fig. 2. Graph ID-VG for 32nm NMOS device

Several input process parameters needed to be varied in order to obtain the right or quite closed value to the nominal threshold voltage, V_{TH}. It is important to notice that all of the input process parameters cannot be varied randomly because it will affect the structure of the designed device. Therefore, statistically modeling is required to

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identify which process parameter variation would give the most significant impact on device characteristics. The results of V_{TH} will then be analyzed and processes with statistical modeling technique to obtain the optimal design. The optimized results will then be simulated in order to verify the predicted optimal design.

3.2 Analysis of 2k-factorial

This section describes optimization of input process parameters on threshold voltage in 32nm NMOS device by using 2k-factorial method. 2k-factorial enables experiment effect of several control factors implemented simultaneously on the certain process. Single repetition design is used for the experiment that involves many control factors [13]. Several experiments are run in order to determine which factor or variable that gives the most significant impact on the output response, V_{TH}. Besides that, it can also give the most recommendable value or optimum value for certain factor.

3.2.1 Threshold voltage acquisitions

By utilizing the TCAD Simulator, the threshold voltage for each individual experiment has been acquired. The process parameter level is varied according to the Table 2. The final results of the experiments are recorded in Table 5.

Table 5 shows the value of V_{TH} value for each set of experiment. Normally, the value of V_{TH} for below 90 nm NMOS device is within 0.1 to 0.6V. It is observed that all the experiment sets produce V_{TH} values are between 0.17 and 0.23V. Therefore, all the experiment set are suitable for the test of threshold voltage.

Table 5. V_{TH} Values for NMOS Device

Exp. No.	Process Parameter				V_{TH} (Volts)
	A	B	C	D	
1	1	1	1	1	0.1971
2	1	-1	1	-1	0.2183
3	-1	1	1	-1	0.2224
4	-1	-1	-1	-1	0.1996
5	-1	1	-1	1	0.1778
6	1	1	-1	-1	0.2032
7	1	-1	-1	1	0.1738
8	-1	-1	1	1	0.1933

Table 6. Estimation of Factor effect and Coefficient for V_{TH}

Term	Effect	Coefficient	SE Coef	T	P
A	-0.00017	-0.00009	0.000069	-1.27	0.293
B	0.00387	0.00194	0.000069	28.14	0.000
C	0.01917	0.00959	0.000069	139.26	0.000
D	-0.02537	-0.01269	0.000069	-184.29	0.000

3.2.2 Estimation of Factor Effects

Analysis of threshold voltage, V_{TH} data begin with the estimation of the effect of factor A, B, C and D towards the response, V_{TH} as shown in Table 6. From Table 6, it can be observed factor B, C and D contributes the most significant effect toward output response, V_{TH}. From the estimation effect analysis done from Table 6, normal plot for the standardize effects can be developed. All the effects along the line can be ignored. Only the significant effects which are located far from the line will be considered. Fig. 3 shows the significant factors towards response, V_{TH} are B, C and D which each of them representing V_{TH} implant energy, pocket-halo implant dose, and compress implant dose.

The guideline that has been used for this analysis is based on 95 percent confidence level. If there are any effects exceed this line, the effect is considered significant. Fig. 4 shows factor B, C and D give the most significant effect on the response, V_{TH}. Based on Pareto chart, main effects of factor B, C and D are plotted as in Fig. 5. Factor effect C which is pocket-halo implant is positive. Halo implantation has ability to reduce short channel effect. The halo also increases fluctuations in gate depletion, because it locally compensates the gate doping.

Therefore the threshold voltage (V_{TH}) will be increased when the dosage of pocket-halo implant being used is large. Next, factor effect B which is V_{TH} implant energy is observed to be positive. This show a higher V_{TH} implant energy would produces a higher V_{TH} value.

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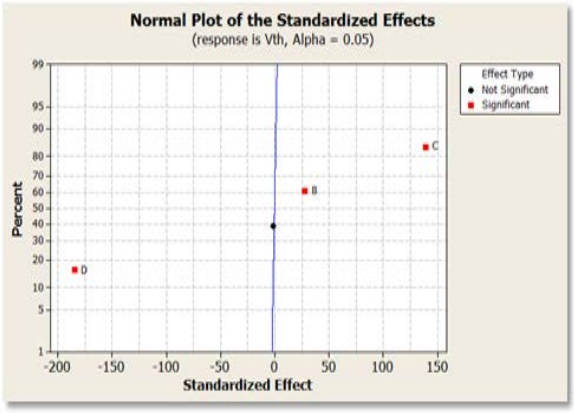

Fig. 3. Normal Plot of the Standardized Effects

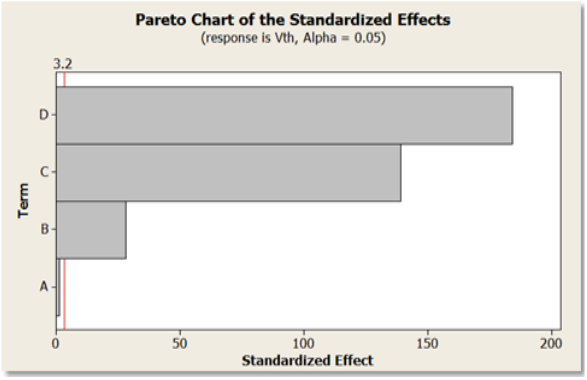

Fig. 4. Pareto Chart of the Standardized Effects

When using a higher energy ion implantation, the particles or atoms tend to react more rapid thus increasing the value of threshold voltage, $V_{TH.}$ But, if there is too much energy injected, it may damage the lattice or the atom structures.

From Fig. 5, it can be seen that factor effect D which named as compress implant dose is negative. This is because the value of V_{TH} is reduced as the increment of compress implant dose. Compress implantation is originally done for minimizing side capacitance.

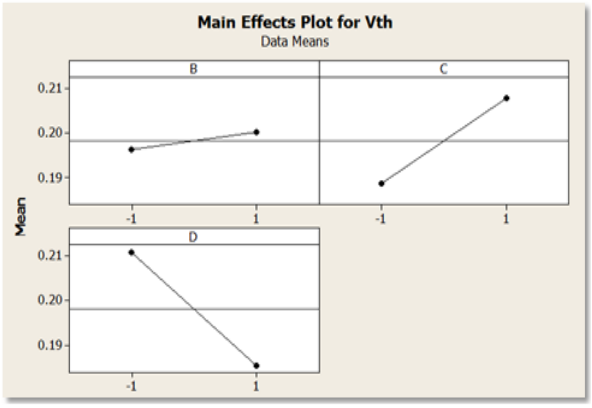

Fig. 5. Main Effects Plot for V_{TH}

3.2.3 Analysis of Variance for V_{TH}

For the purpose of upgrading the built model, factors that are not significant will be removed from the full model. Based on the analysis that has been done, factor A will be ignored because it is not significant. Only factor B, C and D will be analyzed in the new model. Analysis of variance for V_{TH} data are simplified as in Table 7 for investigating the residual error in the model.

Table 7. Analysis of Variance for V_{TH}

Source	DF	Seq SS	Adj MS	F	P
B	1	0.00003003	0.00003003	686.43	0.000
C	1	0.00073536	0.00073536	16808.26	0.000
D	1	0.00128778	0.00128778	29435.00	0.000
Residual Error	4	0.00000017	0.00000004		
Total	7	0.00205335			

R-Sq = 99.99% R-Sq(pred) = 99.97% R-Sq(adj) = 99.99%

P-value represents the probability of residual error involved in determining certain factor as a significant factor. Normally, the effect must be below than 0.05 in order to be considered as a significant factor which achieves 95 percent confident level. Based on the result in Table 7, all the main effect B, C and D are significant with the p-value equal to 0.00.

Residual error analysis can be implemented to ensure model adequacy and to check estimation. Analysis can be done only for main effects which are B, C and D. Normal probability plot for residual error is shown in Fig. 6. It is observed that all the points in the graph are located near to the straight line. Therefore, conclusion that has been made before which is only factor B, C and D have significant effect on V_{TH} is true.

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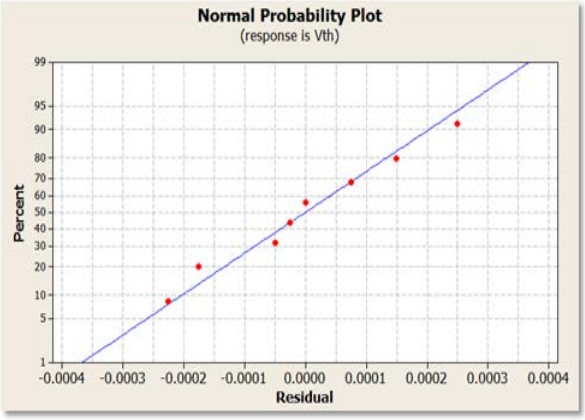

Fig. 6. Normal Probability Plot

3.2.4 Optimization analysis

Fig. 7 shows the optimization plot for the 2k-factorial design. It can be observed that the red color of the current value is the optimal level value for factor A, B, C and D. For factor A, B and C, the levels are set to be high level (1.0). Meanwhile for factor D, the level is set to be low (-1.0). Factor A, B, C and D each representing for oxide growth temperature, V_{TH} implant energy, pocket-halo implant dose and compensate implant energy.

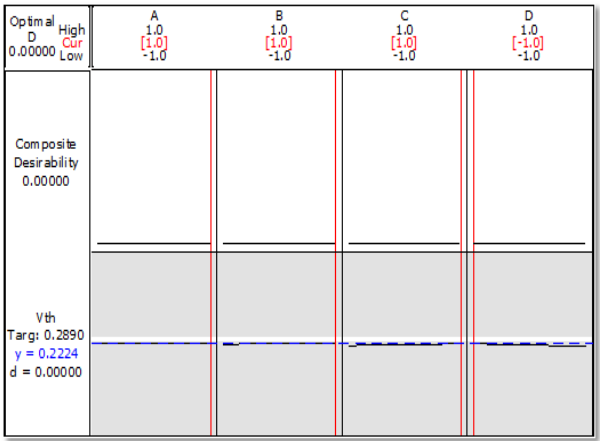

Fig. 7. Optimization Plot

Since the combination of the best setting for input process parameters level are not in the Table 5, the confirmation test has to be done by using TCAD tool. The final result of the confirmation experiment is observed to be 0.2223V as shown in Table 8. Therefore, this result is the nearest value of threshold voltage (VTH) to the expected or nominal value of 0.289V [12].

Table 8. Confirmation Experiment for V_{TH}

Experiment	Process Parameter				V_{TH} (Volts)
	A	B	C	D	
Confirmation	1	1	1	-1	0.2223

3.3 Analysis of Taguchi Method

Eight different experiments in NMOS device is performed using the design parameter in the specified orthogonal array table. Several experiments are run in order to determine which control factor or variable that contributes the most significant effect on the output response, V_{TH}. Besides that, it can also give the most recommendable value or optimum value for certain factor. There are four process parameters of NMOS device that is altered for observing the response, V_{TH} which are oxide growth temperature, V_{TH} implant energy, pocket-halo implant dose and compensate implant energy and each of them are represented by A, B, C and D.

3.3.1 Threshold voltage acquisitions

By utilizing the TCAD Simulator, Athena and Atlas, the threshold voltage for each individual experiment has been obtained. Table 9 shows the value of V_{TH} value for each set of experiment. Normally, the value of V_{TH} for below 90nm NMOS device is within 0V to 0.6V. It is observed that all the experiment sets produce V_{TH} values between 0.17V and 0.25V. Therefore, all the experiment set are suitable for the test of threshold voltage. From Table 9, it is observed that for each set of experiment, there are four different readings of V_{TH}. It is because of the presence of combination levels of noise factor represented by M_1N_1, M_1N_2, M_2N_1 and M_2N_2.

Table 9. V_{TH} Values for NMOS Device

Exp. No.	Threshold Voltage, V_{TH} (Volts)			
	V_{TH1} (M_1N_1)	V_{TH2} (M_1N_2)	V_{TH3} (M_2N_1)	V_{TH4} (M_2N_2)
1	0.1996	0.1905	0.2251	0.2159
2	0.1933	0.1842	0.2188	0.2096
3	0.2033	0.1942	0.2274	0.2182
4	0.1971	0.1880	0.2210	0.2118
5	0.1738	0.1645	0.1991	0.1898
6	0.2183	0.2091	0.2441	0.2350
7	0.1777	0.1685	0.2019	0.1926
8	0.2223	0.2133	0.2468	0.2377

3.3.2 Analysis of process parameter effects on threshold voltage

Threshold voltage (V_{TH}) for each individual experiment has been obtained by utilizing the TCAD simulator tool. The process parameter level is varied according to Table 1. Four specimens were simulated for each of the parameter combinations. The final results of the experiments are recorded in Table 9. After eight experiments of L_8 (2^4) array have been done, the next step is to determine which

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the control factor would give the most significant impact on the output response, V_{TH}. Signal-to-noise (S/N) ratio is utilized in order to figure out the optimal input process parameters and analyze the experimental data. There are three categories of the performance characteristics in the analysis of the S/N ratio (SNR) which are known as lower-the-better, higher-the-better and nominal-the-better [14]. The S/N ratio for each level of process parameters is computed based on the S/N analysis. Regardless of the type of the performance characteristic, the larger S/N ratio is always to be recognized as the better performance characteristic [15].

In this research, V_{TH} of the 32nm device is categorized to the nominal-the-best quality characteristics. The S/N ratio is implemented to obtain V_{TH} value that is closer or equal to a given target value (0.289V) which is also known as nominal value [15]. The S/N ratio (Nominal-the-best), η can be expressed as state in equation [5];

$$\eta = 10\mathrm{Log}_{10}\left[\frac{\mu^2}{\sigma^2}\right] \quad (1)$$

Where:

$$\mu = \frac{Y_1 + ... + Y_n}{n} \quad (2)$$

$$\sigma^2 = \frac{\sum_{i=1}^{n}(Y_i - \mu)^2}{n-1} \quad (3)$$

While n is the number of tests and Y_i the experimental value of the threshold voltage, μ is mean and σ is variance. In the nominal-the best, there are two types of factor to determine which are dominant and adjustment factors [5]. The S/N ratios (Nominal-the-best) for the device are computed and recorded in Table 10.

Table 10. Mean, variance and SNR for NMOS Device

Exp. No.	Mean	Variance	SNR (Mean)	SNR (Nominal-the-Best)
1	0.208	2.44E-04	-13.65	22.48
2	0.201	2.44E-04	-13.92	22.21
3	0.211	2.21E-04	-13.52	23.04
4	0.204	2.18E-04	-13.79	22.84
5	0.182	2.42E-04	-14.81	21.35
6	0.227	2.51E-04	-12.89	23.12
7	0.185	2.23E-04	-14.65	21.87
8	0.230	2.27E-04	-12.76	23.68

The effect of each input process parameter on the S/N ratio at different level will be separated out because the experimental design is orthogonal. The S/N ratio (SNR) for each of the process parameter is summarized in Table 11. In addition, the overall mean SNR for 8 sets of experiment is computed. Fig. 8 and Fig. 9 show the S/N ratio (SNR) and means graphs respectively for NMOS device. Basically, the larger the S/N ratio, the quality characteristic for threshold voltage is better [3]. The closer the quality characteristic value to the target, the better the device quality will be [15].

Table 11. S/N responses for V_{TH}

Symbol	Process Parameter	SNR (Nominal-the-Best)		Max - Min
		Level 1	Level 2	
A	Oxide Growth Temp.	48.90	49.87	0.97
B	V_{TH} Implant Energy	49.84	49.39	0.69
C	Pocket-Halo Implant Dose	49.41	50.05	1.14
D	Compensate Implant Dose	49.34	49.37	0.32

Overall mean of SNR=22.7dB

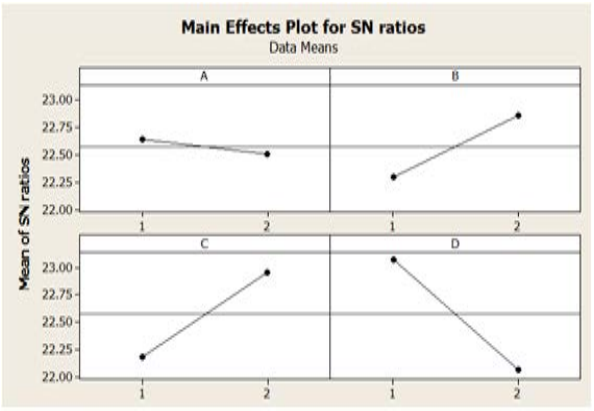

Fig. 8. SNR Graph for V_{TH} in NMOS Device

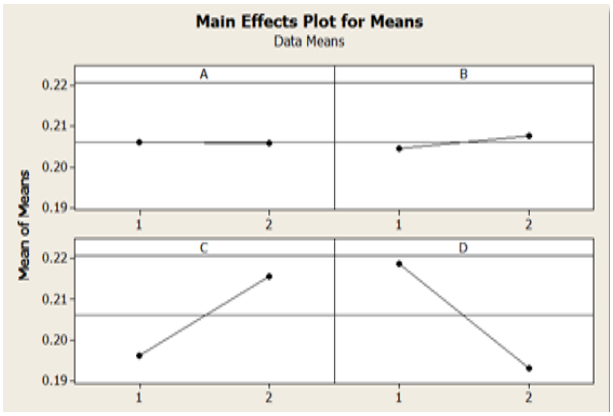

Fig. 9. Mean Graph for V_{TH} in NMOS Device

3.3.3 Analysis of variance (ANOVA)

The analysis of variance (ANOVA) is a common statistical method to investigate which of the input process parameters significantly affect the performance characteristic [16]. Basically it computes parameter called as sum of squares (SS), degree of freedom (DF), variance, F-value and percentage of each factor. F-value for each process parameter is actually the ratio variance due to the factor effect and variance due to the error term. It is used in order to measure the significant level of the factor with respect to the variance of all the factors included in error term. When the variance of error is zero, the F-value of factors A, B, C and D cannot be determined. Then the variance of the error can be combined with another smaller factor variance to calculate a new error variance which can be used to produce more accurate results. The process of disregarding an individual factor's contribution and then subsequently adjusting the contribution of the other factor is known as pooling. The results of ANOVA for the NMOS device are shown in Table 12.

Table 12. Result of ANOVA for V_{TH} in NMOS Device

Symbol	Process Parameters	DF	SSQ	Mean square	F-Value	Factor Effect on SNR (%)	Factor Effect on Mean (%)
A	Oxide Growth Temp	1	0	0	97	1	0
B	V_{TH} Implant Energy	1	1	1	1632	16	1
C	Pocket-Halo Implant Dose	1	1	1	3070	31	36
D	Compensate Implant Dose	1	2	2	5194	52	63

[a]At least 95% confidence

The percent factor effect on S/N ratio indicates the priority of a factor (process parameter) to reduce variation. For a factor with a high percent contribution and a small variance (mean square) will have a great influence on the performance [17].

The Pareto plot of standardized effect of V_{TH} for 32nm NMOS device is shown in Fig. 10. The Pareto plot compares the relative magnitude and the statistical significance of all the main effects and ranks of parameter accordingly. The effective plots are in decreasing order of the absolute value of the effects.

According to these analyses, the most dominant factors for S/N ratio are factor D (compensate implant dose – 52%), factor C (Pocket-halo implant dose – 31%) and factor B (V_{TH} implant energy – 16%). Therefore, these factors should be set at 'best setting' and not recommended to be used as an adjustment factors [5]. In order to describe an adjustment factor; it must have a large effect on mean and small effect on S/N ratio. Meanwhile, factor A is noted as neutral or negligible factor, so any level will not give any significant change on the response, V_{TH}.

In this case, the level of factor A is selected as level 2. Therefore, the best level setting of process parameters is selected as A_2, B_2, C_2 and D_1. Factor A, B, C and D each represents for oxide growth temperature, V_{TH} implant energy, pocket-halo implant dose and compensate implant dose. Since the value of S/N ratio of 23.8dB is within the range of 24.81dB and 22.69dB, this best setting will be allowed to be used.

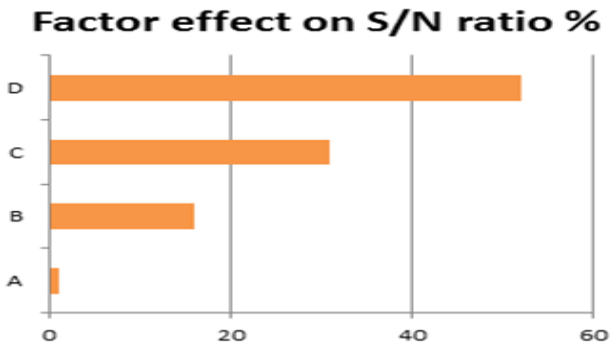

Fig. 10. Pareto plot of V_{TH} for NMOS Device

3.3.4 Confirmation Test for Response, V_{TH}

The confirmation test is used to verify the estimated result with the experimental results. Best setting of the process parameters for NMOS device that has effects on V_{TH} which had been suggested by Taguchi Method is shown in Table 13. The result of the final simulation for the device is shown in Table 14.

After the optimization approaches, the S/N ratio (Nominal-the-best) and S/N Ratio (Mean) of threshold voltage for NMOS device are 23.80dB and -13.70dB respectively as shown in Table 14. These values are within the predicted range. For S/N ratio (Nominal-the-best), 23.80dB is within predicted range S/N ratio of 24.81dB to 22.69dB (23.75 ± 1.06dB). Meanwhile, for S/N ratio (Mean),

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-13.70 dB is within the predicted range S/N ratio of -13.57 to -13.91 dB (-13.74 ± 0.17 dB).

These indicate that Taguchi method can predict the optimum solution in finding the 32nm NMOS fabrication recipe with appropriate threshold voltage value. The variance and threshold voltage (V_{TH}) for the device after optimization approaches are 0.227mV and 0.2468V respectively. The threshold voltage (V_{TH}) value after optimization approach is 14.6% different from the target value

Table 13. Best Setting of the Process Parameters

Symbol	Process Parameter	Units	Best Value
A	Oxide Growth Temperature	C^o	810
B	V_{TH} Implant Energy	kev	6
C	Pocket-Halo Implant Dose	atom cm^{-3}	2.75E13
D	Compensate Implant Dose	atom cm^{-3}	2.5E13

Table 14. Results of the Confirmation Experiment for V_{TH}

Threshold Voltage, V_{TH} (V)				SNR (Mean)	SNR (Nominal-the-best)
V_{TH1} (M_1N_1)	V_{TH2} (M_1N_2)	V_{TH3}(M_2N_1)	V_{TH4}(M_2N_2)		
0.2223	0.2133	0.2468	0.2377	-13.70dB	23.80dB

3.4 Comparison between 2k-factorial design and Taguchi Method

After implementing L_8 (2^4) orthogonal design for both 2k-factorial and Taguchi method, some comparison between these two designs are made. The comparison is done in order to determine which statistical method design is more suitable for the optimization of input process parameters of NMOS device. There are several factors that have been investigated and studied during the experiment.

First observation that has been made is to justify which statistical method would give closer value to the target or nominal value. In this experiment, threshold voltage, V_{TH} has been chosen for the output response of the experiment.

Therefore, after completing both type of analysis, it is observed that Taguchi Method has given closer value to the target value of 0.289 V [12] compared to 2k-factorial design. The output response produced by Taguchi method is observed to be at 0.2468V. Meanwhile, for 2k-factorial, the output response is observed to be at 0.2223V. This value is much far away from the target value compared to the output response produced by using Taguchi method. The reason why Taguchi Method can produce closer value to the target or nominal value than 2k-factorial is because the presence of noise factors. These noise factors enable Taguchi method to obtain four specimens of V_{TH} value for each set of experiment. Therefore, the probability to hit closer to the target value is higher compared to 2k-factorial design.

Second observation is about the adjustment factor. By using 2k-factorial, there is no room for adjustment on the level of the factor value can be made. Once it has been set to be the optimal value, the value cannot be adjusted for better setting (robustness). In contrast with Taguchi method, once the value has been set to be the optimal value, it can be adjusted if the factor is recognized to be neutral or adjustment factor. Because of this capability, Taguchi method is recognized to be the better statistical method in term of achieving the closest value to target or nominal value.

4 Conclusion

In conclusion, Taguchi Method was observed to be the most suitable method to be implemented in statistical modeling of 32nm NMOS device. It was because of Taguchi method had been proven to give the closer threshold voltage (V_{TH}) value to the nominal value compared to the 2k-factorial method. The optimum solution in designing the desired transistor was then successfully predicted by using Taguchi method. There are many physical limitations involved as the size gets smaller, approaching the molecular or atomic limitations of the substrate and dopant. Threshold voltage (V_{TH}) is the main response studied in this project as it is the main factor in determining whether the digital device works or not. Taguchi method design is used to develop a systematic design of experiment. It has many variants that can be applied to model the device, and a lot of input process parameters can be

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studied. Taguchi method has already been applied before to obtain a robust and better design. The level of significance of each input process parameter on the threshold voltage is determined by using ANOVA. Based on the ANOVA method, the high influent parameters on threshold voltage were found as factor D (compensate implant dose – 52%), factor C (Pocket-halo implant dose – 31%) and factor C (V_{TH} implant energy – 16%).

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