Study and Realisation of a Three-Level IGBT voltage source PWM Inverter using D.S.P controller (TMS320LF2407)

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Abstract: - In this paper, a sinusoidal pulse width modulation (SPWM) control of three-level neutral points clamped (NPC) voltage source inverter (VSI) is proposed. In first part, the structure and model of this power converter are presented. After that, a SPWM control strategy is developed and implemented. Finally, experimental results are presented using digital signal processor (DSP TMS 320LF2407).

Key words: - Digital Signal Processor (DSP), SPWM, Three-level inverter, IGBT, Numerical control, Matlab simulink.

1 Introduction

The multilevel converters are based on the neutral point clamped inverter topology proposed by Nabae. The multilevel voltage source inverter is recently applied in many industrial applications such as power supplies, static VAR compensatory, drive systems, etc.

One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing frequency, thus tree level inverters can be operated at lower switching frequency (fsw < 500 Hz).

A PWM inverter switches states many times during a single cycle of the resulting output voltage. At the time of these writing, reference voltages with frequencies as high as 12KHz are used in PWM inverter designs, so the components in a PWM inverter must change states up to 24,000 times per second. PMW inverters need high power, high frequency components such as GTO, Thyristors, and IGBTs transistors so they have the advantage for proper operation, they are the preferred components for building a PWM Inverters.

A synchronous three phase machine is used frequently in industry. They are simple, rugged, low cost and easy to maintain. They run essentially at constant speed from zero to full load.

The rapid development of power semiconductor devices has allowed to be used at the high switching frequencies thus made many changes in static power converter systems and industrial motor drive areas. Especially, the voltage source of pulse width modulation (PWM) inverters has been extending their application. They have great interests in the three-level inverter topology, which can overcome the series connections problems [1]. The three-level inverter is able to generate voltage without output transformer. Therefore, the harmonic components of the output voltage are fewer than those of conventional two-level inverters at the same switching frequency. In addition, when the blocking voltage of each switching device is a half of the dc link voltage, it is easy to produce high voltage and large capacity inverter system.

A block diagram representation of three-level voltage source inverter (VSI) is giving in figure 1. The inverter consists of twelve switching devices (represented as ideal switches) connected in the form of bridge. The control scheme is implemented using TMS320LF2407 DSP controller.

2 Modeling of a three-level inverter

2.1 General structure

The NPC multilevel inverter uses capacitors in series to divide up the DC bus voltage into different voltage levels. To produce m-levels in the phase voltage, an m-level NPC inverter needs m-1 capacitors on the dc bus. A three-phase three-level NPC inverter is shown in figure 1. The dc bus consists of two capacitors C. For a dc bus voltage Uc, the voltage across each capacitor is Uc/2 and each device voltage stress will be limited to one capacitor voltage level Uc/2 through clamping diodes [2],[3].
2.2 Different configurations of the inverter
To describe the different sequences of the inverter function, let us consider the possible states of the first leg switches figure 2.
The three-level inverter has the advantages that the blocking voltage of each switching device is one half of dc-link voltage whereas full dc-link voltage for two-level inverter.

2.3 Complementary command
We define the complementary control of the inverter leg as follows [4]:
\[
\begin{align*}
B_{k1} &= B_{k4} \\
B_{k2} &= B_{k3}
\end{align*}
\] (1)

It was demonstrated [4] that the command given by relationship (1) is the one which gives the three levels \(U_c\), \(0\), \(-U_c\), in an optimum way.

Table 1 shows the state of the switches and the corresponding output voltage of the inverter. Where \(V_k\) (\(k = a, b, c\)) is the potential of the leg.

<table>
<thead>
<tr>
<th>(B_{k1})</th>
<th>(B_{k2})</th>
<th>(B_{k3})</th>
<th>(B_{k4})</th>
<th>(V_k)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>-Uc2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Unknown</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Uc1</td>
</tr>
</tbody>
</table>

Table 1

Fig.1. Power circuit of NPC inverter

Fig.2. Different configurations of a leg
2.4 Model control of the three-level inverter - Connection functions

It defines the state of the switch, it equals 1 if the switch is ON and 0 if the switch is OFF. The connection functions of the three-level inverter are related by the following relation.

\[ F_{k1} = 1 - F_{k4} \]
\[ F_{k2} = 1 - F_{k3} \quad (k = a, b, c) \]  (2)

Therefore, the branch voltages \( V_{AM} \), \( V_{BM} \), \( V_{CM} \) are expressed as follow:

\[ V_{AM} = F_{11} \cdot F_{12} \cdot U_{C1} - F_{13} \cdot F_{14} \cdot U_{c2} \]
\[ V_{BM} = F_{21} \cdot F_{22} \cdot U_{C1} - F_{23} \cdot F_{24} \cdot U_{c2} \]  (3)
\[ V_{CM} = F_{31} \cdot F_{32} \cdot U_{C1} - F_{33} \cdot F_{34} \cdot U_{c2} \]

However, the output phase voltage of the inverter can be deduced from the relation (3) as follow:

\[ V_A = (2V_{AM} - V_{BM} - V_{CM}) / 3 \]
\[ V_B = (2V_{BM} - V_{CM} - V_{AM}) / 3 \]  (4)
\[ V_C = (2V_{CM} - V_{AM} - V_{BM}) / 3 \]

These equations can be rewritten using the voltage branches which give:

\[
\begin{bmatrix}
V_A \\
V_B \\
V_C
\end{bmatrix} = \frac{1}{3} \begin{bmatrix}
2 & -1 & -1 \\
-1 & 2 & -1 \\
-1 & -1 & 2
\end{bmatrix} \begin{bmatrix}
F_{11} \\
F_{12} \\
F_{14}
\end{bmatrix} \begin{bmatrix}
U_{C1} \\
F_{22} \\
F_{24}
\end{bmatrix} - \frac{1}{3} \begin{bmatrix}
F_{13} \\
F_{14} \\
F_{33}
\end{bmatrix} \begin{bmatrix}
U_{c2} \\
F_{23} \\
F_{34}
\end{bmatrix} \]  (5)

In most applications, AC machines are preferable to DC machines due to their easy and more robust construction without any mechanical switch. DC motors have been used in the high-performance domain, with requires fast and precise torque control. However, due to the advancement in micro-and power electronics, high-performance control of ac motors can now be implemented at a reasonable cost.

The vector control concept has become a standard tool for high-performance control of ac motors. The ultimate objective of vector control is to enable decoupling control of torque and flux similar to the control of a separately excited dc motor.

In the case of squirrel cage induction motor drive systems, the direct and indirect methods of vector control have been applied. The direct method requires the difficult task of flux acquisition for field orientation. The indirect method is basically a forward slip frequency control scheme that does not require flux acquisition. Both methods provide decoupling control of torque and flux. However, the indirect method is gaining popularity due to simplicity of implementation and which is applied in this paper.

3 PWM strategy and simulation results

The parameters of PWM control technique are definite as: Amplitude modulation index \( m_a \) and the frequency ratio \( m_f \).

\[ m_a = A_m / A_c \]  (6)
\[ m_f = f_c / f_m \]  (7)

where \( A_m \) is the peak amplitude of the control signal, while \( A_c \) is the peak amplitude of triangle signal (carrier).

\( m_f \) is the ratio between the carrier and the control frequency.

The one carrier PWM three level inverter algorithm is:

\[
\begin{cases}
|V_{ref}| \leq U_p \Rightarrow B_{11} = 1, B_{12} = 0 \\
|V_{ref}| > U_p \text{ et } V_{ref} < 0 \Rightarrow B_{11} = B_{12} = 0 \\
|V_{ref}| > U_p \text{ et } V_{ref} > 0 \Rightarrow B_{11} = B_{12} = 1
\end{cases}
\]  (8)

Where: \( V_{ref} \) is called modulating signal
\( U_p \) is the carrier signal

Table 2 shows the truth table of the algorithm [4].

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>B11</th>
<th>B12</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 2

Where:

\( A = 1 \) when \( V_{ref} > 0 \) if not \( A = 0 \)
\( B = 1 \) when \( |V_{ref}| > U_p \) if not \( A = 0 \)

The logical expressions of \( B_{11} \) and \( B_{12} \) are:

\[ B_{11} = \overline{B}_{14} = \overline{B} + A \]
\[ B_{12} = \overline{B}_{12} = AB \]  (9)
The synoptic diagram of the proposed realisation of the strategy is shown in figure 3 [5], [6].

![Synoptic Diagram](image)

**Fig.3. Synoptic of the proposed PWM strategy**

To illustrate the performance of the three-level PWM inverter, the systems was investigated through computer simulation under no load. Figure4, shows the phase voltage at \( m=24 \) and \( m_i=0.8 \) with a sinusoidal triangle PWM and contains harmonics greater which can be easily filtered and the results are much better than conventional two–level inverter. The comparison of the reference sinusoidal signal with the triangular waveform is done in the PWM generator of the DSP to generate the control signals for the switching devices along with the inverted signals with the required dead band.

By taking the following parameters:
- \( R=22 \) \( \Omega \), \( L=340\text{mH} \), \( m=24 \), \( m_i=0.8 \). \( U_c/2=30\text{V} \), \( f=50\text{Hz} \).

The obtained simulation results are illustrated by figure 4, 5, 6, 7, 8.
Figure 4 shows the simulation sequences of upper-arm.

Figure 5 shows the line voltage $V_{ab}$, it has five voltage levels $2Uc/2$, $Uc/2$, 0, $-Uc/2$, $2Uc/2$.

Figure 6 shows the output voltage of the first phase of the inverter.

Figure 7 shows the $V_A$ analysis spectral. The voltage spectrum shows that the harmonics are grouped into multiple frequencies centered around the frequency switching families. The most important harmonics are numbered number 23 and 25.

Figure 8 shows the voltage $V_{AM}$, it shows three levels of output voltage of an arm $Uc/2$, $-Uc/2$.

Figure 9 shows the evolution of the amplitude of the fundamental output voltage $V_A$ based rate setting $m_a$.

Figure 10 shows the curve of the harmonic content in terms of $m_a$. We note that the harmonics decreases as $m_a$ increases.

4 Experimental test
The schematic diagram of the converter circuit implemented is given in figure 11. It has two parts, the control circuit and the power circuit.

The shaded part is the control circuit containing the DSP controller TMS320LF2407 that generates the PWM signals and also provides soft start function [9].
Later on, the three-level inverter was implemented using DSP TMS320LF2407 and its performance was studied. A comparison is made of the results obtained through simulation and experimental work under the same operating conditions. To verify the theoretical results obtained on the three-level inverter, we designed and built the various circuits forming the full inverter.

A power circuit formed by two arms, formed by twelve transistors I.G.B.T and eighteen diodes connected in anti-parallel. The generated control signals were obtained using several control cards such as conditioning, monitoring, D/A conversion cards.

Figure 11 Shows the D.S.P. TMS320LF2407 implementation diagram.

The DSP programming was based on the software developed by Texas Instruments “Code composer”.

The control algorithm has been written in assembly language in order to optimize the whole tasks of operation and communication between the DSP, the Converter and the Load [10].

After the construction of the various circuits, the three-level inverter was tested in the laboratory; it functioned as an inverter supplying a passive load formed by a resistance and an inductance. The oscillographic results obtained are given in figure 12, 13, 14, 15.

For a triangulo-sinusoidal strategy, a cyclic ratio equal to 0.8 and the index of modulation equals 24 were taken.
Figure 12 clearly shows the $V_{AM}$ voltage variation. The waveform of the voltage is similar to that obtained from the simulation, the difference in the zero level of the voltage that is a little shifted. This is due to the imbalance of the midpoint.

Figure 13 shows the change in the voltage of the first phase $V_A$. Both $V_A$ voltage obtained in simulation and experiments almost the same.

The $V_{AB}$ voltage was presented in figure 14. Experimental control pulses were shown in figure 14.

Both voltages ($V_{AM}$, $V_A$, $V_{AB}$, $B_{11}$) of three level inverter obtained in simulation and experiments almost the same.

5 Conclusion
Simulation and experimental results show the feasibility of such a system. The low commutation frequency of three-level inverters permits a realization of an optimal control by relatively simple tools. With a high number of semiconductors devices, current quality is improved and weight reduced by avoiding heavy current filters.

The control voltage was controlled by microcomputer in a much more sophisticated manner than that described here. This work opens new ways for future research because the inverter can be controlled by numerical control. The results obtained are satisfactory and the harmonic components of the output phase are fewer than those of conventional two-level inverters at same switching frequency. A fuel cell, battery and solar cell can be a source of power for our inverter which it is well suited for a low input voltage.

References