Soft-Switching performance of Dual Active Bridge DC-DC Converter

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Abstract: - This paper presents the Zero-Voltage Switching (ZVS) performance of Dual Active Bridge (DAB) DC-DC converter for high power density aerospace applications. Switching transitions of the transistor occurring in favorable conditions such as device zero-voltage or zero-current is called as soft-switching. The benefits of soft-switching are reduced switching losses, switch stress, low electromagnetic interference and easier thermal management. These are essential features for high frequency operation of power converters. The DAB converter topology has been chosen as it features high power density, high efficiency, bidirectional power flow capability, inherent soft switching, galvanic isolation and low number of passive components. Hence the converter is a candidate for high power density aerospace applications. For performance evaluation, input side of the converter is connected to the high voltage (HV) DC bus and output side of the converter is connected to the low voltage (LV) ultracapacitor. A DAB converter is modelled using SABER software. SABER simulation results under ZVS verify the soft-switching performance of the DAB DC-DC converter.

Key-Words: - DC-DC converter, Zero-voltage switching, Dual active bridge topology, High power density, Soft-switching operation, Galvanic isolation.

1 Introduction

The interest in Dual Active Bridge (DAB) converter topology for high power density applications such as aerospace applications is increasing rapidly due to its attractive features. However, most of the soft switching techniques employed for DAB converters improve performance at the expense of introducing additional active and passive components. The first article on a DAB converter [1], published 17 years ago, highlighted its performance for high power applications. Subsequently, several papers were published [2-6] on the converter performance, accompanied by comprehensive analysis. Design considerations for high frequency transformers used in DAB converters were concerned with core material selection, loss minimisation and realisation of controlled leakage inductances as discussed in [7-8]. A comparative evaluation of the DAB topology with other isolated converter topologies was reported in [9-10] and soft switching techniques to enhance the performance were presented in [11-14]. Various modulation techniques and control strategies to minimise the losses were investigated in [15-18]. This paper discusses the inherent soft-switching phenomenon of the DAB converter at high power and high frequency operating conditions.

2 Problem Formulation

This paper presents the DAB converter soft-switching operational performance for high power density aerospace applications. The DAB converter shown in Figure 1 consists of two full-bridge circuits connected through an isolation transformer and a coupling inductor L, which may be provided partly or entirely by the transformer leakage inductance. The full bridge on the left-hand-side of Figure 1 is connected to the high voltage (HV) DC bus and the full-bridge on the right-hand-side is connected to a low voltage (LV) ultracapacitor.

Each bridge is controlled to generate a high-frequency square-wave voltage at its transformer terminals of the same frequency.

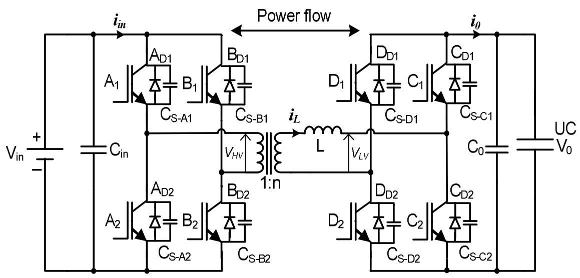

Fig. 1 (a) Schematic of the DAB DC-DC converter with loss-less snubber

The two square-waves can be phase-shifted with respect to each other to control the power flow through the transformer and inductor. Thus power can be made to flow from V_{in} to V_0 or vice versa. Power always flows from the bridge generating the leading square-wave to the other bridge [1].

For illustration purposes, the switching devices on the HV side are labelled ‘A’ and ‘B’ and those on the LV side are indicated ‘C’ and ‘D’. In order to differentiate the devices located in the top and bottom portions of each leg, the devices located in the top of each leg are affixed with a subscript ‘1’ and the devices in the bottom of each leg are affixed with a subscript ‘2’. The anti-parallel diode across each device is named in the same manner with an additional subscript ‘D’.

Simple snubber capacitors were used to reduce the turn-off switching loss of the devices. These capacitors slow down the rate of voltage rise across the devices so that a lower voltage appears during the current decay time. Figure 1 shows the schematic of the DAB converter with snubber capacitors C_s across all the devices. These capacitors are identified with the subscript of their respective parallel devices. The effect of the added snubber capacitors during device turn-off is explained in the following paragraphs, starting with the HV device turn-off and followed by the LV device. Two devices are turned-on or turned-off at any switching instant in each case. Hence, an explanation is provided for one device with the other device details in brackets.

2.1 Soft-switching operation

Assuming that initially transistor A_1 (B_2) is on and forward current flows through the device during the on-state. The snubber current is zero and the snubber capacitor $C_{s\text{-}A1}$ ($C_{s\text{-}B2}$) is uncharged. Now transistor A_1 (B_2) stops conducting and all the other devices are not in conduction. The turn-off time of the device is considered to be negligible, and the value of snubber capacitor is sufficiently high to ensure very little change in the voltage across the transistor during its turn-off time. Without the capacitor, the voltage across transistor A_1 (B_2) would rapidly rise to V_{in} with high *dv/dt*. If parasitic inductance is present, this may lead to a device over voltage. The snubber reduces this high *dv/dt* by conducting the device turn-off current. Therefore, during the device A_1 (B_2) turn-off, the current in coupling inductor *L* discharges $C_{s\text{-}A2}$ ($C_{s\text{-}B1}$) and charges $C_{s\text{-}A1}$ ($C_{s\text{-}B2}$) in a resonant manner until their respective voltages reach the opposite rails, at which point, if the current is still positive, diode A_{D2} (B_{D1}) turns on, clamping the voltage across $C_{s\text{-}A2}$ ($C_{s\text{-}B1}$) to zero and that of $C_{s\text{-}A1}$ ($C_{s\text{-}B2}$) to V_{in}.

The upper devices in each leg are switched in anti-phase with the lower devices of the same leg. However, there is a short period after a transistor in a leg turns off before the other transistor in the leg is turned on. This period is termed as a dead-time. The dead-time should be longer than the snubber charging time to prevent high current pulses. Hence, after the dead time, a gate drive signal is applied to A_2 (B_1); later current is transferred from A_{D2} (B_{D1}) to A_2 (B_1) under ZVS. This is depicted in Figure 2 for the turn-off instant of transistors A_1 and B_2.

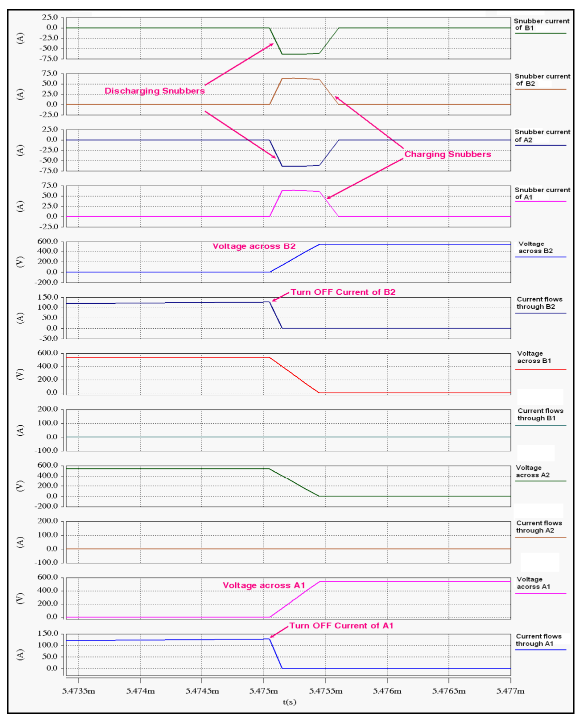

Figure 2 Turn-off of transistor A_1 and B_2 at d = 0.5, V_{HV} = 540V, V_{LV} = 62.5V, L = 2.11μH, C_s = 47nF, I_{OFF} = 128A, f_s = 20 kHz

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Figure 2 depicts SABER simulations of the voltage across and current flowing through all the HV side devices, and the charging/discharging current of HV side snubbers. Similarly, in the LV bridge, assume that transistor C_1 (D_2) is on, forward current flows through the transistor and the snubber current is zero. Thus the capacitor $C_{s\text{-}C1}$ ($C_{s\text{-}D2}$) is discharged. When transistor C_1 (D_2) stops conducting, the snubber capacitor reduces the high *dv/dt* by conducting the current. Thereby the current in the coupling inductor L discharges $C_{s\text{-}C2}$ ($C_{s\text{-}D1}$) and charges $C_{s\text{-}C1}$ ($C_{s\text{-}D2}$) in a resonant manner. As a result, their respective voltages reach the opposite rails. Now, if the current is still positive, diode C_{D2} (D_{D1}) turns on clamping the voltage across $C_{s\text{-}C2}$ ($C_{s\text{-}D1}$) to zero and that of $C_{s\text{-}C1}$ ($C_{s\text{-}D2}$) to V_0. The gate control signal is applied after the dead-time duration to C_2 (D_1); hence, current is transferred from C_{D2} (D_{D1}) to C_2 (D_1) under ZVS. The switching instant of transistors C_1 and D_2 can be observed in the simulation of Figure 3.

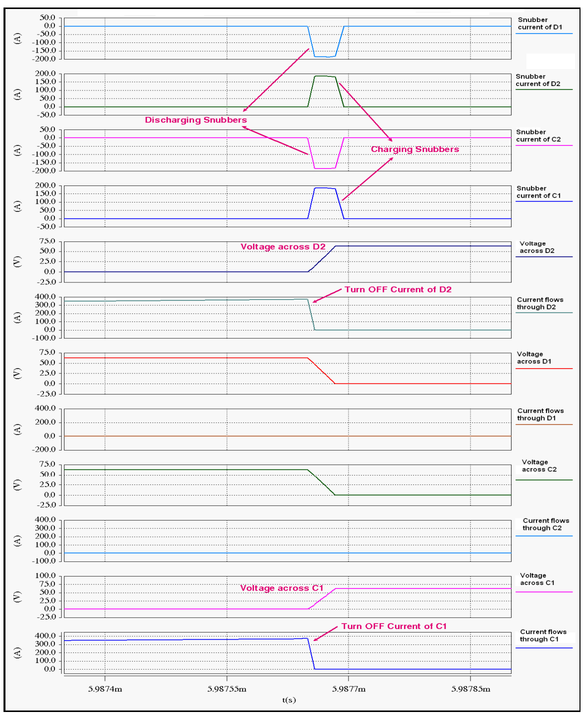

Figure 3 Turn-off of transistor C_1 and D_2 at d = 0.5, V_{HV} = 540V, V_{LV} = 125V, L = 2.11µH, C_s = 100nF, I_{OFF} = 371A, f_s = 20 kHz

The snubber capacitor allows device current to fall before the device voltage rises significantly during the switching period; thereby it minimises the turn-off switching loss. It limits the rise time of voltage across the transistor during turn-off. This limitation of *dv/dt* can be observed on the inclined edges of transistor voltage waveform shown in Figures 2 and 3. Hence, all the devices turn-on and turn-off under ZVS with reduced stress.

In the absence of a snubber capacitor across the device during turn-off, resonance would naturally occur between device output capacitance and the coupling inductance. The energy stored in the coupling inductance would be sufficient to ensure charge/discharge of device output capacitances at the switching instants. Normally, the device output capacitance is of low value and would not be enough to produce a low *dv/dt*. As a result, there would be a high rate of initial current fall (*di/dt*) with a rapid voltage rise (*dv/dt*) across the device, during turn-off. This produces turn-off switching loss and device stress. If stray inductance is present in the circuit, this can result in a device over voltage. Values mentioned in Figure captions 2 and 3 are likely similar to future aerospace systems [19].

3 Problem Solution

The converter operating conditions to achieve virtually loss-less zero-voltage switching conditions are:

- At turn-on of any device, its anti-parallel diode is conducting and
- At turn-off of any device, the minimum current flow through the device is positive

In practice, the zero-voltage switching limits will be imperfect since the inductor current must always be large enough to charge/discharge the device output capacitances at the switching instants. The key equations of the DAB converter to achieve soft-switching operation are summarized below. The detailed derivation can be found in [19].

By applying zero-voltage switching conditions to the device current waveforms of the DAB converter, the current at the LV switching instant must be greater than zero to achieve ZVS in the LV bridge. Therefore, the following condition must be satisfied for ZVS in the LV bridge:

$$I_{L1} = \frac{T_S}{4L}\left[nV_{in}(2d-1)+V_0\right] \geq 0 \qquad (1)$$

Solving for the inequality given in (1), the duty ratio at which ZVS occurs is obtained as,

$$d \geq 0.5 - \frac{V_0^{'}}{2} \qquad (2)$$

Where $V_0^{'} = \dfrac{V_0}{nV_{in}}$ is the normalized voltage conversion ratio.

If $V_0^{'} > 1$, the zero-voltage switching limit still occurs in the LV bridge, but is now given by the condition:

$$d \geq 0.5 - \frac{1}{2V_0^{'}} \tag{3}$$

The expression for the minimum inductor current during transistor turn-off is given by,

$$I_L = 2\sqrt{\frac{V_0^{'} V_{in}}{L'/C_S}} \tag{4}$$

$$I_L = 2\frac{\sqrt{V_0^{'} V_{in}}}{Z}, \tag{5}$$

Where $Z = \sqrt{L'/C_S}$

Thus the inductor current should be greater than or equal to the value of I_L in equation (4) during transistor turn-off to achieve ZVS. Although the turn-on of transistors is achieved at minimum (near-zero) positive diode current, the instantaneous transistor currents that occur during the turn-off process are significant. Hence, minimal transistor currents during the turn-off switching time instant are mandatory in order to achieve low switching losses. In order to enhance the converter performance and minimise switching losses, snubber capacitors, C_s, have been introduced across all the switches in the DAB converter circuit, see Figure 1.

From the above analysis, it is clear that in order to achieve soft switching, the minimum inductor current required must equal the value obtained from (4) during device turn-off to benefit from ZVS operation. Although inclusion of snubber capacitors decreases the device switching losses, the minimum current required during turn-off restricts the output voltage and output current region available for soft-switching operation.

Figure 4 depicts the ZVS boundary waveforms of the converter with 100nF snubber capacitors. Figure 4 shows the voltages generated by the two full-bridges V_{HV} and V_{LV}, the current flowing through the coupling inductance i_L, the device currents on the LV side i_{C1}, i_{CD1}, the LV side device voltage V_{C1}, the charging and discharging snubber currents of transistors C_1 and C_2. Based on the theoretical analysis, the expected steady-state value during ZVS boundary operation is, I_{L1} = 35.78A. Once again the steady-state analysis value is found to be in close agreement with the simulation results. From Figure 4, the instantaneous value of inductor current during device turn-off is found to be 35.78A, which is also the minimum current requirement necessary to achieve ZVS with 100nF snubber as estimated by the analysis in this section (4), thus demonstrating the accuracy of the analysis.

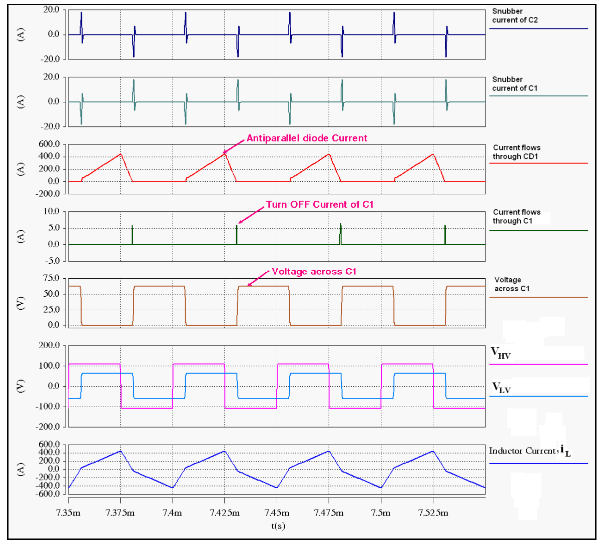

Figure 4 Simulation results for ZVS boundary of the DAB converter during charging mode with 100nF snubber V_{HV} = 540V, n = 1: 0.2, V_{LV} = 62.5V, d = 0.2386, P_0 = 14.5kW, I_0 = 232A, f_s = 20kHz, L = 2.11μH

4 Conclusion

This paper presented the soft-switching performance verification of the DAB DC-DC converter for high power density aerospace systems. The DAB converter has been modeled using SABER package. The simulation results obtained for DAB converter verify its performance during ZVS operating modes for ultracapacitor based aerospace energy storage systems. The results confirm that the transistors in DAB converters are subjected to reduced stress and switching losses of their inherent soft-switching feature with the inclusion of snubber capacitors.

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