A Low Power High CMRR CMOS Instrumentation Amplifier Based on Differential Voltage – Current Conveyor for Beta-Dispersion Range Bio-Impedance Applications

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Abstract: - In this paper, a low power and high CMRR Instrumentation Amplifier is presented. It has been designed for use in Bio-Impedance (BI) applications that operate within the beta dispersion frequency range. An IA with a high CMRR and input impedance allows the extraction of the low amplitude BI signal while reducing the error signals and noise associated with the tissue and instrument interface. These result from the parasitic impedances of the electrodes and their corresponding half-cell potentials, the finite output impedance of the current source, and the common-mode signals coupled to the current source. The IA has a current-mode structure utilizing a Differential Voltage Current Conveyor (DVCC) to provide most of the CMRR. This structure has an improved performance with regard to CMRR and operating frequency as compared to voltage-mode topologies. The DVCC is coupled to a Folded-Cascode Operational Transconductance Amplifier (FC-OTA) which provides the voltage gain. The FC-OTA is coupled to an analog buffer that serves as the output drive stage. The IA has been designed using TSMC 0.35µm CMOS 2P4M Technology. The pre-layout and post-layout performance of the IA has been verified using HSPICE. The layout was done in LAKER. The IA has achieved, in post-layout simulation, a CMRR of 98dB, an input impedance of 4.85MΩ (differential mode) and 1.4MΩ (common-mode) at 1MHz, a DC voltage gain of 67dB, and a Unity Gain Bandwidth (UGBW) of 7.2MHz. The IA's power dissipation is only 1.27mW in open-loop configuration. Transient simulations using an interface model at 1MHz of frequency showed a Total Harmonic Distortion (THD) of only 1.9%, a Signal to Noise Ratio (SNR) of 49.5dB and a Spurious Free Dynamic Range (SFDR) of 33.dB. The IA has a layout area of 250µm x 250µm.

Key-Words: - Current-Mode Instrumentation Amplifier, Bio-Impedance, CMRR, CMOS, DVCC, FC-OTA, Analog Buffer

1 Introduction

The response of a cellular suspension to an AC excitation current has been categorized into three dispersions namely: α, β and γ [1]. These are summarized in Fig. 1. Most BI researches utilize the α and β dispersion frequencies to gain diagnostic information on tissue state and function. Some of these are: detection of hypertension and hyper-hydration of hemodialysis patients [2], pressure ulcer [3], and skin cancer [4].

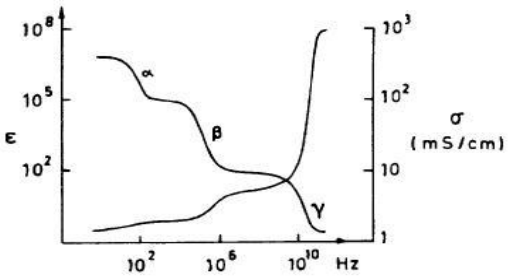

Fig 1. Graphs of the Permittivity (ε) and Conductivity(σ) of Cellular Suspensions versus Frequency [1]

A typical BI system will consist of an AC excitation current source, an IA for voltage

detection, and the corresponding analog blocks that render the magnitude and phase of the impedance.

2 Problem Formulation

The input amplifier stage plays a vital role in the overall performance of a BI system. It must be able to detect and amplify the low amplitude BI signal while cancelling the modulations caused by the front-end interface non-idealities. These include the parasitic impedances of the current injection and voltage detection electrodes, the half cell potential of the electrode-electrolyte interface, and the finite output impedance of the current source. Large common-mode signals can also be coupled into the system like the myoelectric impulses, breathing and beating frequencies, and the 60Hz power line interference. The amplifier must therefore have a sufficiently high CMRR and input impedance to reduce these effects. For this case, an IA is commonly used. A typical voltage-mode IA is shown in Fig. 2.

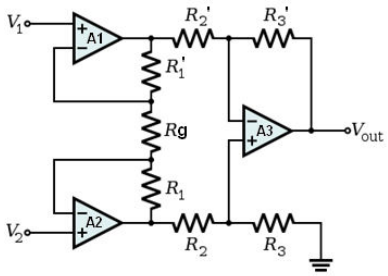

Fig 2. Voltage-Mode Instrumentation Amplifier

This IA is composed of three operational amplifiers "op-amps": A_1, A_2 and A_3. A_1 and A_2 form a differential stage while A_3 forms a simple difference amplifier. A differential voltage between V_1 and V_2 creates a differential current through R_g. This is sensed and amplified by A_3. Any common-mode signal through the two input terminals will yield zero current through R_g and thence a null signal at the output. This however will only be true if the resistors: R_1-R_1', R_2-R_2', R_3-R_3', have a high degree of matching. Such is relatively difficult to achieve and require costly laser trimming technologies. This IA also has a limited gain-bandwidth product which therefore delimits its CMRR on high frequencies [5].

3 Problem Solution

3.1 IA Design and Stages

A different approach has been presented in literature to improve the CMRR that is by using current-mode circuits like the supply current sensors [5,6], Second Generation Current Conveyors (CCII) [5] and the DVCC [7].

In this paper, a complementary DVCC has been used removing the need for pairs of matched CCII and the vulnerability to power supply variations. Furthermore it is different from the DVCC based IA of [7] since the gain stage is separate from the DVCC. Simulations revealed an increase in CMRR by a factor of 3dB. The functional block of the designed IA is shown in Fig. 3.

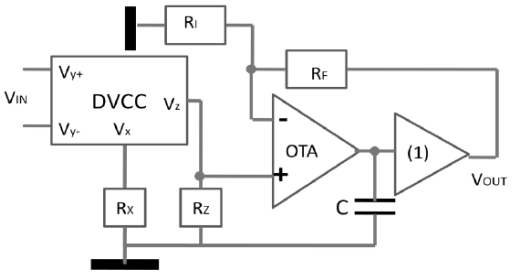

Fig 3. Designed Instrumentation Amplifier

The DVCC provides the common-mode signal rejection and the high input impedance. The CMRR performance of the DVCC depends on its intrinsic X-terminal impedance r_x and does not require stringent resistor matching. This must be minimized so that a higher CMRR may be achieved [5,8]. The DVCC has been configured to have unity voltage gain by setting the on-chip resistors R_x and R_z equal to 5kΩ. The FC-OTA forms a non-inverting amplifier which also provides isolation between the output of the DVCC and the output of the IA. The analog buffer is a simple current mirror load differential amplifier with a DC level shifter stage to extend its ICMR [9]. This is necessary so that the IA will have a relatively wide input linear range even in low voltage operation and sufficient noise margin.

3.1.1 DVCC

The functional block diagram and operational matrix of a DVCC is shown in Fig. 4.

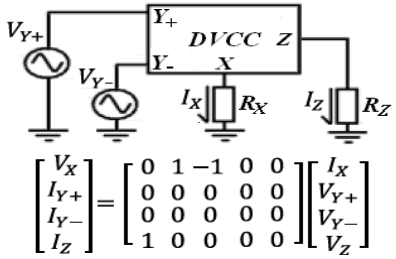

Fig 4. DVCC Functional Block and Operational Matrix

The X-terminal voltage V_X is equal to the differential voltage V_{Y+}-V_{Y-}. This yields a current

I_X through the external resistor R_X which is effectively conveyed onto the Z-terminal as I_Z. The DVCC can be realized by using a differential difference stage as shown in Fig. 5.

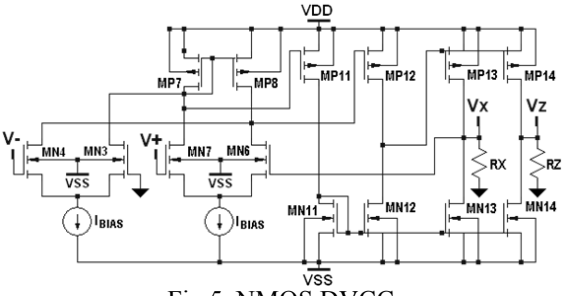

Fig 5. NMOS DVCC

The transistors M_{N3}-M_{N4} and M_{N6}-M_{N7} are differential pairs sharing a common current mirror load formed by M_{P7} and M_{P8}. An additional circuitry composed of M_{N11}-M_{P11} and M_{N12}- M_{P12} cancels the X-terminal offset current that results from the unequal drain voltages of the current mirror load [8]. HSPICE simulations show a decrease in the offset voltage by a factor of 1500. M_{N13}-M_{P13} form a cascode push-pull amplifier that serves as the output drive stage for the X-terminal and correspondingly, M_{N14}-M_{P14} for the Z-terminal. A complementary type of DVCC has been chosen so that r_x may be reduced and that the ICMR may be extended. A simplified functional block of the Complementary DVCC is shown in Fig. 6 [8].

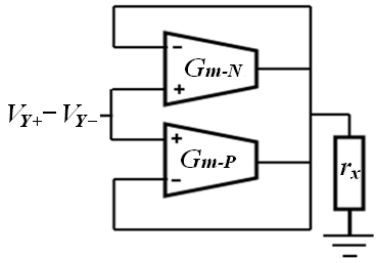

Fig 6. Complementary DVCC Block Diagram [8]

The blocks labeled $G_{m\text{-}N}$ and $G_{m\text{-}P}$ represent the transconductance of each differential difference stage. The transconductance of a stage is

(1)

where g_m is the transistor's transconductance and g_d is its channel's conductance. The value of r_x is

(2)

where g_{dno} and g_{dpo} are the output cascode transistors' channel conductances. HSPICE simulation shows a decrease in r_X by a factor of 1.7 as well as an extension of the ICMR toward the negative voltage by -0.6V for a complementary DVCC.

Some of the pre-layout specifications of the DVCC are 104dB of CMRR, -0.77 to 0.86V of ICMR with a maximum DC offset of 8.53mV, and slew rates of 0.22V/ns (positive) and 0.175V/ns (negative). It dissipates only 0.937mW.

3.1.2 FC-OTA

The gain stage is composed of an FC-OTA. This features a wide output swing and high PSRR - for low voltage operation, a large gain bandwidth product and high slew rate - for high frequency low amplitude BI signals [10,11]. The FC-OTA is shown in Fig. 7.

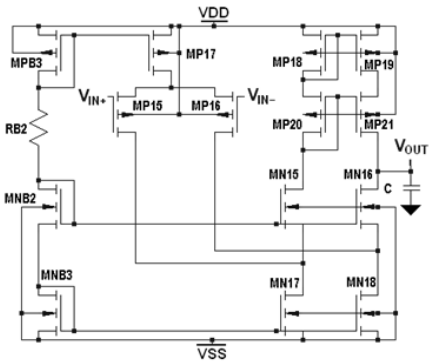

Fig 7. FC-OTA

It is composed of a folded differential pair of PMOS transistors M_{P15}-M_{P16} The transistors M_{P18}-M_{P21} form a cascode current mirror pair which offers a wider output swing as compared to the typical Wilson current source [11]. The transistors $M_{N15} - M_{N18}$ form a cascode current sink.

Some of the pre-layout specifications of the designed FC-OTA are 73.4dB of Gain, 9.22MHz of UGBW with the second pole at 47MHz, 82.3° of Phase Margin (PM), -1.43 to 0.87V of ICMR and an offset voltage of -48.4μV, and slew rates of 5.44V/μs (positive) and -9.26V/μs (negative). It dissipates only 0.179mW

3.1.3 Analog Buffer

An analog buffer has been added to isolate the gain stage from external load. The external load could push the second pole of the FC-OTA at a lower frequency, thereby making the gain non-linear within the UGBW. Furthermore, this may cause the overall PM of the IA to decrease which may result to circuit instability or oscillation. The

high input impedance of the buffer prevents this loading effect on the FC-OTA, while its low output impedance increases the output current driving capacity of the FC-OTA. Such is necessary so that the output voltage does not decrease heavily with load. The circuit of the analog buffer is shown in Fig. 8 [9].

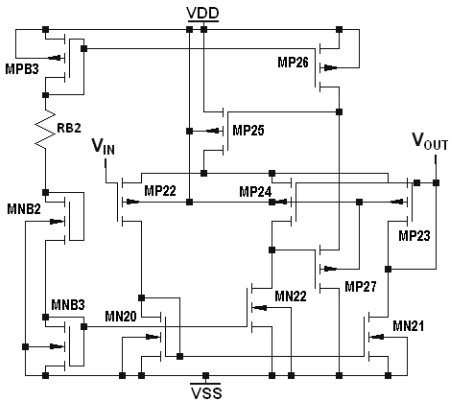

Fig 8. Analog Buffer

It is composed of a PMOS differential amplifier with current mirror load, configured as a non-inverting unity gain amplifier, and a DC level shifter coupled at its local feedback. The differential pair is formed by transistors M_{P22} and M_{P24}, the current mirror load by M_{N20} and M_{N21}, and the bias current source by M_{P25}. The DC level shifter is formed by transistors M_{N22}, M_{P27}, M_{P23} and M_{P26}. The level shifter is used to extend the ICMR of the differential amplifier to provide a sufficient headroom for the maximum output voltage swing of the FC-OTA.

Some of the analog buffer pre-layout specifications are -0.474mdB of gain, 19.6MHz of bandwidth with the second pole of the transfer function at 212MHz, -1.36V to 0.72V of ICMR, -7.67mV of offset voltage, and slew rates of 6.04V/μs (positive) and -145.2V/μs (negative). It dissipates only 0.297mW.

3.2 Instrumentation Amplifier

3.2.1 IA Performance Specification and Layout

The overall IA schematic is shown in Fig. 9. It highlights the different IA stages namely: the DVCC, FC-OTA and Analog Buffer. Table 1 summarizes the performance of the IA resulting from pre-layout and post-layout HSPICE simulations.

Table 1. IA's Performance Specifications

Specification	Pre-Layout	Post-Layout
CMRR [dB]	107	98
DC Open-Loop Voltage Gain [dB]	73.2	67
Phase Margin (*PM*) [deg]	57	59
Unity Gain Bandwidth (*UGBW*) [Hz]	8	7.2
Input Impedance [MΩ] (single-ended mode) @ 1MHz	8.8	4.85
Input Impedance [MΩ] (common-mode) @ 1MHz	2.1	1.4
Input Common-Mode Range (*ICMR*) [V]	-0.77 to 0.7	-0.81 to 0.72
Input Offset Voltage [μV]	49.5	119
Slew Rate [V/μs]	6.9 (+), -9.2 (-)	4.2 (+), -6.5 (-)
Rise (↑) & Fall Times (↓) [μs]	0.47 (↑ & ↓)	0.58 (↑), 0.86 (↓)
PSRR [dB]	71 (+), 83 (-)	76 (+), 83 (-)
Circuit Noise (10kHz – 1MHz) [nV/sqrt(Hz)]	460 to 78	480 to 81
THD (0.1mV – 10mV, 1MHz)[%]	< 1%	< 7%
Power Dissipation (Open Loop) [mW]	1.3	1.27

The IA has achieved sufficient CMRR and input impedance to attenuate the effects of the interface non-idealities. It can also handle a relatively large common-mode input signal as shown by its ICMR. The IA can be used for BI applications operating up to 1MHz of the beta dispersion range as shown by its UGBW, Slew Rate and Rise and Fall Times. It can also provide a sufficient voltage gain without being unstable as shown by its phase margin. The IA dissipates very low power and is not sensitive to supply variations as shown by its high PSRR. This is necessary for circuits biased with low voltage supply rails. Fig. 10 shows the layout of the IA.

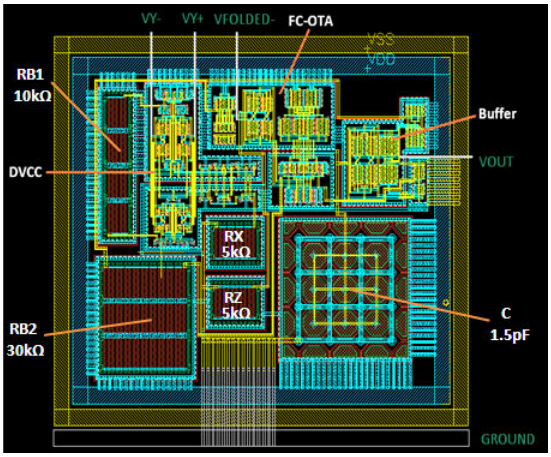

Fig 10. IA Layout

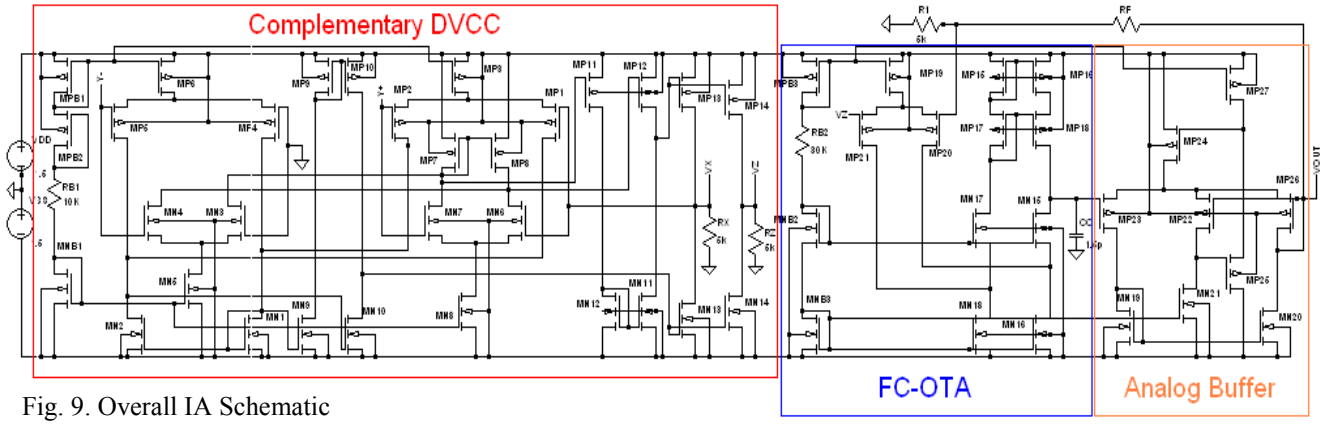

Fig. 9. Overall IA Schematic

Stacked layout and interdigitation patterns are used to layout transistors with similar dimensions. Such create a smaller layout and reduce the overall circuit parasitics: gate resistance and source/drain to bulk capacitances. The differential pairs are layout using common-centroid technique to reduce cross chip gradients. Dummy transistors are used at the lateral ends of each transistor circuit so that the boundary conditions for the inner transistors remain the same. This avoids the tendency for the main transistors to acquire uneven ion diffusions. Each circuit block is enclosed with guard rings to serve as bulk interconnects and stray current protection.

The 1.5pF capacitor has been realized using 9 parallel 0.167pF Poly1 Poly2 (PIP) Capacitors. The use of octagon shaped capacitors reduces the fringing effect and permits even field distribution all throughout the surface of the capacitor. The resistors are built from Poly2 layer with 50Ω/m^2 of sheet resistance. Both capacitors and resistors include dummy devices and are enclosed in guard rings.

3.2.2 IA Transient Simulation

The transient response of the IA has been verified using the front-end interface circuit shown in Fig. 11.

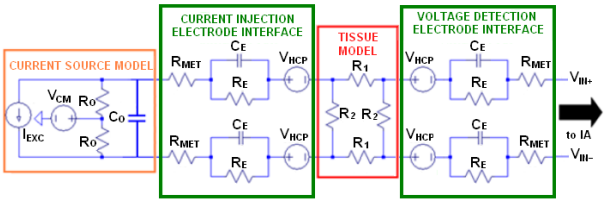

Fig 11. BI Front-End Interface Circuit

It consists of the current source, the electrode-tissue interface and the tissue model. A purely resistive network has been used for the tissue model with R_1=600Ω and R_2=60Ω [13].

The electrode interface model consists of the interconnecting metal wire resistance R_{MET} =100Ω, and the double-layer capacitance C_E =0.1μF and resistance R_E=1MΩ for a platinum type of point contact electrode [12]. The simulated half cell potential V_{HCP} is 50mV. The simulated output impedance of the current source consist of R_O=1MΩ and C_O=10pF in parallel [Boone]. Its amplitude is set to 500μA and its frequency to 1MHz. A noise signal V_{CM} is coupled to the output of the current source. This is simulated as a Piece-Wise Linear (PWL) source whose amplitude is obtained from the randn function of Excel 2007 with intervals of 0.01μs and peak signal of 100mV.

Fig. 12 shows the common-mode signal generated by the simulated interface circuit.

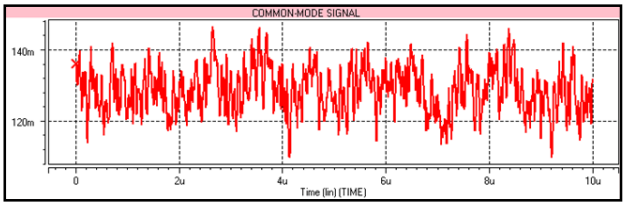

Fig 12. Common-Mode Signal

Fig. 13 shows the differential signal embedded in the large common-mode signal which represents the bio-impedance signal.

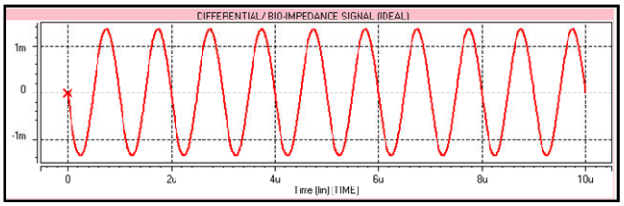

Fig 13. Differential Signal

As can be seen, the common-mode signal has an average of about 130mV with a peak of 10mV. This is about 40dB greater than the level of the

differential signal which is at $1mV_{pk}$. The output of the IA under Typical-Typical (TT) process corner post-layout simulation is shown in Fig 14. Table 2 shows the results of the FFT Analysis which includes the THD, SNR and SFDR for the five process corners under a bipolar supply of 1.5V and 37°C.

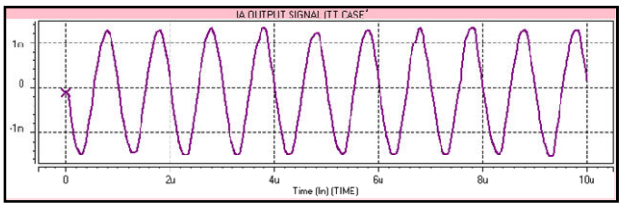

Fig. 14. IA's Output Signal

Table 2. FFT Analysis Results

	THD [%]	*SNR* [dB]	*SFDR* [dB]
TT	2.5996	51.5554	34.5612
FF	2.2030	57.7547	36.3486
SS	2.3521	46.0012	33.4237
SF	2.8231	49.7364	33.0399
FS	2.4592	50.1002	34.6065

The IA in all of the process corners was able to extract the BI signal with sufficient SNR and SFDR and minimal THD even at high frequency operation.

4 Conclusion

A new implementation of a Current-Mode IA was developed. The IA is based on TSMC 0.35µm 2P4M technology composed of the DVCC for common-mode input signal rejection, an FC-OTA for the gain stage and an extended ICMR flipped Analog Buffer for the output drive stage. The results of the pre-layout and post-layout simulations show that the designed IA can be used as a front-end circuit for a β-dispersion frequency (10kHz to 1MHz) BI system. Because of its low power dissipation it can also be used for implantable systems.

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