Negative High Voltage Power Supply (HVPS) For Laser Beam Printer Applications

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Abstract: A novel negative high voltage power supply that features the high input to output step-up voltage conversion ratio characteristics is presented. The proposed circuit features the reduced voltage stresses of the components compared to those of the conventional ones. The operational principles of the proposed circuit are analysed and comparative features are presented. The simulation results and experimental results are presented to verify the validity of the proposed circuit.

Key-Words: Polarity Inversion, High Voltage Power Supply, Voltage Multiplier,DC-DC Power Converter

1 Introduction

The High voltage power supply (HVPS) has recently expanded its applications to a variety of industries, and it became an essential part in many areas. Since the applications of HVPS has become so prevalent, they can be found in many different sectors including new composition development and plasma application for industrial, domestic, medical and military uses as well as printers. Printers, which are now a part of everyday life at work and even at home, has adapted high voltage power supply for the Laser Beam Printer (LBP) image processing system.

Fig. 1 shows the conventional polarity inversion DC-DC converter for a HVPS used in the printer application. The conventional circuit, composed of single semiconductor switch, single high-voltage transformer, several diodes and several capacitors, is the well-known flyback converter which employs a voltage multiplier circuit. By incorporating voltage multiplier circuit, the diodes and capacitors with a low stress voltage can be chosen even with a high output voltage above a few KV. Because of its simple structure, it has been widely used for HVPS with a low power capacity in Watt such as printer application. It is noted that in such a printer application, a high negative output voltage with respect to the earth-ground,and the output voltage (-V_o) should be tied to meet the safety requirement.

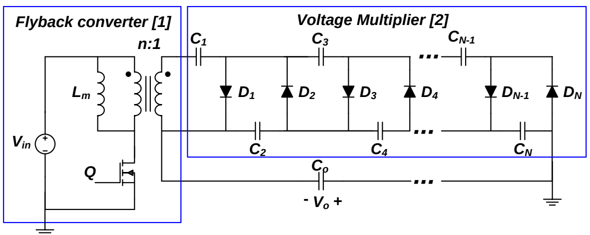

Fig.1, Polarity Inversion DC-DC converter for conventional high voltage power supply

However, the use of the high-voltage transformer in the conventional circuit requires an increased size of magnetic component, since, there should be an enough spacing between the primary windings and the secondary windings, to prevent a voltage-arch due to high output voltage above one kV. Therefore, it results in a large-window-area transformer. Also, the energy stored in the leakage inductance of the transformer is dissipated in the circuit, which results in a low power conversion efficiency. The high voltage stresses of the diodes and capacitorsin the voltage multiplier results in the high-price components. These features have been a major obstacle in minimizing the size and weight of the HVPS and in reducing the cost of whole product [1]-[3].

In this paper, a novel polarity inversion dc-dc power conversion circuit features the reduced voltage stresses of the components and the increased input-output step-up voltage conversion ratio characteristics compared to the conventional one. Instead of using a transformer, the proposed circuit utilizes magnetic components as an inductor. This results in reducing the size of magnetic components while maximizing the efficiency of power conversion. Analysis and the operational principles of the proposed circuit have been done to demonstrate the advantages of the proposed circuit. Simulation and experiment has been performed to verify the validity of the proposed circuit.

2 Operational Principles

The circuit diagram of the proposed two-level polarity inversion circuit is shown in Fig. 2. The proposed circuit is similar to the conventional polarity inversion circuit in that both of them are composed of Switch *Q*, Inductor L_m, Diode $D_O$and Capacitor C_O, while it has an additional voltage multi-cell, consisting of Diodes D_1 and D_2 and Capacitors C_1 and C_2, to reduce the component voltage stresses. To analyze the operation of the proposed circuit, the following assumptions have been made.

•All power semiconductors are ideal.

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•The circuit operates in a steady state.
•The Capacitor C_1, C_2, and $C_O$are assumed to be large enough so that the voltage across the capacitors are approximated by a DC voltage of the source.
•The voltages across the Capacitor C_1 and C_2 have a value equal to V_X.
•$V_{in} < V_x < V_o$
The last two assumptions become evident from the circuit behavior that is described below in detail.

2.1Continuous-Conduction-Mode Operations

Fig. 3 shows two topological states of the equivalent circuit when the inductor current of the proposed circuit operates in CCM. Key waveforms of the voltage/current for the proposed circuit are illustrated in Fig. 4. The detailed description of each topological state is given in the next.

2.1.1 Mode 1[T_0~ T_1]

Mode 1 begins as switch Q is turned off at T_0. The Diode D_1 and the output diode D_O are forward-biased, and the energy stored in the magnetizing inductance is discharged via paths $L_m - V_{in} - C_1 - D_1$ and $L_m - C_O - D_O - C_2$. Therefore, the current $i_{Lm}(t)$ flowing through Inductor L_m is expressed as follows.

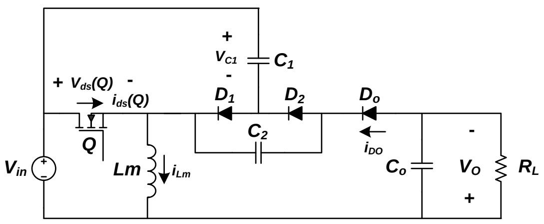
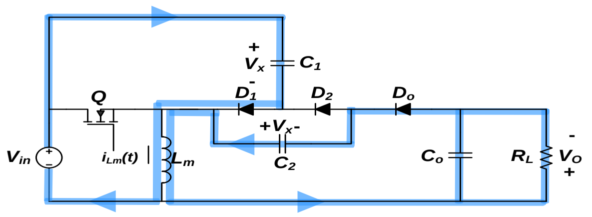
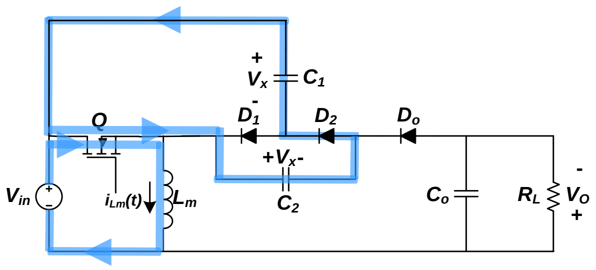


Fig.2, The proposed Polarity Inversion DC-DC converter ofTwo-Level



a) Mode 1: Switch Q off



b)Mode 2: Switch Q on

Fig.3,Equivalent Circuit of CCM

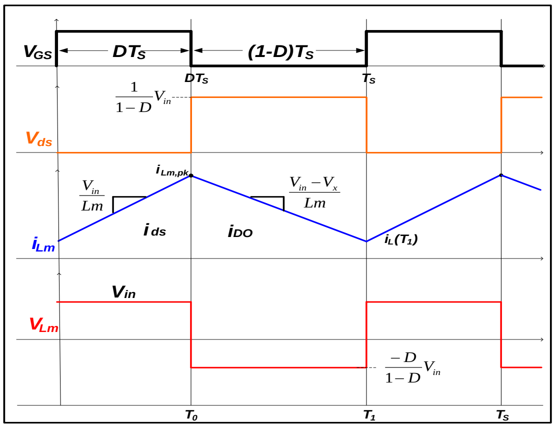


Fig.4,Steady-state waveforms of CCM

$$i_{Lm}(t) = i_{Lm}(T_0) + \frac{V_{in} - V_x}{L}(t - T_0) = i_{Lm}(T_0) + \frac{V_x - V_o}{L}(t - T_0) \quad (1)$$

At T_1, the current $i_{Lm}(T_1)$ can be written as follows.

$$i_{Lm}(T_1) = i_{Lm}(T_0) + \frac{V_x - V_o}{L}(1 - D)T_s \quad (2)$$

where$D$ is a duty ratio of the switch Q and T_S denotes a switching period. During Mode 1, the reverse voltage of the diode D_2, V_{D2}, and the Drain-to-Source voltage of the switch Q, $V_{DS}(Q)$, become V_X.

2.1.2 Mode 2 [T_1 ~ T_2]

At T_1, as the switch Q is turned on, the diodes D_1 and D_O are turned off. Since, during Mode1, capacitor C_1 is charged and C_2 is discharged, which results in forward-biased of the diode D_2 at T_2. Energy is stored in the magnetizing inductance via the path $V_{in} - Q - L_m$. Therefore, the Inductor Current $i_{Lm}(t)$ is expressed as

$$i_{Lm}(t) = i_{Lm}(T_1) + \frac{V_{in}}{L_m}(t - T_1) \quad (3)$$

At T_2, the current $i_{Lm}(T_2)$ can be written as

$$i_{Lm}(T_2) = i_{Lm}(T_1) + \frac{V_{in}}{L_m}DT_s = i_{Lm}(T_0) \quad (4)$$

During Mode 2, the path $C_1 - Q - C_2 - D_2$ is established, and thus the output voltages V_{C1} and V_{C2} across the capacitors C_1 and C_2 are equal to V_X. Therefore, it is obvious that the reverse voltage of the diode D_1, V_{D1}, and the reverse voltage of the output diode D_O, V_{DO} are equal to V_X and V_{in}+V_O-V_X , respectively. Mode 2 ends when the switch Q becomes turn-off at T_2, Mode 1 starts again and the cycle repeats.From the equations (2) and (3), the voltage across the capacitors $C_1$and C_2, V_X, and the ratio of the input voltage to the output voltage, V_O/V_{in} , are given by:

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$$V_x = \frac{V_{in}}{1-D} \quad (5)$$

$$\frac{V_o}{V_{in}} = \frac{1+D}{1-D} \quad (6)$$

It should be noted that $V_{in}<V_X<V_O$ is always true, since the duty ratio D has a value between 0 and 1.

2.2 DCM Operations

The input tooutput voltage ratio *Vns* $_O/V_{in}$ of the proposed circuit operating in DCM is given by

$$\frac{V_o}{V_{in}} = \frac{1+\sqrt{1+\frac{4D^2}{K}}}{2} \quad (15)$$

where, $K = L_m/(R_L T_S)$. Equation (15) shows that high output voltage gain is obtained by L_m, R_L, T_S.

2.3 N-Level Polarity Inversion DC-DC converter

Fig. 5 illustrates the proposed DC-DC converter with N-level polarity inversion. The circuit basically expands the concept of the two-level polarity inversion circuit, and, reduction in the component stress increases as the number of level increases. When the switch Q is turned on, the N-level DC-DC converter stores energy in the inductor L_m, and diodes D_{12}, D_{22}, …,$D_{(N-1)2}$, D_{N2} are turned on, which leads to the voltage balance among the capacitors. When the switch Q is turned off, the output diode D_O and diodes D_{11}, D_{21}, …,$D_{(N-1)1}$, $D_{N1}$are turned on, and thus the energy stored in the inductor is supplied to the output load. The following equations can be obtained by applying the same process of analysis employed for the operational principles of the proposed DC-DC converter with two-level polarity inversion.In CCM operation, the input to output voltage ratio is given by

$$\left.\frac{V_o}{V_{in}}\right|_{CCM} = \frac{N-1}{1-D} + \frac{D}{1-D} \quad (16)$$

In DCM operation, the input to output voltage ratio is given by

$$\left.\frac{V_o}{V_{in}}\right|_{DCM} = \frac{N-1+\sqrt{(N-1)^2+4D^2/K}}{2} \quad (17)$$

where $K = L_m/(R_L T_S)$

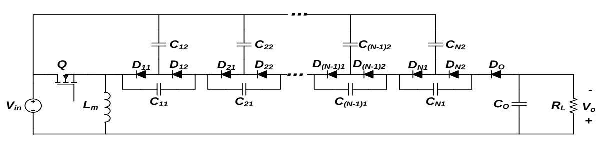
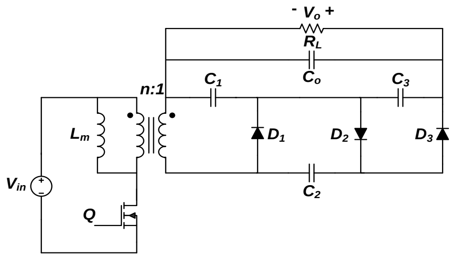
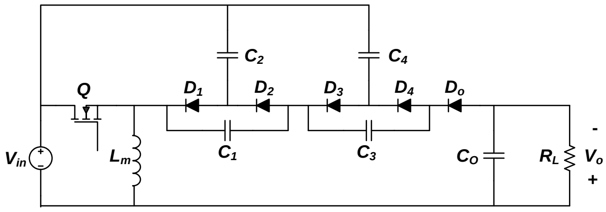


Fig.5, Polarity Inversion DC-DC converter of N-Level



a) The flyback converter using triple voltage Multipliers



b) Polarity Inversion DC-DC converter of 3-Level

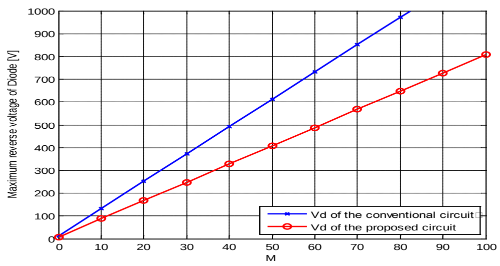
Fig.6,Comparison of the circuits

3. Comparison to the Conventional Circuits

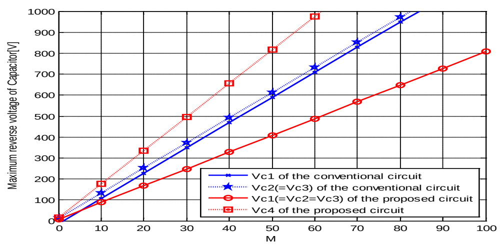
3.1. Polarity inversion DC-DC converter with 3-Level VS. Flyback converter using triple voltage multipliers

Compared to the conventional circuit with a voltage multiplier, the proposed polarity inversion DC-DC converter features the low voltage stresses of the components, which save the cost and volume. To prove the hypothesis, we compared the proposed DC-DC converter with 3-level polarity inversion and the flyback converter with triple voltage multiplier.

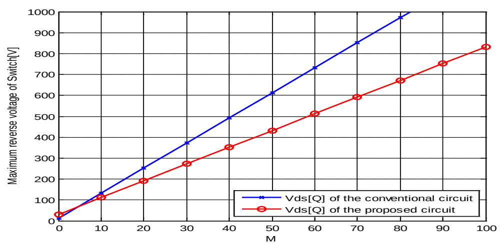
Fig. 6(a) demonstrates the flyback converter using triple voltage multiplier, where the transformer turns ratio is assumed to be 1. The conventional circuit contains four less diodes compared to the proposed circuit shown in Fig.6(b). Although the proposed circuit consists of a greater number of components, the cost of the power converter can be actually reduced since the voltage stresses of the proposed circuit are lower than those of the conventional one. Table 1 shows the voltage stresses comparison of the components for each circuit. As can be seen, the duty ratio of the proposed circuitis smaller than that of the conventional one under the same input-output voltage condition. In consequence, the voltage stresses for all components in the proposed circuit, except the capacitor C_4, remains low.The component stresses of the conventional circuit compared to the proposal circuit versus the input-output voltage conversion ratio M, is shown in Fig. 7. The voltage stresses of all elements except C_4 decreases in the proposed circuit as M increases. Thus, the proposed circuit is well suited in the high step-up voltage conversion application such as HVPS in LBP.



(a) Maximum reverse vtg. of diode



(b) Maximum reverse vtg. of Capacitor



(c) Maximum reverse vtg. Of Switch

Fig. 7,The proposed Polarity Inversion DC-DC converter ofTwo-Level

It is noted that if the turns ratio of transformer in the conventional circuit is set to n, larger than one, the maximum reverse voltage of diode(D_1, D_2, D_3) and the voltage of capacitor(C_1,C_2,C_3) will increase more. Even when considering turns ratio of the transformer, it is expected that the proposed circuit is superior to the conventional one.

3.2 Design Considerations and Design example

For comparison, the specifications used in a typical HVPS in LBP are listed as follows :

- Input voltage V_{DC} : 24V$_{\mathrm{DC}}$
- Output voltage V_O : -1200V$_{\mathrm{DC}}$
- Output power P_O : 15W
- Switching frequency f_S : 50 kHz
- Inductor current operation mode : CCM

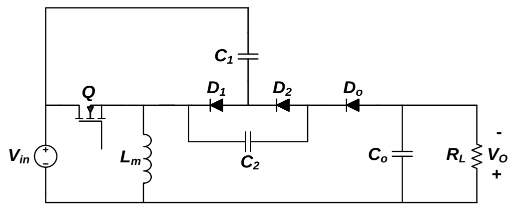
Duty ratio **:**The required input output voltage ratio (V_O/V_{in}) is 50. As shown in Table 1, the duty ratio D of the proposed DC-DC converter is 0.9410, while the duty ratio D* of the flyback converter using triple voltage multipliers is 0.9607.

Switch **:**The maximum drain-to-source voltage of the switch $V_{DS}(Q)$ is 432V, and that of the conventional circuit $V_{DS}*(Q)$ is 612V.

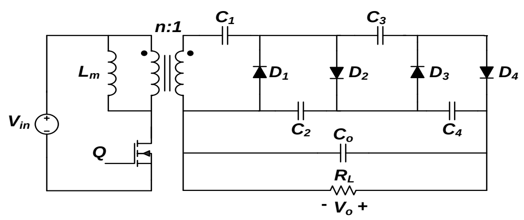
Diode **:**Diodes should be selected to have the standard capacity greater than the maximum reverse voltage. The maximum reverse voltages of all diodes are 408V for the proposed circuit, while those are 612V for the flyback converter using triple voltage multiplier (Table 1).

Capacitor **:**Capacitors should have a greater capacity than the maximum stress voltage, considering the de-rating factor. As shown in Table 1, the maximum capacitor voltages of C_1, C_2 and C_3 are the same values of 408V, and that of C_4 is 816V, in the proposed circuit.On the other hand, in the conventional circuit, the voltages across C_1, C_2 and C_3 are 588V, 612V and 612V, respectively.

In this design example, it seems that the proposed circuit successfully reduces the voltage stress for its components by at least 30%, compared to the conventional one. Therefore, the proposed circuit has an advantage in design which enables the use of low-cost and low-rating components, resulting in a significant cost reduction in the production of high voltage power supply.



(a)Polarity Inversion DC-DC converter of 2-Level



(b) The flyback converter using quadruple voltage Multipliers

Fig. 8,Comparison of the circuits

3..3 Polarity Inversion DC-DC converter with 2-Level VS. Flyback converter using quadruple voltage multipliers

Even if the proposed converter is designed with the same voltage stresses of the components as those used in the conventional converter, the effect of the cost reduction can still be achieved since the number of the components is reduced compared to the conventional one in designing the HVPS. Under the specifications in the previous design example, we also compared the proposed

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circuit with two-level polarity inversion and the flyback converter with quadruple voltage multipliers. The proposed and flyback converters are shown in Fig. 10.

Table 1: Comparison of the component stresses and size

Item	Conventional circuit	Proposed circuit
n	$n=\frac{\text{turns of primary side}}{\text{turns of secondary side}}$	-
M	$M=\frac{1}{n}\cdot\frac{1+D^*}{1-D^*}$	$M=\frac{2+D}{1-D}$
D	$D^*=\frac{nM-1}{nM+1}$	$D=\frac{M-2}{M+1}$
Diode Max. reverse Vtg.	$V_{D1}=V_{D2}$ $=V_{D3}=\frac{1}{n}\cdot\frac{V_{in}}{1-D^*}$	$V_{D1}=V_{D2}=V_{D3}$ $=V_{D4}=V_{Do}=\frac{V_{in}}{1-D}$
Capacitor Vtg.	$V_{C1}=\frac{1}{n}\cdot\frac{D^*}{1-D^*}V_{in}$ $V_{C2}=V_{C3}=\frac{1}{n}\cdot\frac{1}{1-D^*}V_{in}$	$V_{C1}=V_{C2}=V_{C3}=\frac{V_{in}}{1-D}$ $V_{C4}=\frac{2V_{in}}{1-D}$
Switch Q Max. Vtg.	$V_{ds}=V_{in}+\frac{D^*}{1-D^*}V_{in}$	$V_{ds}=V_{in}+\frac{1}{1-D}V_{in}$
Core size of magnetic components (Volume)	EE2525S ($2760\ mm^2$)	EE2519S ($1940\ mm^2$)

n : transformer turns ratio
M : input-output voltage rati0
D : Proposed circuit Duty ratio
$D*$: Conventional circuit Duty ratio

Duty ratio: The duty ratio is 0.9608 for the proposed DC-DC converter with two-level polarity inversion, and 0.9600 for the conventional flyback converter.

Switch:The maximum drain to source voltage $V_{DS}*(Q)$ and the maximum current $I_{DS,pk}$ of the switch are 636V and 1.275A, in the proposed circuit, while those are 612V and 1.29A, in the conventional circuit, respectively. When considering the reliability, the maximum drain-to-source voltage and the maximum current of the switch should be chosen to have greater values than 700V and 1.5A, respectively, for both circuits. In other words, the same power switch component can be selected for both circuits.

Diode :The maximum reverse voltages of each diode for the proposed circuit are 612V, and those are 612V for the conventional circuit. Thus, the same diode component can be selected for both circuits.

Magnetic components :Instead of using a transformer, the proposed circuit utilizes magnetic components as an inductor. This results in reducing the size of magnetic components. As shown in Table 1, the proposed converter can reduce approximately 30% in magnetic components.

Capacitor : The voltages across the capacitors for the proposed circuit, C_1 and C_2 are all 612V. The voltages C_1, C_2, C_3 and C_4 composing the conventional circuit are 588V, 612V, 612V and 612V, respectively. Except for C_1 of the conventional circuit, the capacitors which have the maximum voltage greater than 700V, should be used for both circuit.

When both converters are compared for their component voltage stresses following the specifications of the design example described above, the similar components should be used. This example clearly demonstrates that the proposed circuit can be built using one less diode and on less capacitor compared to the conventional circuit, resulting in the cost reduction.

4. Experimental Results

The performance of the proposed converter is verified by PSIM simulation and experimental results. The specifications of the circuit are the same as the previous design example. The proposed converter with 3-Level polarity inversion is implemented with the conditions that the inductance Lm is 531uH and the capacitances C_1~C_4, including C_O are the same value of 33nF.

Fig. 9 shows the simulation results for the proposed circuit with 3-Level. When a 3-level polarity inversion DC-DC converter was designed targeting the output voltage of –1200V, the simulation result showed the output voltage of –1185V. The difference between the target and simulation output voltages was approximately 15V, falling within the 5% error range of the simulation. The magnetic inductance current of the proposed Polarity Inversion DC-DC converter with 3-Level is operated in CCM. The maximum peak current is 1.1A, and the minimum current is 0.2A. The drain-source voltage switch measured is 411V. Inductor voltage is measured 24V at the switch ON time. Inductor voltage is measured -383V at the switch OFF time. Simulation results show that all the values and calculated values are within the range of 5% error of the match.

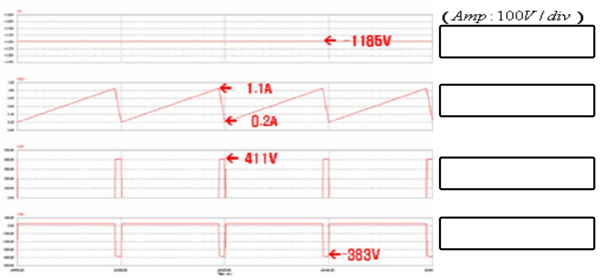


Fig. 9,Simulated Waveforms of the proposed circuit (3-Level circuit)

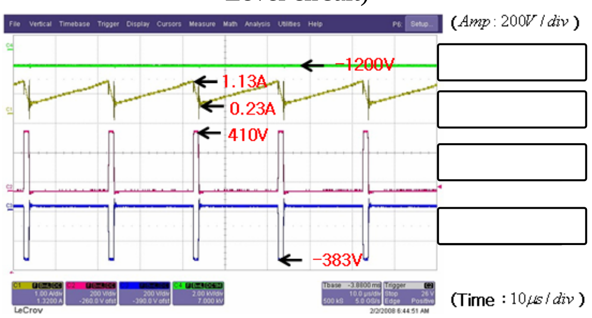
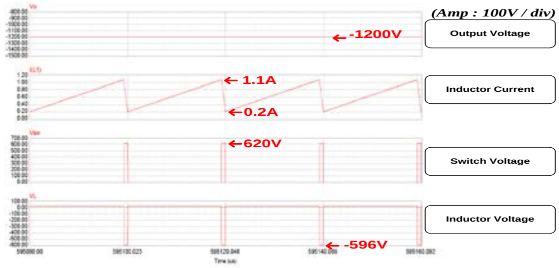


Fig. 10,Measured waveforms of the proposed circuit(3-Level circuit)



Fig,11,Simulated Waveforms of the proposed circuit(2-Level circuit)

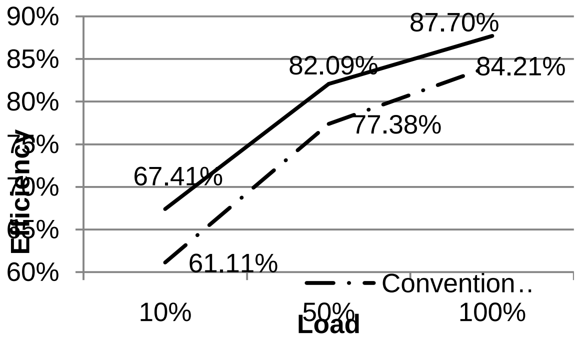


Fig. 12, Comparison of the measured efficiency between the proposed and conventional converters

Fig. 10 shows the experimental results for the proposed Polarity Inversion DC-DC converter of 3-Level. The experimental parameters are equal to the simulation parameters. The experimental waveforms of the output voltage of the converter are given in Fig. 7, which is in good agreement with the theoretical estimation. The magnetic inductance current of the proposed Polarity Inversion DC-DC converter with 3-Level is operated in CCM. The maximum current is 1.13A, and minimum current is 0.23A. The results are within the margin of error in matching the simulation results. The drain-source voltage of the switch is 410V. And Inductor voltage is 24V at switch ON time, -383V at switch OFF time. Simulation results of the experiment resulting value is a calculated value of all the values match within the margin of error 5%.Fig. 11 shows the simulation results for the proposed circuit with 2-Level. The results are good agreement with the analysis.Fig. 12 shows the comparison of the measured efficiency between the conventional converter and proposed converters. As shown in this figure, the proposed converter can achieve higher efficiency along wide load ranges (10–100%), and its efficiency at the full-load condition (16W) is as high as 87.7%.

5 Conclusion

A novel polarity inversion dc-dc power conversion circuit that has the high input-output voltage conversion ration characteristics is presented for high voltage DC power supply applications. The proposed circuit features the reduced voltage stresses of the component compared to those of the conventional ones. The operational principles of the proposed circuit are analyzed and comparative features are presented. The simple formulas and choosing the parameters of the converter elements are given. The features of this converter include high efficiency, low voltage stress on the switching elements. The computer simulation and experimental results have verified the predictions of the theoretical analysis

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