A band-tunable Auto-Zeroing Amplifier

MEHDI AZADMEHR
Vestfold University College
Department of Technology
Raveien 197, 3184, Horten
NORWAY
mehdi.azadmehr@hive.no

YNGVAR BERG
Vestfold University College
Department of Technology
Raveien 197, 3184, Horten
NORWAY
yngvar.berg@hive.no

Abstract: In this paper we present a tunable Auto-Zeroing Amplifier(AZA). The amplifier is based on Pseudo Floating gate and in addition to gain, it offers frequency band adjustment. Both the low- and high-frequency cutoffs are controlled electronically using bias voltages, thus the amplifier can be used in design of various time continues filters. The peak gain of the AZA is 22dB dB at 100 MHz and has a bandwidth from. The AZA enjoys low component spread and compactness, containing only small size transistors and capacitors suited for integration. We will also show a second order section realized using the AZA. The simulations presented in this paper are valid for the 90nm CMOS transistor models from STM having a VDD equal to 1.2V and threshold voltage of 0.25V.

Key–Words: Analog, Filter, Amplifier, Floating Gate, Tunable, LaTeX

1 Introduction

As the demand for higher integration and lower power consumption in circuits and systems increases, the need for alternative design approaches become more evident. One important area is within the radio communication where multiband communication is an emerging trend [1, 2]. In order to cover the various bands, multiple-band time-continues filtering in the system is needed. Electrically tunable analog filters offer a good solution to these problems as they can be tuned so they cover the various bands. There exist different methods for designing tunable filters. Most popular are the transconductance, capacitor (gm-C) filters[3, 4], Switched capacitor SC [5, 6], varactor tunable filters [7, 8] and active-inductor filters[9]. Also transconductance tunable filters based on floating-gate are emerging [10, 11, 12, 13]. These filters, offer more tunability as it is possible to control both the lowest and the highest cutoff-frequencies at the same time. Another important advantage of floating gate is the capacitive input that limits the gate-leakage [14] due to thinner gate oxide in newer technologies. This becomes even more important as the gate-oxide becomes thinner as a result of downscaling. The amplifier presented in this paper is based on a pseudo-floating gate. In pseudo-floating gate the floating gate are biased weakly, avoiding the need for programming of the floating gate.

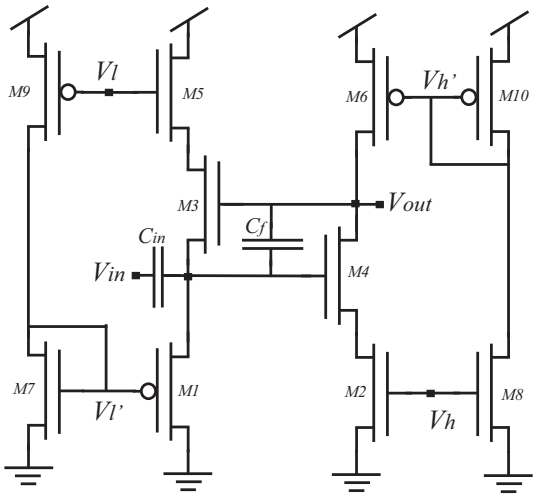

Figure 1: *Schematic of the band pass autozeroing floating-gate amplifier. The bias voltages Vl and Vh are used to control the current through their respective branches.*

2 The AutoZeroing Amplifier

The AutoZeroing Amplifier (AZA) is shown in figure 1. The amplifier is a common-source amplifier with an active-load $M6$ and the source follower $M4$. $M2$ is added to the amplifier to make the circuit more stable regarding the DC output variations when changing the bias Vh. The output of the amplifier is connected to the gate of $M3$ that is series connected to $M1$ and

ISBN: 978-1-61804-131-9

$M5$. $M1$, $M3$ and $M5$ form a non-inverting buffer. The output of the non-inverting buffer is connected to the input of the amplifier and forms a loop. Since the input of the amplifier is made floating using the input capacitor C_{in}, this loop will zero the output when no signal is applied to the input, an equilibrium state that allows it to be used as an amplifier in analog applications. Variation of Vh, results also in variations in the DC output voltage. Figure 2 shows the DC output voltage of the amplifier as a function of the bias voltages Vl when the bias voltages Vh is swept from $0.35V$ to $0.85V$. From the figure we see that the DC output voltage of the circuit is susceptible to the variation in Vh, but variations in Vl.

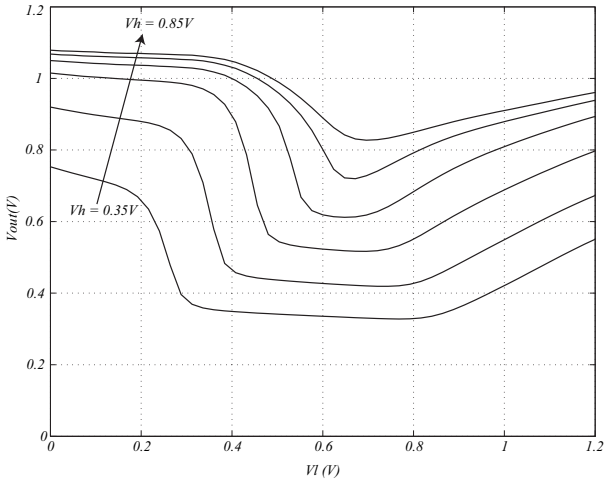

Figure 2: *The DC output voltage of the AZA as a function of the bias voltage Vl when different bias voltages Vh from 0V to VDD = 1.2V is applied.*

The ratio between the input capacitor C_{in} and the feedback capacitor C_f sets the gain of the amplifier and is given by:

$$A \approx -\frac{C_{in}}{C_f} \tag{1}$$

The current through the amplifier and the feedback circuitry is controlled by the bias voltages Vh, Vh' and Vf, Vf' respectively. In order to control each pair of bias voltages simultaneous, we use a current mirror to mirror the current from Vh to Vh' and Vl to Vl'.

2.1 AC properties

The frequency response of Autozeroing amplifier for various bias voltages at Vl is shown in figure 3. Variations in bias voltage Vl results in variations in the

$Transistor$	M1	M2	M3	M4	M5
$Width(nm)$	450	300	120	120	450

Table 1: Transistor sizes of the amplifier shown in figure 1

current through the non-inverting buffer($M1$, $M3$ and $M5$) that again controls the lowest cut-off frequencies of the amplifier. In this simulation $Vh = 0.6V$ that results in a DC level of around $VDD/2$.

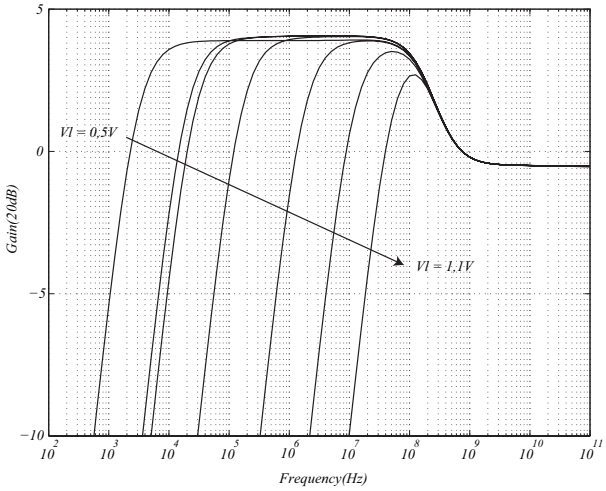

Figure 3: *Figure above shows that the lowest cut-off frequency can be controlled using the bias voltage Vl. Vh is 0.6 V*

Figure 4 shows the frequency response of the AZA when Vh is swept from $0.30V$ to $0.7V$ with a step of $0.05V$. In this figure we see that the highest cut-off is changing due to variations in Vh. Due to the feedback in the circuit, variations in Vh, results in variations in gate voltage of transistor $M3$ the lowest cut-off frequency of the AZA. This effect is shown in figure 4 as variations in the lowest cutoff even when Vl is constant and is 0.6V.

The highest cut-off frequency of the AZA can be obtained using simple transistor models and assuming that the starving transistor operates in the linear region:

$$f_{max} \approx \frac{\beta_{M2} V_{hf_{effective}}^2}{2C_l VDD} \tag{2}$$

where $V_{hf_{effective}}$ is $V_{hf} - Vt$ and $M2$ is the starving transistor, see fig 1. If Cin and Cf are equal, the transfer function of the circuit can be obtained by:

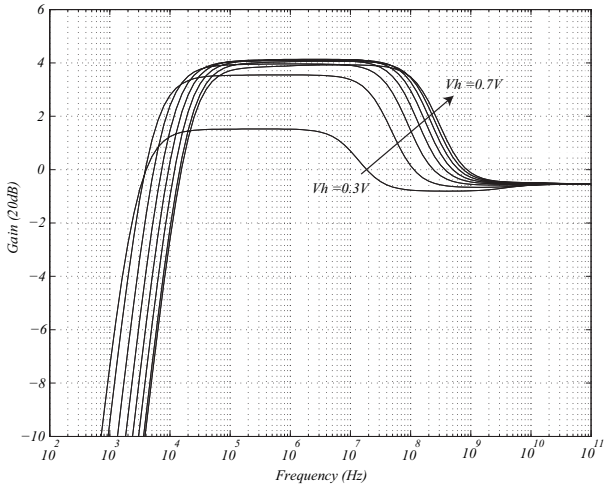

Figure 4: *The frequency response of the AZA shown in figure 1) when various bias voltages Vh from 0.35V to 1.05V is applied. Vl is 0.6 Volts.*

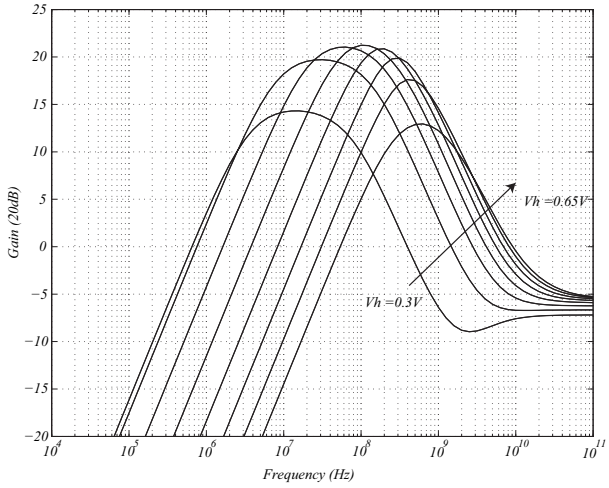

Figure 5: *The frequency response of the AZA used as a bandpass filter) when Vl is 0.3 Volts and various bias voltages Vh from 0.35V to 1.05 V applied.*

$$\frac{V_{out}}{\frac{1}{SC_l}} = -gm(V_{in} + V_{out})$$

$$\frac{SC_l V_{out}}{g_m} = -V_{in} - V_{out}$$

$$\tau = \frac{C_l}{g_m} => S\tau V_{out} = -V_{in} - V_{out}$$

$$H(S)_{lp} = \frac{V_{out}}{V_{in}} = \frac{-1}{1+\tau S} \qquad (3)$$

2.2 Band pass filter

Since the lowest and the highest cut-off frequencies can be controlled independently, the AZA can be tuned to operate as a bandpass filter. Figure 5 shows the frequency response of the AZA when tuned so that the lowest and highest cut-off frequencies are close. In this simulation, Vl is 1.1 Volts and Vh is swept from $0.3V$ to $0.65V$. Since variation in Vh, controls the lowest cutoff frequency in addition the highest, The AZFA can be used as a band-pass filter where its center frequency is controlled using only the Vh and the bandwidth using Vl. In figure 5, the band pass filter has a tuning range from $15MHz$ to $800MHz$. Frequencies above and blow this values, results in large attenuation in gain.

3 Gain and linearity

The AZA When operated as class an amplifiers, the main drawback of these amplifiers are the fact that all the transistors are on, resulting in continuous power consumption, but a smoother transition across the DC level. Figure 6 shows the sine response of the AZFA as a function of different bias voltages Vh. From the figure we can see that the circuit experiences small delay as the bias voltage Vh decreases. In this simulation the bias voltage Vl is $600mV$. The input signal is marked with a dashed line and has an amplitude of $300mV$ and a frequency of $10MHz$.

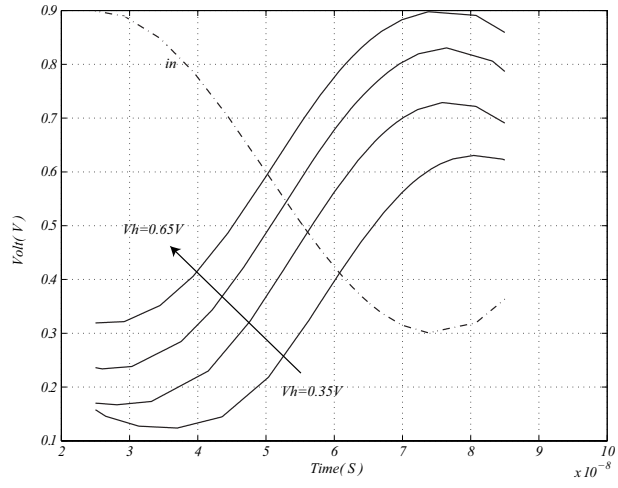

Figure 6: *The sine response of the amplifier shown in figure 1a) as a function of different bias voltages Vh when Vl = 0.6 V.*

Figure 7 is the gain of the AZA. From this figure we can see that the gain is smallest when the bias

voltage $Vh = 400mV$ and the linearity increases as the Vh increases. The linearity within 3% deviation is marked with circles on the figure. These simulations are done with minimum length transistors and an increase in transistor lengths results in increased linearity and gain. An increase in length also effect the frequency response and decreasing the pass band when used as band pass filter.

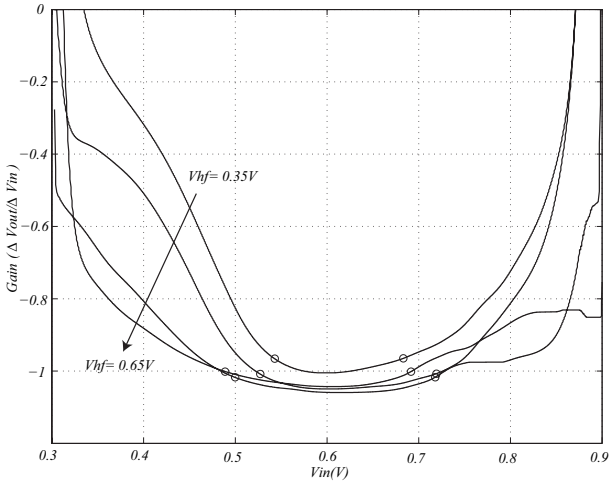

Figure 7: *The gain of the Amplifier shown in figure 1 as a function of different bias voltages Vh when Vl = 0.6 V. The area with linearity within 3% is marked with circles*

4 The second order section

Second order sections are important components for designing high quality filters. We have realized a second order section as shown in fig. 8, this circuit is based on the design from R.F Lyon [15] and made of three amplifiers.

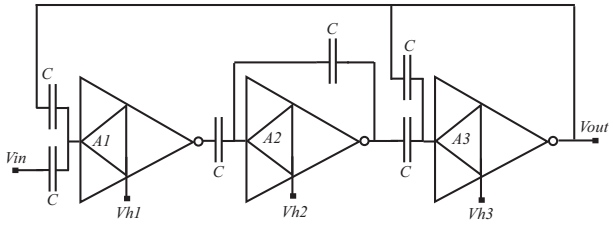

Figure 8: *The second order section realized using 3 AZAs as shown in figure 1.*

The frequency response of the amplifier is shown in figure 9 where $Vh1$ is varied from $425mV$ to $550mV$. By doing this we are able to control the quality factor Q of the Second order section. This SOS has 40dB/dec attenuation at it cut-off.

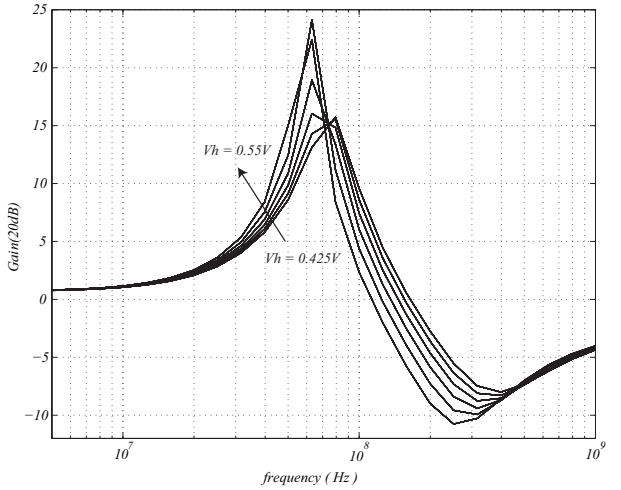

Figure 9: *The AC response of the Second order section shown in figure 8. when various bias voltages Vhf1 is applied*

5 Conclusion

The auto zeroing amplifier presented in this paper has good properties regarding linearity and frequency band adjustment and has a more stable DC value than the presented earlier. The stability of the DC level, allows the circuit to be more tunable at its highest cut-off frequencies. The circuit enjoys low component spread and is very compact. The AZFA can be used for designing filters at the same time as it offers a limited voltage gain. We have also presented a second order section

References:

[1] Hussaini, A.S.; Abd-Alhameed, R.; Rodriguez, J.; , "Tunable RF filters: Survey and beyond," Electronics, Circuits and Systems (ICECS), 2011 18th IEEE International Conference on , vol., no., pp.512-515, 11-14 Dec. 2011

[2] Rofougaran, A.R.; Rofougaran, M.; Behzad, A.; , "Radios for next generation wireless networks," Radio and Wireless Conference, 2004 IEEE , vol., no., pp. 1- 4, 19-22 Sept. 2004

ISBN: 978-1-61804-131-9

[3] R. R. Harrison, I. A. Bragg, P. Hasler, B. A. Minch and S. P. Deweenh *"A CMOS Programmable Analog Memory-Cell Array Using Floating-Gate Circuits"*, In IEEE Transactions on Circuits and Systems-II: Analog and digital signal processing, vol. 48, no. 1. pp 4-11. jmuoT 2001.

[4] Sanchez-Rodriguez, T.; Lujan-Martinez, C.I.; Carvajal, R.G.; Ramirez-Angulo, J.; Lopez-Martin, A.; , "A CMOS linear tunable transconductor for continuous-time tunable Gm-C filters," Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on , vol., no., pp.912-915, 18-21 May 2008

[5] Voorman, H.; Veenstra, H.; , "Tunable high-frequency Gm-C filters," Solid-State Circuits, IEEE Journal of , vol.35, no.8, pp.1097-1108, Aug 2000

[6] Saeedi, S.; Heidari, T.; Hafezi, M.H.; Baabuei, J.M.; , "Design, simulation and fabrication of a varactor tunable combline microwave filter," Microwave Conference Proceedings, 2005. APMC 2005. Asia-Pacific Conference Proceedings , vol.1, no., pp. 3 pp., 4-7 Dec. 2005

[7] Chatterjee, S.; Musah, T.; Tsividis, Y.; Kinget, P.; , "Weak inversion MOS varactors for 0.5 V analog integrated filters," VLSI Circuits, 2005. Digest of Technical Papers. 2005 Symposium on , vol., no., pp. 272- 275, 16-18 June 2005

[8] Ausin, J.L.; Perez-Aloe, R.; Duque-Carrillo, J.F.; Torelli, G.; Sanchez-Sinencio, E.; , "High-selectivity SC filters with continuous digital Q-factor programmability," Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on , vol.4, no., pp. IV-631- IV-634 vol.4, 2002

[9] Huikwan Yang; Sanghyun Cha; Seungyun Lee; Sangheon Lee; Jinup Lim; Joongho Choi; , "A 1.2V Wide-Band SC Filters for Wireless Communication Receivers," TENCON 2006. 2006 IEEE Region 10 Conference , vol., no., pp.1-4, 14-17 Nov. 2006

[10] Reja, M.M.; Moez, K.; Filanovsky, I.; , "A wide frequency range CMOS active inductor for UWB bandpass filters," Circuits and Systems, 2009. MWSCAS '09. 52nd IEEE International Midwest Symposium on , vol., no., pp.1055-1058, 2-5 Aug. 2009

[11] Munoz, F.; Torralba, A.; Carvajal, R.G.; Tombs, J.; Ramirez-Angulo, J.; , "Floating-gate-based tunable CMOS low-voltage linear transconductor and its application to HF gm-C filter design," Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on , vol.48, no.1, pp.106-110, Jan 2001

[12] M. Azadmehr, Y. Berg. *"Current-starved pseudo floating-gate amplifier"*, International Conference on circuits, systems, electronics, control & signal processing, CSECS 2007.

[13] P. Hasler, M. Kucic, *"A Transistor-Only Circuit Model of the Autozeroing Floating-Gate Amplifier"*, IEEE midwest symposium on circuits and systems, Las Cruces, August 1999, pp 157-160.

[14] A. Annema, B. Nauta, R.V Langevelde, and H. Tuinhout *"Analog Circuits in Ultra-Deep-Submicron CMOS"*, IEEE Journal of Solid-State Circuits, Vol. 40, No. 1, January 2005

[15] R.F. Lyon, *"analog implementation of auditory models"*, lEEE Trans. Acoust., Speech, Signal Processing, vol. 36, pp. 11 19-1 134, July 1988