Design of a 10-b Pipelined ADC without calibration

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Abstract: - This paper describes the design of a 10-b fully differential pipelined analog-to-digital converter (ADC). The pipelined ADC has been designed using the switched-opamp technique without calibration in a 0.7 \( \mu \)m CMOS process for sensor applications. Low power consumption is one of the most important issues. An operational amplifier (opamp) sharing technique was used to decrease the power usage.

Key-Words: - Pipelined ADC, MDAC, SC technique, operational amplifier, comparator, opamp sharing technique

1 Introduction

A pipelined topology is a popular option for ADCs which offer good trade-off between conversion rate, resolution and power consumption. Popularity of this topology can be also assigned to its relatively simple and repeatable basic structure, as well as a significant reduction in the number of comparators required to achieve a high resolution when compared to other Nyquist-rate ADCs such as flash ADC. Pipelined ADCs are used in a variety of applications such as sensors, mobile systems, CCD imaging, digital video, PDA, digital receivers, fast Ethernet, etc.

However, a more serious drawback is that fewer bits per stage increase the sensitivity to component matching errors. Therefore, calibration is often required in pipelined ADCs with higher resolution. Calibration typically results in a significant die area penalty and it also needs another reference ADC with itself calibration.

In this paper, the 10-b 10MS/s ADC without calibration for sensor application is presented. To obtain low power consumption and low silicon area opamp, sharing technique was used.

2 Pipelined ADC architecture

Fig. 1 shows a 10-b pipelined ADC architecture. It consists of 8 cascaded stages (every 2 stages sharing 1 opamp), timing circuits and digital correction block. The concurrent operation of all pipelined stages makes this architecture suitable to achieve very high conversion rates. The overall speed is determined by the speed of the single stage.

Firstly, the input signal \( v_{in} \) is captured by the sample and hold (S/H) circuit. Secondly, this signal is compared in the sub-ADC with the reference levels of comparators, which produce a digital output (2 bit). This signal passes into the sub-DAC which converts it back onto the analog signal. This analog signal is subtracted from the original sampled signal \( v_{in} \). The residual signal goes into the opamp where it is amplified to the full scale range. Last stage does not need to generate residual signal, therefore is realized as a 2 bits flash ADC consisting of three comparators and few logic gates.

2.1 Input Sample and Hold circuit

Pipelined ADCs need a Sample and Hold (S/H) circuit to acquire a high frequency input signal. Without it, a pipeline ADC will have another
voltage level in a sampling network of a first stage MDAC and comparators in a first stage sub-ADC. This error will have the same effect on a pipelined ADC like if there was a comparator offset voltage, and the error becomes larger as the input frequency gets higher. If there is S/H in a pipelined ADC, input signal is sampled and is kept constant during a holding clock phase. An error arising in small timing difference between a MDAC and a sub-ADC is cancelled.

Fig. 2 shows fully differential S/H circuit, which is on a pipelined ADC input.

2.2 Multiplying digital-to-analog converter

It is difficult optimization problem to determine the optimal number of bits resolved in each stage [1][2][3]. Typically a multi-bit first stage results in lower power consumption and matching and also amplifier gain requirements of the following stages. However, the implementation of multi-bit stage possesses two major challenges. Firstly, lower feedback factor limits the maximum sampling frequency to low-to-mid rates. Secondly, multi-bit DAC requires several floating switches. Due to this reason a conventional 1.5-b stage and switched capacitor technique (SC) was used.

Fig. 3 shows a fully differential 1.5-b stage used in proposed pipelined ADC.

In the sampling phase - when the clock $\phi_1$ is high, the inputs are sampled to capacitors $C_s$ and $C_r$. When entering into the amplification phase - the clock $\phi_2$ is high, output of the sub-DAC is connected to the capacitor $C_s$ and both capacitors are connected to the opamp input/output. The residue for 1.5-bit stage is expressed mathematically by the following equations:

\[
v_{res} = 2v_{in} - V_{ref} \text{ if } v_{in} \geq \frac{1}{4} V_{ref}. \tag{1}
\]

\[
v_{res} = 2v_{in} + V_{ref} \text{ if } v_{in} \leq -\frac{1}{4} V_{ref}, \tag{2}
\]

\[
v_{res} = 2v_{in} \text{ otherwise}, \tag{3}
\]

where $v_{in}$ is an input signal of the MDAC and $V_{ref}$ is a voltage reference, which depends on the maximum input signal swing.

2.3 Comparator

A comparator produces an output signal indicating whether input signal is larger than a reference level or not. The important performance parameters for comparators are gain and speed, like for opamps. The offset of a comparator is also an important parameter to be considered. When the comparator computes the difference between two input signals, an internal offset voltage is added to this difference. Thus, when the two inputs are close together, the comparator may make an incorrect decision. However, [4] shows that by using redundant bits in the sub-ADC, a large offset in the sub-ADC comparators can be tolerated.

All bulks of NMOS transistors are connected to the ground and PMOS transistors to the $V_{DD}$. 

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where $v_{in}$ is an input signal of the MDAC and $V_{ref}$ is a voltage reference, which depends on the maximum input signal swing.
The operation of the comparator can be described as follows. When the comparator is inactive, the latch signal $V_{\text{latch}} = 0$ V, which means that the current source transistors M5 and M6 are switched-off and there is not current path between the supply voltages and ground. Concurrently the PMOS switch transistors M9 and M12 reset the outputs by shorting them to $V_{\text{DD}}$. The NMOS transistors M7 and M8 of the latch conduct and also force the drains of all input transistors M1-M4 to the $V_{\text{DD}}$; while the drain voltages of M5 and M6 are dependent on the comparator input voltages. When $V_{\text{latch}}$ is raised to $V_{\text{DD}}$, the outputs are disconnected from the positive supply, the switching current sources M5 and M6 turn on, and M1-M4 compare $V_{\text{IN+}} - V_{\text{IN-}}$ with $V_{\text{REF+}} - V_{\text{REF-}}$. Since the latch devices M7-M8 are conducting, the circuit regeneratively amplifies the voltage difference at the drains of the input pairs. The threshold voltage of the comparator is determined by the current division in the differential pairs and between the cross coupled branches [5].

Because of the dynamic current sources, together with the latch, connected directly between the differential pairs and the supply voltage, the comparator does not dissipate DC power.

### 2.4 Operational amplifier

An opamp is one of the most important building blocks in analog circuits and also in switched capacitor implementation of pipelined ADCs. Opamps are the main source of power dissipation in the pipelined ADC circuit. The power consumption of the ADC is reduced by reducing the power dissipation of opamps. This is done by designing opamps to achieve high gain without using gain boosting techniques [6]. In order to avoid limiting linearity performance from the non-idealities of opamps, opamps must have a sufficient DC gain and wide bandwidth, so output settles within 1/2 LSB to desired value in half a clock cycle. The DC gain requirement of opamp can be obtained from equation for total charge during sampling and amplifying phase [2][4][7]. Error portion due to finite opamp gain should be smaller than 1/4 LSB of remaining resolution. The gain can be found from

$$\frac{1}{A} \beta < \frac{1}{4}.\text{LSB},$$

(4)

where $\beta$ is the feedback factor and depicts, how much of the output voltage of opamp is returning back to opamp input. From equation 4 is set minimum DC gain for opamp used in this work: $A > 80$ dB.

In order to have opamp which is sufficiently settled within a given timeframe, the opamp must have enough bandwidth. However, opamp which has a large bandwidth requires high power consumption – thus, to minimize power, it is critical to optimize opamp bandwidth [8]. Referring the settling error of the first pipelined stage to the input of the ADC and noting that the total error must be less the quantization noise (i.e. $< 2^{-N}$), the required unity gain frequency of the opamp $f_{\text{GBW}}$ to achieve $N$-bit settling is thus given by

$$f_{\text{GBW}} = \frac{(N - n)\log2}{\beta \pi} f_s,$$

(5)

, where $f_s = 1/T$ is the sampling rate of the pipelined ADC, $N$ is the ADC resolution, $n$ is the MDAC resolution and $\beta$ is the feedback factor. From equation 5 is set minimum opamp bandwidth used in this work: $f_{\text{GBW}} > 30$ MHz.

![Fig.5 Principal schema of the opamp](image)

Fig. 5 shows principal schema of designed opamp. It is two stage fully differential opamp with common mode feedback circuit (cmfb) and bias circuit. This opamp has 85 dB DC gain and 28 MHz bandwidth. Power consuption is 1.2 mW.

### 3 Simulation results

The 10-b 10MS/s pipelined was designed and verified in CMOS 0.7 µm technology and is intended for sensor applications. Fig. 6 shows simulated INL a DNL.
4 Conclusion
The SC technique has been utilized to realize a 10-b 10-MS/s pipelined ADC that requires 5 V supply. The ADC consumes 20 mW at 5 V power supply, the conversion rate is 10 MS/s. Simulated INL and DNL for the ADC are +0.3/-1.88 LSB and +1.6/-0.4 LSB respectively. To improve INL and DNL parameter, it requires achieve better linearity of opamp with higher bandwidth.

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