Differential Difference Current Conveyor Based Cascadable Voltage Mode First Order All Pass Filters

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Abstract: - This paper proposes two first-order all-pass filters using DDCCs as active elements, one resistor and one capacitor. Both proposed filters have two DDCCs, one grounded resistor and one grounded capacitor. Thus the two topologies are having minimum number of components and there is no need for matching constraints on passive components. The performance of the proposed circuits is examined using PSPICE simulations with the model parameters of a 0.5 µm CMOS process. Obtained results demonstrate excellent agreement with theoretical values.

Keywords: - Current conveyor, CCII, DDA, DDCC, all-pass filter, SPICE

1 Introduction

Second generation current conveyor (CCII), introduced in 1970 [1], has been a popular building block in voltage-mode and current-mode analog applications like oscillators, various types of filters and amplifiers, due to its high and versatile performance, low power consumption, high bandwidth and high output voltage swing. Many CCII applications were available in the literature [2-13].

But CCII has a drawback. It has only one voltage input terminal. Thus it is not suitable for applications that use differential inputs or floating inputs. So, such applications require two or more CCIIIs. Differential difference current conveyor (DDCC) is more suitable in such applications. CMOS based DDCC was introduced in 1996. DDCC encompasses the good features of Differential difference amplifier (DDA) like high input impedance, low output impedance, less number of components and capability of performing arithmetic operations, and advantages of CCII such as high gain, accuracy and bandwidth. DDCC applications such as realizing squarer, square rooter and multiplier circuits, differential integrators, and voltage mode and current mode low-pass filters and high-pass filters were also demonstrated [14]. Later, many applications using DDCC were presented [15-21].

All-pass filters of first-order are widely used in analog signal processing applications for changing the phase shift, where amplitude remain unchanged. They are also used to construct quadrature and multiphase oscillators. Recently many voltage-mode and current-mode all-pass filters were presented using CCII or DDCC. Grounded passive components provide tuning facility that is required in analog ICs after manufacture, because of the problem of high tolerances. The frequency of oscillation can be adjusted by a grounded resistor without disturbing the oscillation condition. Grounded capacitors are easier for fabrication and have less parasitics compared with floating capacitors [5-8], [11-13], [18-27]. Here two new first order all-pass filters are proposed using DDCCs as active elements.

The remaining sections of the paper are organized as follows. The DDCC fundamentals and proposed design are presented in section 2 and 3. Non-ideal analysis is included in section 4. Finally, simulation results and conclusions are given in section 5 and 6 respectively.

2 DDCC Fundamentals

The symbol of five-port DDCC is shown in Fig. 1. The internal structure of this device is shown in Fig. 2 and it can be characterized by the following matrix-relations between various voltage and current variables [20, 28].

\[
\begin{align*}
[I_1] & = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_X \\ V_Z \end{bmatrix} \\
[I_2] & = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_X \\ V_Z \end{bmatrix} \\
[I_3] & = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_X \\ V_Z \end{bmatrix} \\
[I_X] & = \begin{bmatrix} \beta_1 & -\beta_2 & \beta_3 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_X \\ V_Z \end{bmatrix} \\
[I_Z] & = \begin{bmatrix} 0 & 0 & 0 & a & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_X \\ V_Z \end{bmatrix}
\end{align*}
\]

(1)

In the DDCC, \(Y_1\), \(Y_2\), and \(Y_3\) are three voltage input terminals with high input impedance. Terminal \(X\) is a low impedance current input terminal. There is a high impedance current output terminal \(Z\). The hybrid matrix can be represented by the following equations:

\[
I_{Y1} = I_{Y2} = I_{Y3} = 0, V_X = \beta_1 V_1 - \beta_2 V_2 + \beta_3 V_3,
\]

and \(I_Z = \alpha I_X\)

(2)
Here α represents the current tracking error from X to Z terminal. β₁, β₂ and β₃ represent the voltage tracking errors from Y₁, Y₂, Y₃ to X terminal. Ideally β₁ = β₂ = β₃ = α = 1. Actually these tracking errors arise due to parasitic capacitance and resistance of the DDCC.

It provides 0° to 180° phase shift. Its phase response is given by
\[
\phi(\omega) = -2 \tan^{-1}(\omega CR)
\]  
(6)

4 Non-Ideal Analysis

So far, ideal characteristics for the DDCC are being considered in the analysis. However, in this section of investigation, the analysis could change if the parameters of non-idealities are taken for granted.

From Fig. 3, we can write voltage transfer function as
\[
\frac{V_o(s)}{V_i(s)} = \frac{\beta_{11} \beta_{21} sC - \alpha_1 \beta_{22}}{sC + \alpha_1 \beta_{12}}
\]  
(7)

and phase response as
\[
\phi(\omega) = 180° - \tan^{-1}\left(\frac{\beta_{21} \omega CR}{\alpha_1 \beta_{22}}\right) - \tan^{-1}\left(\frac{\omega CR}{\alpha_1 \beta_{12}}\right)
\]  
(8)

From Fig. 4, we can write voltage transfer function as
\[
\frac{V_o(s)}{V_i(s)} = \frac{\beta_{11} (\alpha_1 \beta_{21} - \beta_{22} sC)}{\alpha_1 \beta_{12} + sC}
\]  
(9)

and the phase response as
\[
\phi(\omega) = -\tan^{-1}\left(\frac{\beta_{21} \omega CR}{\alpha_1 \beta_{12}}\right) - \tan^{-1}\left(\frac{\omega CR}{\alpha_1 \beta_{21}}\right)
\]  
(10)

Effects of non-ideality on pole frequency:

Ideally, from Eqs. (3) and (5), we can observe that the pole/zero frequency will be \(\omega_{p/z} = 1/RC\) and its sensitivity due to passive element is \(S_{\phi_{p/z}} = 1\). From
Eqs. (7) and (9) we can observe that the pole frequency is different from the zero frequency and it is given by the following characteristic equations.

For Fig. 3, $\omega_p = \frac{\alpha_1 \beta_{12}}{RC}$, $\omega_z = \frac{\alpha_1 \beta_{22}}{\beta_{21} RC}$ and

For Fig. 4, $\omega_p = \frac{\alpha_1 \beta_{12}}{RC}$, $\omega_z = \frac{\alpha_1 \beta_{22}}{\beta_{21} RC}$

After completion of analysis we found that the sensitivity of pole or zero frequency due to DDCC is not more than unity. The sensitivities for Fig. 3 are given by

$$S_{\omega p} = 1$$

$$S_{\omega z} = 1$$

and for Fig. 4, they are denoted by

$$S_{\omega p} = 1$$

$$S_{\omega z} = 1$$

In comparison with the published all pass filter, this filter can have additional transfer function,

$$\frac{V_i(s)}{V_o(s)} = \frac{2(1-sCR)}{1+sCR}$$

i.e., this filter is also capable of producing amplified output by connecting the Y3 terminal to Y1.

5 Simulation Results

The proposed all-pass filters were simulated using PSPICE with 0.5 µm MITECH parameters. The parameters are given in table I and the aspect ratios of transistors are given in table II.

The supply voltages of proposed all-pass filter circuits are ±2.5 V and the biasing voltage $V_B$ is -1.7 V. The simulation results of all-pass network shown in Fig. 3 are given in Fig. 5 and Fig. 6 and those of all-pass network shown in Fig. 4 are given in Fig. 7 and Fig. 8. The passive component values selected are $R=10$ kΩ, $C = 100$ pF and the pole frequency $f_0 = 159$ KHz.

6 Conclusion

In this paper, two new voltage-mode first-order all-pass networks employing two DDCCs, one grounded resistor, another grounded capacitor are presented. Both use optimum and canonical number of passive components. So there is no need for passive component matching. No capacitors are connected at X terminal. We found that Total Harmonic Distortion (THD) of both circuits is less than 4%. However its value is decreasing for first proposed circuit with increasing frequency and it is less than 2%. Both the circuits have grounded resistor and grounded capacitor, which provide the tunable property. The circuits are verified using SPICE simulation and the simulated results agreed with theoretical ones. These are alternative better circuits than the ones present in [15], and have added advantages of parasitic resistances and capacitances that can be minimal. The circuit presented in [18], provides only low output impedance. And circuits presented in [5-7] uses the floating passive element and have element matching restrictions.

References


TABLE I 0.5 µm MITEC CMOS PROCESS MODEL PARAMETERS; LEVEL-3

<table>
<thead>
<tr>
<th>MODEL NT NMOS LEVEL=3</th>
</tr>
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<tbody>
<tr>
<td>+UO=460.5 TOX=1.0E-8 TPG=1 VTO=-.62 JS=1.8E-6+XJ=.15E-6 RS=417 RSH=2.73 LD=0.</td>
</tr>
<tr>
<td>ETA=0+VMAX=130E3 NSUB=1.71E17 PB=.761</td>
</tr>
<tr>
<td>PHI=0.905+THETA=0.129 GAMMA=0.69</td>
</tr>
<tr>
<td>KAPPA=0.1 AF=1+WD=.11E-6 CJ=.764E-5</td>
</tr>
<tr>
<td>MJ=0.357CGSO=.38E-10+MJSW=0.302</td>
</tr>
<tr>
<td>CGSO=1.38E-10 CGDO=1.38E-10+CGBO=3.45E-10</td>
</tr>
<tr>
<td>KF=3.07E-29 DELTA=0.42+NFS=1.2E11</td>
</tr>
</tbody>
</table>

TABLE II TRANSISTORS ASPECT RATIOS

<table>
<thead>
<tr>
<th>TRANSISTOR</th>
<th>W (µm)</th>
<th>L (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M3, M4, M5</td>
<td>0.8</td>
<td>0.5</td>
</tr>
<tr>
<td>M6</td>
<td>14.4</td>
<td>0.5</td>
</tr>
<tr>
<td>M7, M8</td>
<td>4.0</td>
<td>0.5</td>
</tr>
<tr>
<td>M9, M11</td>
<td>10.0</td>
<td>0.5</td>
</tr>
<tr>
<td>M10, M12</td>
<td>45.0</td>
<td>0.5</td>
</tr>
</tbody>
</table>


Fig. 5 Phase and magnitude plots of the proposed circuit of Fig. 3

Fig. 6 Dependence of output voltage harmonic distortion on input voltage frequency for 0.2 V_{pp} of Fig. 3

Fig. 7 Phase and magnitude plots of the proposed circuit of Fig. 4

Fig. 8 Dependence of output voltage harmonic distortion on input voltage frequency for 0.2 V_{pp} of Fig. 4