A Combinational Approach of Modeling Analog Phase Locked Loop

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Abstract:- In this paper a vital component of communication system, a general purpose analog Phase lock loop (PLL) is modeled using a novel combinational approach which apart from having a high speed also mimics IC behavior in Silicon. An analog/digital circuit simulator PSpice is used for the purpose. The advantage of SPICE is that it offers models that accurately define a CMOS process. Since, SPICE simulator is actually a standard CAD tool for IC design; modeling phase detector (PD) at primitive/component level improves accuracy. On the other hand, Voltage Controlled Oscillator (VCO) modeled using Analog Behavioral model (ABM) technique results in increasing speed. The proposed combinational approach is a cascade of primitive model of PD and behavioral model of VCO and has an overall effect to augment accuracy. Not only the proposed model is more accurate but speed is also now comparable to less accurate behavioral model of PLL. The loop filter being a simple RC circuit can be modeled either by using ABM method or using PSpice primitives, and doesn’t affect simulation speed. The concept is used for modeling PLL IC LM 565.

Key-Words:- Phase Detector, Voltage Controlled Oscillator, PLL, PSpice, Analog Behavioral Model.

1 Introduction
There are several different simulators used in industry for PLL simulations, each one having its advantages and disadvantages. Traditionally, PLL’s implemented on a chip (microprocessor, digital signal processor, ASIC, clock chip, etc.) are modeled with general-purpose simulators such as PSpice. Other simulators include EESof, Matlab, and analytical/behavioral models. The main aspects that make a PLL difficult to simulate are as follows:

- Two sources of feedback – main feedback (“loop” in phase-locked loop) and oscillator feedback
- High frequency clocks in conjunction with low frequency time constants
- Pico-second accuracy
- Digital components mixed with analog components (mixed-mode)
- Digital – phase detector, frequency divider
- Analog – voltage-controlled oscillator (VCO), charge pump, loop filter
- A PLL simulator should:
  - Run fast?
  - Model CMOS processes
  - Predict lock range (frequency range over which the PLL will lock) [1].
  - Although SPICE given accurate models, can perform an accurate simulation, it can be very time consuming.
  - The utilization of a voltage-controlled tuned circuit as the VCO that does not require feedback to produce an oscillating output is a method that can be used to reduce simulation time [2]. Despite the reduced simulation time, the number of data points and calculations are still immense. The advantage of SPICE is that the models that accurately define a CMOS process are readily available. Apart from Spice, the communication toolbox in Matlab also have model for charge-pumped PLLs. These models run fairly fast but still generate large amount of data. The Matlab models would have to be significantly modified to simulate a PLL built in a real CMOS process. Matlab still has the notion of time steps, which leads to some of identical problems as with SPICE, but does not have to make transistor-level calculations. Clearly accuracy would suffer if the analytical model does not mimic the behavior in silicon. Efforts have been made to increase the accuracy of Matlab simulations by better modeling of the PLL blocks to reflect the CMOS process [3] [4]. Traditionally, the textbook s-domain PLL model has been used to
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Hierarchical description level, the information loss the VCO control voltage.

with a sine function in which the phase is linked to using Laplace domain transfer function and a VCO function for phase detection, a first order loop filter modeling syntax, by using a cascade of a multiplier modeled succinctly in PSpice extended behavioral called system level description [7]. The PLL can be modeled at its global function level, or so (OP Amps, PLL, Filters etc), and finally, the circuit sources, VCO), then a circuit at the functional level are the elementary bricks for the ICs (current elements), then the basic building functions that can also be used to design systems at an abstract level, ensuring that the concepts are correct, before proceeding with the detailed circuit -level design. Spice’s syntax is nonprocedural. This approach has proven to be convenient and powerful. Presenting Analog Behavioral Modeling as functional or state machine forms fits in naturally with existing SPICE usage and is to be preferred over procedural, programmatic, extensions.

2. PSpice Modeling of Analog PLL

In this paper a novel combinational method of modelling general purpose analog Phase locked loop is presented. When investigating the analog circuit structure of PLL IC, the several levels of function description can be distinguished. Firstly, the lowest transistor level containing the simulator's primitives (transistors, passive elements), then the basic building functions that are the elementary bricks for the ICs (current mirrors, differential stages, current and voltage sources, VCO), then a circuit at the functional level (OP Amps, PLL, Filters etc), and finally, the circuit can be modeled at its global function level, or so called system level description [7]. The PLL can be modeled succinctly in PSpice extended behavioral modeling syntax, by using a cascade of a multiplier function for phase detection, a first order loop filter using Laplace domain transfer function and a VCO with a sine function in which the phase is linked to the VCO control voltage. **Though, behavioral modeling is fast but doesn’t mimic the IC behavior in silicon.** In practice, when we pass off a higher hierarchical description level, the information loss increases and simulation time decreases [7]. Therefore, the challenge is how to solve the conflict between accuracy and simulation time (speed). A novel “combinational” method of modeling PLL is presented here which is a compromise between accuracy and speed. In this method, the phase detector is modeled using PSpice primitives (increasing accuracy and reducing speed), and VCO is modeled using analog behavioral modeling (ABM) approach (increasing speed and reducing accuracy). Since, SPICE simulator is actually a standard CAD tool for IC design, modeling phase detector at primitive level improves accuracy. On the other hand, VCO modeled using ABM technique results in increasing speed, a great deal. The cascading of PD & VCO outputs has overall effect to augment accuracy, and speed is now comparable to behavioral model of PLL. The loop filter being a simple RC circuit can be modeled either by using ABM method or using PSpice primitives, and doesn’t affect simulation speed. **Moreover, phase detector modeled mimics the IC behavior in silicon.**

As an example, the Phase Locked Loop IC LM565 is modeled here with the proposed approach. It is a standard PLL integrated circuit that, apart from the bias circuitry, contains a Schmitt trigger for VCO and a Gilbert multiplier for phase detector. It has 28 transistors, 10 diodes and many resistors. The goal here is to use an IC whom the characteristics are given in the datasheets and to perform an accurate simulation of IC internal behavior.

2.1 Primitive Model of Phase Detector

Fig.1 depicts the double balanced phase detector and amplifier used in the microcircuit LM 565. Referring application notes AN-46 and datasheet of LM 565 the resistance values in circuit of Fig. 1 can be found out. The simulation of this circuit at transistor level is especially difficult and not sure because not all parameter values for IC internal elements, in particular transistors are available, and also the topology is too complex. But, a judicious thinking in case of doubly balanced phase detector can enable accurate modeling even without knowing all internal details of the transistors. The fact that the transistors Q1 through Q6 used in doubly balanced modulator has to be identical firstly because of they being differential pairs (Q1&Q2, Q3&Q4, and Q5&Q6) and secondly their transfer characteristics have to be identical as they are required to
Fig. 1: Phase detector spice model: A circuit level approach

Fig. 2: Simulated output of phase detector for 0, 90, 180 deg

Fig. 3: PD Sensitivity graph

Fig. 4: Analog Behavioral Model of VCO
be operated in linear region for multiplier operation [8].

Not only this the transistors (Q8, Q9,Q10 ) in phase detector model of Fig. 1, are used for setting up current and voltage bias, and also substituted by PSpice transistor library transistor Q2N2222. The Resistance R15 is adjusted such that the PLL parameter “common mode error voltage” is 4.5 volts to conform to datasheet value. The remaining transistors Q10 & Q11 are amplifiers their gain is adjusted so as to get phase detector sensitivity is close to manufacturer’s specified value of 0.68 volts/rad. The simulation results of Fig. 2 is one-shot display of resultant error voltage as obtained through parametric sweep for phase angles of 0, 90 & 180 degree and identical to characteristics as given in application notes AN-46 thus confirming the viability of PD model.

PSpice simulator is also used for obtaining phase detector sensitivity. For this purpose, parametric sweep of phase angle attribute of Spice Sinusoidal source ‘Vsln’, for the range from –180 deg to +180 deg; in steps of 10 degree is made. The transient analysis of PSpice simulator has produced 18 sets of output voltage, which is then averaged out using probe macro facility, and is measured, with the help of probe cursor. These measured values corresponding to phase angle parameter are exported to MS Excel for obtaining sensitivity plot as shown in Fig. 3. The measured value of PD sensitivity (K0) is 0.65 volts/radian as against 0.68 volts/radian mentioned in data sheet. This error may easily be compensated by adjusting VCO sensitivity (K0), as in closed loop calculation, normally; one is interested in loop gain (Kv,K0), which is a product of individual sensitivity of PD or VCO. Moreover, VCO being modeled using ABM technique, K0 is only a variable parameter and can be assigned any value of interest.

3 Behavioral Modeling of VCO

The VCO is modeled with a sine function in which, the phase is linked to the control voltage. The modeling approach is termed as Analog Behavioral Modeling (ABM) as shown in Fig 4. The proposed model assumes a linear response however the control voltage equation can be modified as desired. The circuit is modeled as a sine generator controlled by control voltage. The sine generator can be modeled using ‘EVALUE’ function or the ‘ABM’ functions. The EVALUE function in Fig. 4 is used to generate divided output whereas ABM function is used for undivided output. The equation for the generator is:

\[ e = \sin\left(\frac{tw \cdot f_c}{N} \cdot \text{time} + V(\text{int})\right) \]  

(1)

Where, fc is defined as the centre frequency of VCO, when control voltage is zero. This is expected VCO frequency before frequency division. For the purpose of simulation, the counter value N, has been written into the equation to ensure correlation between modeled circuit and mathematical loop filter calculations. ‘tw’ is 2π; additional decimal places can be added as needed. If, (1) is compared with a general sinusoidal expression \( e=\sin((2\pi f)\cdot \text{time}+\phi) \), then \( V(\text{int}) \) is clearly a representative value for the phase and is produced by a control voltage effect in ABM modeling of VCO. This is expressed as:

\[ V(\text{int}) = \left(\frac{k_1}{tw \cdot N}\right)(V(\text{ctrl})-4.5) \cdot Qc \]  

(2)

Qc determines the value of the current to be integrated by the capacitor C1. R1 is arbitrarily set to 1000 Mega ohms and is not an active part of the circuit; however it has been included to prevent open pin errors from PSpice software. The GVALUE function is used to perform the generation of \( V(\text{int}) \). There is some interaction between the integrator (GVALUE output & C1), and R1. \( V(\text{int}) \) is a continuous ramp that is loaded by resistance of R1. Unless GVALUE output current is sufficiently large for the value chosen for R1, the VCO control voltage required to maintain lock will increase throughout the simulation producing nonlinear operation. The output of sine generator is amplified by 1000 to produce a sharp rise/fall time and output is limited by limiter to swing between the values of –0.6 volts and +5.4 volts to make it compatible with LM 565 VCO output as shown in Fig. 5. The resultant circuit/symbol accepts a voltage input from the loop filter and produces a square wave output at the desired frequency. If sufficient resolution is used in the simulation, the PSpice probe FFT transform can be used to provide the typical spectrum analyzer display.

4. Combinational Modeling

In the earlier section modeling of Phase detector and that of VCO is described. For complete modeling of LM 565, the phase detector output is connected with VCO control input Vctrl through loop filter as an intermediate functional block.
Fig. 5: Simulated compatible VCO output

Fig. 6(a): Phase locking between input & VCO Output

Fig. 6(b): Frequency spectrum during phase locking
In classical PLL’s, the loop filter is a RC network with one pole and one zero. Some loop filters also have a gain factor included. Alternatively, loop filter may be represented in Laplace transform form using frequency domain controlled sources such as elaplace or glaplace. The loop filter integrates the error signal, attenuates high frequency components, and provides the needed phase correction to keep the PLL stable. Overall stability of the PLL is tuned via the loop filter characteristics. However, it is also influenced by the VCO frequency and control sensitivity (VCO gain), the phase detector gain, and the scaling factor used between VCO and phase detector.

In the operation of the loop, the low-pass filter serves dual function: (i) attenuating high frequency error components at phase comparator output (enhances interference rejection characteristics); (ii) provides short term memory against noise transient (ensures rapid recapture of the signal if it is thrown out of lock). A transient analysis is run to analyze capture and lock process. The simulation results are shown in Fig. 6 (a-b). The PLL does not respond to input signal until input frequency reaches lower edge of capture range. Up to lower capture frequency, the VCO output frequency does not change significantly since average voltage of beat frequency is zero. The PLL then suddenly locks to input signal, causing a negative jump in loop error voltages with resulting nonlinear capture transients. Once locked, error signal tracks small frequency changes of the input signal by generating additional phase error between VCO and input signal until it is converted to DC error voltage by phase detector and low-pass filter. At the upper lock range frequency, the model losseeds lock, and error voltage suddenly drops with resultant beat note.

5 Conclusion
This paper presents modeling of one of the building block of a communication and a tracking system, a general purpose analog PLL IC LM 565, by introducing a new concept of combinational modeling. Wherein, modeling phase detector at primitive level improves accuracy, and VCO is modeled using ABM technique that results in increasing speed, a great deal. The cascading of PD & VCO outputs has overall effect to augment accuracy, and speed is now comparable to behavioral model of PLL. The loop filter being a simple RC circuit can be modeled either by using ABM method or using PSpice primitives, and doesn’t affect simulation speed. Moreover, phase detector modeled mimics the IC behavior in silicon. . The model works out to the specifications.

References: