

Static Ultra Low-Voltage and High Performance CMOS NAND and NOR Gates

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Abstract: In this paper we examine the robustness and performance of static ultra low-voltage CMOS binary logic. The logic gates presented are designed using semi floating-gate transistors and resembles domino CMOS. The performance and robustness of different logic gates are examined and compared to complementary and domino CMOS logic.

Key-Words: CMOS, Low-Voltage, Domino logic, Floating-Gate, High-Speed, NAND, NOR

1 Introduction

The need for novel digital logic styles for both ultra low supply voltage and low power applications is more and more evident. Especially, for hand held and mobile equipment, the power and supply voltage are important aspects to consider when designing both analog and digital systems. The digital circuits shrink rapidly with the introduction of recent semiconductor processes. The energy requirement for switching digital signals are at its minimum when the supply voltage is at its minimum[1]. However, the performance of digital systems is often characterized by Energy-Delay-Product (EDP) which for most applications will entail a optimum for supply voltages close to the threshold voltage of the transistors used. Low supply voltage can be a requirement as a result from a power reduction strategy in digital circuitry.

Floating-Gate (FG) gates have been proposed for Ultra-Low-Voltage (ULV) and Low-Power (LP) logic [2]. However, in modern CMOS technologies there are significant gate leakage which undermine non-volatile FG circuits. FG gates implemented in a modern CMOS process require frequent initialization to avoid significant leakage. By using floating capacitances to the transistor gate terminals the semi-floating-gate (SFG) nodes can have a different DC level than provided by the supply voltage headroom [2]. There are several approaches to FG CMOS logic [3, 4, 5]. The gates proposed in this paper are influenced by ULV non-volatile FG circuits [6]. The logic style characterized in this paper is based on dynamic and static ULV inverters presented in [7, 8]. In section 2 the static ULV differential domino inverter is de-

scribed followed by a differential static ULV NAND and NOR gates in section 3.

2 Static ULV Logic

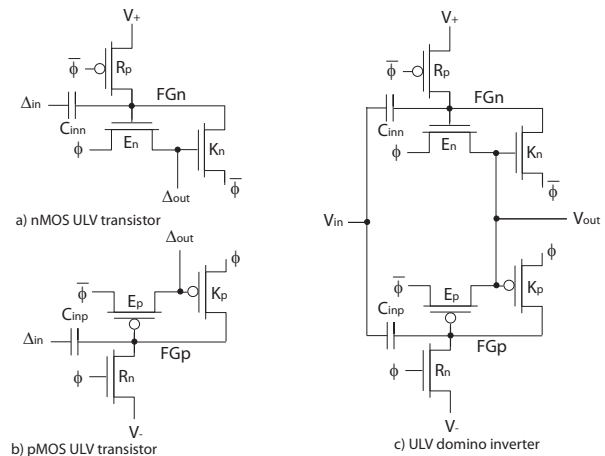


Figure 1: a) *nMOS ULV transistor*, b) *pMOS ULV transistor* and c) *static ultra low-voltage semi-floating-gate recharge inverter*. The transistors labeled K_n and K_p provide a feedback making the output static.

The ULV transistor configurations and an ULV domino inverter is shown in Figure 1. The ULV transistor configuration consists of two three standard transistors:

- **Evaluate transistor**, E_p or E_n . The evaluate transistors are driving the gate outputs.

- **Recharge transistor**, R_p or R_n . The recharge transistors are used to recharge the gate of the evaluate transistors in the precharge mode.
- **Keeper transistor**, K_p or K_n . The keeper transistors are used to reduce the static current consumption by draining one of the evaluate transistors in the evaluation mode. The keeper transistors will improve both power consumption and noise margin.

The static ULV domino inverter[8] shown in Figure 1 c) will be precharged to $V_{DD}/2$ in the precharge phase and invert any input changes occurring in the evaluation phase, i.e. $\Delta V_{out} = -\Delta V_{in} \equiv |V_{DD}/2|$.

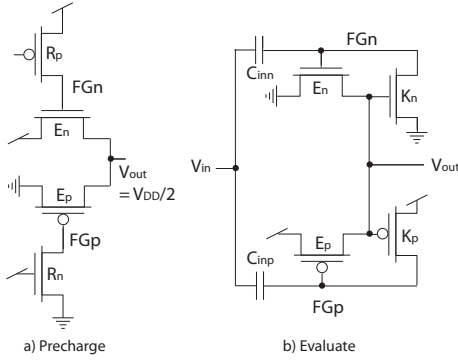


Figure 2: a) ULV inverter in precharge mode and b) ULV inverter in evaluate mode.

The recharge and evaluation mode are characterized by:

- **Precharge/recharge**, shown in Figure 2 a). The nMOS floating-gate is recharged to V_+ and the pMOS floating-gate is recharged to V_- while the output and input are precharged to $V_{DD}/2 = (V_+ - V_-)/2$. The output will be forced to $V_{DD}/2$ due to a reversed biased inverter.
- **Evaluate**, shown in Figure 2 b). The output will be pulled to V_{DD} if a negative transition, $\Delta V_{in} = -V_{DD}/2$, occurs and to V_{SS} if there is a positive transition, $\Delta V_{in} = V_{DD}/2$, applied at the input.

2.1 Differential Static ULV Logic

A problem with the SULV logic is the potential false output transient if the input transient is significantly delayed compared to the clock edge. If the output reaches a false state the state will be fixed. By using a differential ULV style shown in Figure 3 the keepers will not be activated before the arrival of the input transient.

The differential ULV inverter in evaluation mode is shown in Figure 4 assuming $\Delta V_{in} = V_{DD}/2$.

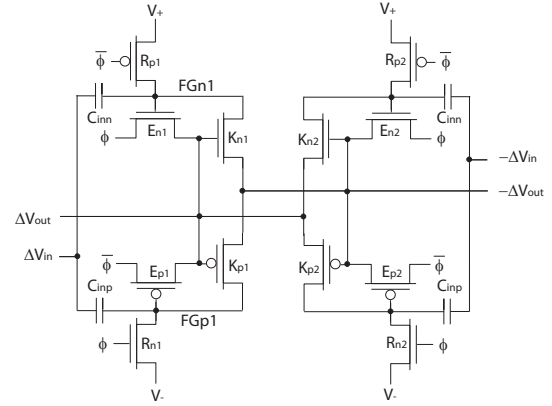


Figure 3: Differential ULV inverter.

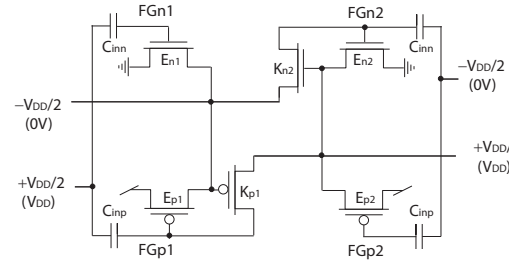


Figure 4: Differential ULV inverter in evaluate mode assuming an input $\Delta V_{in} = V_{DD}/2$.

3 ULV NAND/NOR Gates

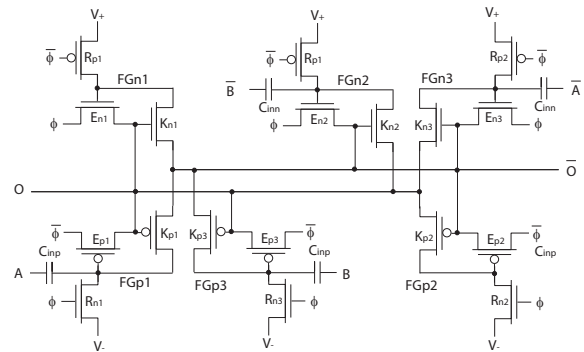


Figure 5: Differential ULV NAND gate (N1).

The differential ULV NAND (N1) gate is shown in Figure 5. By applying the two inputs A and B to two parallel static pMOS ULV transistors, the output O will be pulled from $V_{DD}/2$ ($1/2$) to V_{DD} (1) if any of these inputs switches from $1/2$ to 0 . Assuming that the external load for each output is $C_{inn} + C_{inp} \approx 6C$, yielding a capacitive division factor for the floating capacitances equal to $1/2$, we can derive a simple model for the output load of the gate; $C_L = C_{inn} + C_{inp} + 2C_d + 3C_g + 3C_s \approx 14C$. The delay of the NAND gate is dependent on the input sig-

A	B	O	E_{p1}	E_{p3}	E_{n2}	E_{n3}	Speed
0 (-1/2)	0 (-1/2)	1 (1/2)	on	on	on	on	Fast
0 (-1/2)	1 (1/2)	1 (1/2)	on	off	off	on	Medium
1 (1/2)	0 (-1/2)	1 (1/2)	off	on	on	off	Medium
1 (1/2)	1 (1/2)	0 (-1/2)	off	off	off	off	Slow

Table 1: The operation of the differential ULV NAND (N1) gate.

nals, the delay increases with the number of positive input transients of A and B as shown in Table 1. The worst case delay is obtained when $A = B = +1/2$ ($\bar{A} = \bar{B} = -1/2$) because the current level of nMOS evaluate transistor E_{n1} is not increased. The response of the gate will be correct due to the decrease in current level of both E_{p1} and E_{p3} . The synchronization of the input signals is important for the NAND gate shown in Figure 5. Consider the case where the one of the input signals is delayed compared to the other input signal. If the first arriving input transient is $+1/2$, for example $A = +1/2$ and $\bar{A} = -1/2$, the current level of transistors E_{p1} and E_{n3} will be reduced and transistor E_{n1} will pull output 0 down towards 0 (gnd) while E_{p2} will pull \bar{O} towards 1. The current levels of E_{p3} and E_{n2} will not be reduced significantly until the keeper transistors K_{p3} and K_{n2} kicks inn. The timing response of the NAND gate in this stuation is dependent the diffence in driving capabilites of transistor E_{n1} and E_{p3} , and E_{p2} and E_{n3} . We may assume that the current providing a transient at B and \bar{B} will be at least twice the current level pulling the outputs due to the leakage situation decribed. If the NAND gate snaps into a false state it will not be influenced by the second input and the false state will be crucial.

There are some additional problems associated with the NAND gate

1. The worst case delay. Determined by the inputs $A = B = -1/2$ yielding an effective gate voltage equal to V_{DD} of E_{n1} (and E_{p3}). The minimum ON current, i.e. effective gate voltage, should be as high as possible in order to reduce the delay and increase the noise margin.
2. The leakage current compared to the minimum ON current, both determined by an effective gate voltage equal to V_{DD} . The minimum ON current should be higher than the leakage current, i.e. higher effective gate voltage for the ON transistor.
3. The minimum ON current compared to the maximum ON current, given by effective gate voltages equal to V_{DD} and $\frac{3V_{DD}}{2}$. A large difference

	C_L	E_{n1} V_{eff}	E_{p2} V_{eff}	V_{gs} I_{LEAK}	NM^*
N1	14C	V_{DD}	V_{DD}	V_{DD}	V_{DD}
N2	17C	$\frac{3V_{DD}}{2}$	$ \frac{3V_{DD}}{2} $	$\frac{4V_{DD}}{3}$	$\frac{3V_{DD}}{2}$

Table 2: Worst case, i.e. $A = B = 1/2$ for N1 and $A \neq B$ for N2.

in ON currents will yield an increased power consumption.

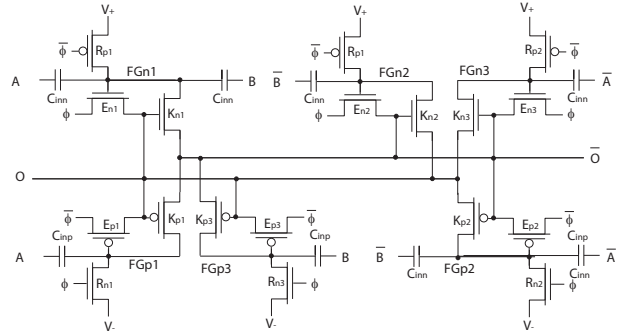


Figure 6: Differential ULV NAND (N2) gate.

In order to increase the worst case speed of the NAND gate we can add floating input capacitors as shown in Figure 6 (N2). The timing response of the N2 gate is less dependent of the input signals and more similar to complementary CMOS. All evaluate transistors receive inputs and the current level in the worst case will be increased compared to N1. When $A = B = 1/2$ the effective voltage of E_{n1} is increased from V_{DD} to $\frac{3V_{DD}}{2}$ as shown in Table 2. The worst case delay for N2 is when $A \neq B$ and the timing response is not significantly dependent of the input values. Furthermore we can apply a simple model for the noise margin $NM = V_{ON}/V_{OFF} \approx V_{ON}$, where V_{ON} is the maximum current level of the evaluate transistors in the worst case, i.e. $A = B = 1/2$ for N1 and $A \neq B$ for N2, and $V_{OFF} = 0V$ is the OFF current or static leakage current. The ON current of the ULV NAND2 gate is approximately 10 times

VDD	N2 min	N2 max	CMOS	Relative
200mV	3.31ns	5.39ns	14.01ns	38%
250mV	0.689ns	0.931ns	4.15ns	22%
300mV	0.264ns	0.426ns	1.63ns	26%
350mV	0.110ns	0.165ns	0.583ns	28%
400mV	0.058ns	0.082ns	0.292ns	28%

Table 3: The minimum, $A = B$, and the maximum, i.e. $A \neq B$, parasitic delay for the NAND2 ULV gate. The parasitic delay for complementary CMOS inverter is also shown.

the ON current of a complementary CMOS inverter while the OFF currents are equal. In effect this will increase the ratio of the ON to OFF current of the ULV gates compared to complementary CMOS. By inverting the inputs of the circuit shown in Figure 5 and 6 the boolean function is changed to NOR2. The performance of the NOR2 gates are equivalent to the NAND gates in terms of speed, power, EDP and robustness. Furthermore, the UVL logic gates presented in this paper can easily be applied as latches by using two gates with opposite clock signals [8].

3.1 Simulation Results

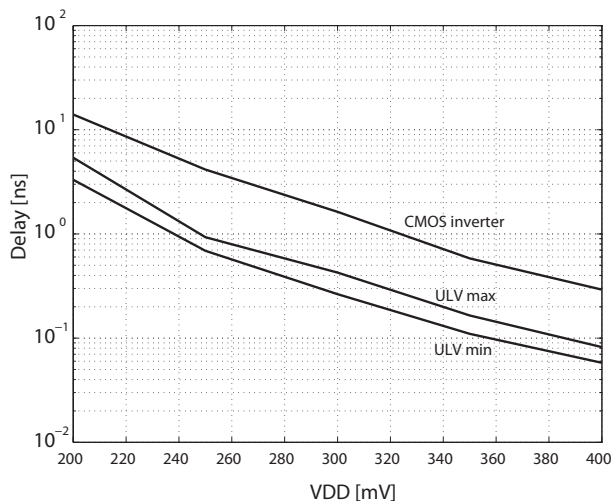


Figure 7: Maximum and minimum delay for the ULV differential NAND2 gate.

The minimum, $A = B$, and the maximum, i.e. $A \neq B$, parasitic delay for the NAND (N2) ULV gate is shown in Table 3 and Figure 7. The effect of a natural load can easily be estimated. If the ULV NAND2 gate is driving a similar gate the additional load will be $C_{inn} + C_{inp}$ which is an increase of the load equal to 75%. For a CMOS inverter the added load would be

100%. The proposed domino logic style can be used to reduce the delay in critical paths and in critical sub-circuits and systems.

4 Conclusion

Ultra low-voltage and high speed differential NAND and NOR gates have been presented. The gates offers increased speed and noise margin for ultra low-voltage applications. Preliminary simulation results are included for a 90nm CMOS process.

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