Differential Static Ultra Low-Voltage CMOS Flip-Flop for High Speed Applications

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Abstract: In this paper we present a simple ultra low-voltage and high speed D flip-flop. The delay of the static differential flip-flop presented is less than 12% compared to conventional differential CMOS flip-flops. The presented circuits have been simulated using $Hspice$ and are valid for $90nm$ TSMC CMOS process. The proposed high-speed and ultra low-voltage flip-flop can be used for any digital low-voltage CMOS application.

Key–Words: CMOS, Low-Voltage, Flip-Flop, Floating-Gate, High-Speed, Differential

1 Introduction

The ever increasing problem associated with modern CMOS processes is the demand for digital CMOS gates operating at low supply voltages. The available supply voltage and threshold voltage is lowered as a consequence of the reduction in transistor length. When the supply voltage is decreased the speed of the logic circuits may be reduced due to reduced effective input voltage to the transistors. When the threshold voltage is reduced the off current running through transistors which are switched off will increase and thereby increase static power consumption and reduce noise margins. Voltage scaling reduces the active energy and unfortunately speed as well. Low voltage applications are often dominated by low speed and low energy requirements, typical battery-powered electronics. The optimal supply voltage for CMOS logic in terms of Energy-Delay-Product (EDP) is close to the threshold voltage of the nMOS transistor V_{tn} for the actual process, assuming that the threshold voltage of the pMOS transistor V_{tp} is approximately equal to $-V_{tn}$ [1]. Several approaches to high speed and low voltage digital CMOS circuits have been presented [2, 3, 4].

Floating-gate (FG) CMOS gates have been proposed for ultra low-voltage (ULV) and low power (LP) logic [5]. However, in modern CMOS technologies there is a significant gate leakage which undermines non-volatile FG circuits. FG gates implemented in a modern CMOS process require frequent initialization to avoid significant leakage. By using floating capacitances to the transistor gate terminals the semi-floating-gate (SFG) nodes can have a different DC level than than provided by the supply voltage headroom [5].

The ULV logic [6] gates can be operated at a clock frequency more than 10 times than the maximum clock frequency of a similar complementary CMOS gate operating at the same supply voltage. For high clock frequencies, the switching energy consumed by the ULV gate will be reduced compared to a complementary gate.

In this paper we present an ultra low-voltage flip-flop using ULV CMOS logic. The ULV logic offers a significant speed improvement compared to conventional sense amplifier flip-flop [7]. In section 2 we propose a simple ultra low-voltage flip-flop. The proposed symmetric and static ultra low-voltage flip-flop is described in section 3 with simulated results using a $Hspice$ simulator.

2 ULV Flip-Flop

The single phase high-speed ULV flip-flop is shown in Figure 1. The master latch is active when $\phi = 1$. In this phase the differential input is latched onto QM and $\overline{QM}$ and the differential output is not affected by the input due to the low skew inverters. The gates of transistors labeled E_{p1} and E_{p2} are charged by $\overline{D}$ and D respectively. At the arrival of a negative clock edge the recharge transistors R_{n1} and R_{n2} connected to the differential input are OFF and both QM and $\overline{QM}$ will be pulled down by the floating capacitor. We can express the impact of the floating capacitors to the floating-gate voltages as

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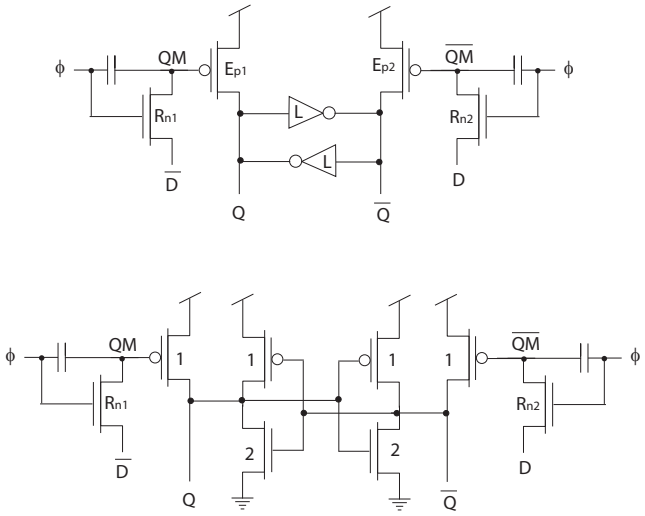

Figure 1: The single phase high-speed ULV Flip-Flop.

$$V_{QM} = V_{\overline{D}} - k_{in}V_{DD}$$
$$V_{\overline{QM}} = V_D - k_{in}V_{DD},$$

where $k_{in} = C_{in}/C_T$, C_{in} is the floating input capacitance and C_T is the total capacitance seen by a floating-gate. If $V_{QM} = 0V$, i.e. logic 0, the effective gate source voltage of the E_{p1} transistor is $|(1 + k_{in}) \times V_{DD}|$ after the negative clock edge has arrived. An appropriate value for k_{in} is 0.5, hence the effective gate source voltage is $|(3/2) \times V_{DD}|$. This is the only event that may override the present value of the output of the flip-flop. The large current provided by the boosted E_{p1} transistor will set the output Q to 1 and the low skew inverter will respond and force $\overline{QM}$ to 0.

The operation of the ULV flip-flop is shown in detail in Figure 2. Depending on the clock signal the operation is defined as

1. $\phi = 1$, shown in Fig. 2 b). The recharge transistors connecting the differential input is on and the input is latched, i.e. $\overline{QM} = D$ and $QM = \overline{D}$. The output of the flip-flop is stable and will not be affected by latching of the input. The $E_{p1/2}$ transistors are weak and can not affect the output.

2. $\phi = 1 \rightarrow 0$, shown in Figure 2 c). The recharge transistors connecting the differential input are turned off. Assuming that $\overline{D}$ is 0 a boosted E_{p1} transistor will pull QM to 1 regardless of the state of the flip-flop. The low skew inverter will pull $\overline{QM}$ to 0. The E_{p2} transistor will not provide significant current.

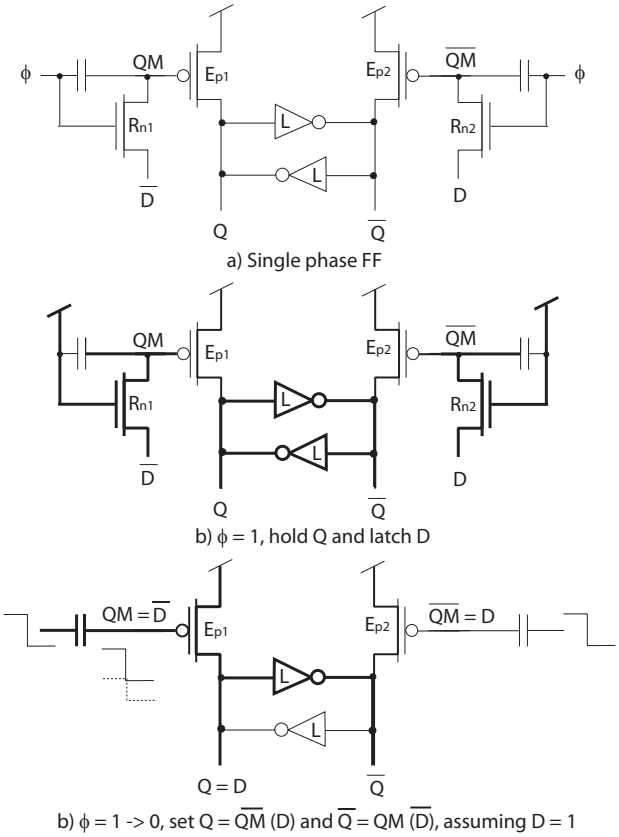

Figure 2: The single phase high-speed ULV Flip-Flop.

3. $\phi = 0$. QM and $\overline{QM}$ will remain more or less stable at the value given in 2. The floating-gates are only affected by leakage currents.

4. $\phi = 0 \rightarrow 1$. Both recharge transistors are turned off by a postive charge provided by the capacitor. The recharge transistors will be turned ON and the latching of the differential input starts.

2.1 Timing Details

Prior to a negative clock edge QM and $\overline{QM}$ needs to be at appropriate levels, i.e. one of the gates of the $E_{p1/2}$ transistors needs to be close to 0V in order to provide a significant boost at the arrival of a negative clock edge. The set-up time is dependent on the recharge transistors, $E_{p1/2}$ transistors and the floating capacitors. The clock to Q delay is given by the boosted $E_{p1/2}$ transistor and the following low-skew inverter that provides the inverted output.

A significant problem with this flip-flop is asymmetrical delay. If $D = 1$ and $\overline{D} = 0$, the output Q responds quickly while $\overline{Q}$ will be pulled down to 0 by the complementary inverter. The difference in time delay will depend on the difference in the current level of transistor E_{p1} relative to a standard CMOS transistor. In practice the difference in delay is more than 10

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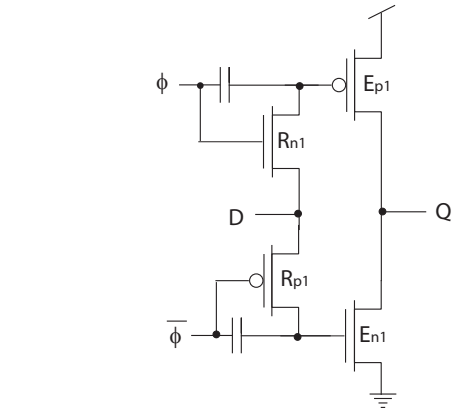
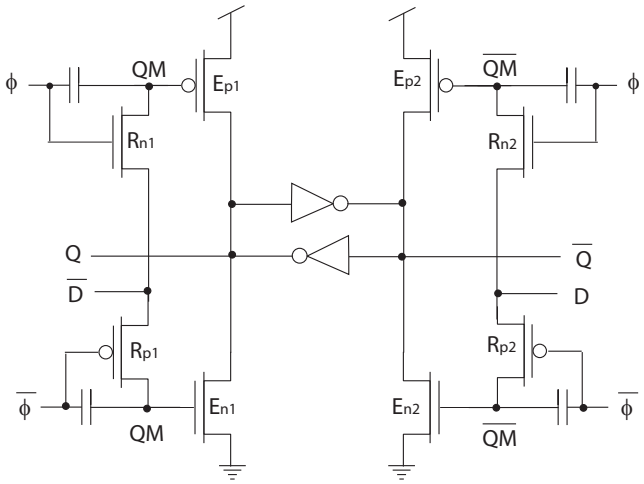


a) Dynamic inverting Latch



b) Differential Flip-Flop

Figure 3: The symmetric high-speed ULV Flip-Flop.

times.

3 Symmetric Differential ULV Flip-Flop

We can use the pMOS master latch in Figure 1 and a similar nMOS master latch to obtain a dynamic inverting latch as shown in Figure 3 a). The latch is transparent when the recharge transistors are ON, i.e. $\phi = 1$. At the arrival of a negative clock edge one of the transistors, the recharge transistors are turned OFF and E_{p1} or E_{n1} will be turned ON and pull Q to $\overline{D}$. The output state will remain until the next $\phi = 1$ phase. The state of the latch may be affected by leakage currents if the frequency is low.

We can utilize the dynamic latch to obtain a symmetric flip-flop as shown in Figure 3 b). The two cross coupled inverters must be able to hold the output state when the latches are transparent and thus make the

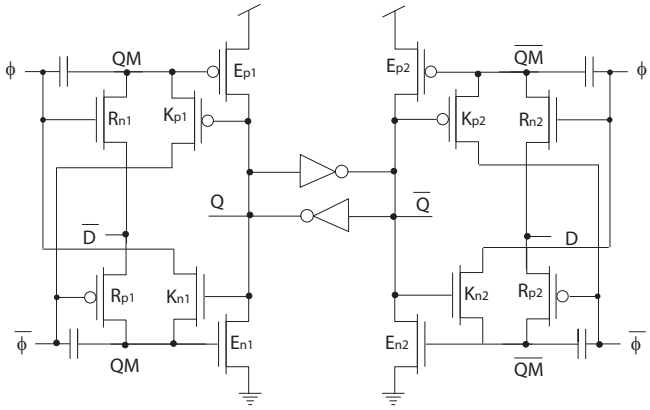


Figure 4: The low-power symmetric high-speed static ULV Flip-Flop.

flip-flop static. Alhough the fip-flop is static the power consumption will be significant when the output is stable after ϕ switches to 0. In order to reduce the static power consumption of the flip-flop and increase the robustness or noise margin, i.e. I_{ON}/I_{OFF}, we can apply additional keeper transistor in a feedback loop as shown in Figure 4. The keeper transistors, labeled K_{n1}, K_{n2}, K_{p1} and K_{p2}, will not be effective when the flip-flop receive a negative clock edge, i.e. ϕ switches from 1 to 0. When $\phi = 1$ the output of the flip-flop is not affected by input changes because the recharge transistors are ON. In this state the input is latched into QM and $\overline{QM}$. When ϕ switches from 1 to 0, two of the evaluate transistors will have a current boost and effectively change the output state depending on the QM state. The cross coupled inverters will not be able to hold the previous value. When the output reaches its new state, two of the keeper transistors will drain the floating-gate of the evaluate transistors that are not contributing. These transistors will be turned OFF properly and the static current running through the evaluate transistors will be reduced to a minimum. The large ratio of I_{ON}/I_{OFF} will effectively increase noise margin and robustness which secures the operation for ultra supply low-voltages. Assume that $\phi = 1$ and $D = 1$, hence $\overline{QM} = 1$ and $QM = 0$, the evaluate transistors E_{n2} and E_{p1} are ready to receive a negative positive ($\overline{\phi}$) and a negative (ϕ) clock edge respectively. The keeper transistors are in the OFF state due to the source voltage applied through the clock signals. When the clock edge is received the increased current in the evaluate transistors will set the output state to $Q = \overline{QM} = D = 1$ and $\overline{Q} = QM = \overline{D} = 0$ regardless of the previous state. The source of the keeper transistors will now be changed. The keeper transistors K_{n1} and K_{p2} will be turned ON due to the new output state and effectively turn off the evaluate transistors E_{n1} and

V_{DD}	t_{cqm}	t_{su}	t_{cq1}	t_{cq2}	t_{cq3}	t_{cq4}	t_{cq5}	t_{cq}	t_{dq}
	ULVX	ULVX	ULV1	ULV2	ULV3	ULV4	UFF	This	NIK.
			18 trans.	18 trans.	24 trans.	16 trans.	32 trans.	16 trans.	26 trans.
$300mV$	$0.096ns$	$0.75ns$	$1.51ns$	$1.19ns$	$1.61ns$	$0.45ns$	$1.40ns$	$0.22ns$	$8.55ns$
$275mV$	$0.24ns$	$1.15ns$	$2.64ns$	$1.53ns$	$2.37ns$	$0.70ns$	$2.44ns$	$0.29ns$	$12.65ns$
$250mV$	$0.46ns$	$2.0ns$	$3.26ns$	$2.41ns$	$4.17ns$	$1.12ns$	$4.10ns$	$0.50ns$	$18.80ns$
$225mV$	$0.72ns$	$2.8ns$	$7.10ns$	$3.94ns$	$7.26ns$	$1.98ns$	$8.24ns$	$0.88ns$	$30.28ns$

Table 1: Timing details and number of transistors for the simulated FFs.

E_{p2}. The static ultra low-voltafe Flip-Flop has been compared with other ultra low voltage Flip-Flops [9] and the Nikolic Flip-Flop[7] as shown in Table 1. As shown in Table 1 the FLIP-FLOP presented is simple, i.e. few transistors, compared to the Nikolic Flip-Flop. In addition the delay, i.e. clock to Q delay is less than $1ns$ for supply voltages $\geq 225mV$. The data to output delay of the Nikolic Flip-Flop is close to ten times the setup plus the clock to output delay of the flip-flop presented in this paper.

4 Conclusion

In this paper we have presented high-speed ultra low-voltage static flip-flops and a dynamic latch. The latch and flip-flops are designed for ultra low voltage digital systems, i.e. supply voltages down to approximately 0.2V. The differential static Flip-Flop presented is close to 10 times as fast as the Nikolic flip-flop and offers an increased noise margin due to the large ON and OFF current ratio.

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