Thermal Analysis of a high power LED multi-chip Package Module for Electronic Appliances

Bor-Jang Tsai, Sheam-Chyun Lin and Wei-Kuo Han

***Abstract*—**By using multiple high-power LEDs in products, some difficulties occur in predicting the temperature distribution because of the interaction of heat generated by each single-chip LED in the same module. To determine the heat dissipation of a multi-chip LED module, solid physical models for both single-chip and multi-chip LEDs with cooling fins were constructed. Simulation of the temperature distribution under natural convection was conducted using numerical analysis and by introducing formulas to estimate change in heat resistance. In addition to elucidating the heat dissipation of multi-chip LED modules, this study attempts to identify the major factors affecting the temperature distributions of LEDs.

Simulation results from the finite element program indicate that expressing the temperature distribution of a single LED chip using a spherical coordinate system is appropriate. The temperature curve of a copper plate away from the chip is nonlinear since the distribution curve declines dramatically and is no longer linear. The temperature of a multi-chip LED module is slightly less than that of linear superposition. A comparison of the estimated value for a multi-chip LED with the simulation result confirms the practicability and accuracy of the proposed thermal resistance formula in this work. This study provides reference data for estimating of thermal resistance in a multi-chip module.

***Keywords*—**LED(Light Emitting Diode), Heat dissipation, Thermal resistance

Vortex

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I. INTRODUCTION

Most conventional Light Emitting Diode (LED) chips are small, approximately 0.16mm^2 in area and 0.11mm thick with 20mW input power and a low luminance level. Since 2000, the luminance efficiency of LEDs has increased and high-luminance LEDs have been developed. However, single-chip LEDs are insufficient as a light source. Thus, multi-chip modules are used currently. The advantages of an LED as a light source are single-color light emission, colorfulness, wide color range, no ultraviolet rays, small volume, light weight, and no environmental issues. However, an LED still has the disadvantage of inadequate luminance efficiency resulting in low LED light levels. Regular luminance requires hundreds to thousands of lumen. Conventional small chips fall far short of this luminance level. Currently, luminance is achieved using a large multi-chip array of LED chips. Conversely, use of a multi-chip high-power LED package is likely to produce a temperature exceeding 100^{o}C. Notably, thermal dissipation is difficult. Although an LED is a cold light source, luminance efficiency is currently low. These high temperatures decrease LED luminance efficiency and its capacity to emit light. Additionally, its lifespan is also greatly reduced. Therefore, the thermal resistance of an LED light module has a determining effect on product quality.

Using the definition and model of single-chip package thermal resistance in a multi-chip module remains difficult. Sofia [1] hypothesized that a heat source is available on a sectional thermal rod (conductor). Both ends of the thermal rod have fixed temperatures and the remaining parts are thermally insulated. The temperature distribution of a thermal rod is inversely linear distance from the heat source. Therefore, the principle of the heat transfer superposition model is established, which is represented by a thermal resistance matrix to account for insufficiencies of traditional thermal resistance analysis. This hypothesis cannot be applied to multi-chip LED modules because multi-chip LED thermal-dissipation base plates are generally not strip-shaped and contain heat sinks for convection. Nevertheless, interface temperatures measured for each chip coincide with theoretical basis of superposition in thermal conduction. Kim et al. [2] used instruments to measure the thermal resistance of multi-chips and substitute this thermal resistance into the superposition principle based upon the thermal resistance matrix. Thermal resistance system is then subdivided into LED chip thermal resistance and thermal resistance of the thermal dissipation base plate. When thermal resistance of the chip is significantly higher than the thermal resistance of the base plate dissipating into environment, the ratio of both is 10:1. As the number of chips increases, thermal resistance decreases. When the ratio of number of chips increases to thermal resistance is 1:1 or 1: 10, the number

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of chips has almost no effect on thermal resistance. The experiment in this study does not contain heat sink package modules. When tens to hundreds watts from a high-power LED chip package module are applied, the condition changes and such approach is infeasible. Thus, analysis of LED multi-chip applications for high-power LED multi-chip products is necessary. Thus, this study simulates a model with heat sink and discusses process in detail. Experiments will be performed next year.

Methods and analysis related to the application of the electrical method for junction temperature measurement applies thermal characterization of packaged semiconductor devices. This study is essential for anyone involved in the collection, interpretation, or application of semiconductor component thermal data, not only those in the LED industry but also those of developing new products such as high- frequency and high power devices with a total power dissipation of energy for a clock frequency of 200MHz and gate power switching requirement of 0.15 μW/NG/MHz [3]. Sikka, et al. identified the thermal and mechanical challenges of a multi-chip module (MCM) used in a high-end computer system. The chip and thermal paste carrier for an IBM MCM package [4]. A futuristic microprocessor package uses micro channels and an embedded thermoelectric device [5]. An innovative concept based on Advanced Thermal Solutions minimizes spreading resistance by using a Forced Thermal Spreader (FTS) in a BGA package [6] Along with optimizing spreading resistance, thermal transport must be managed to dissipate high heat fluxes in electronic devices. Such an example is provided by Colgan, et al. [7]. In their application, the chip operated at 400 W/cm^2. Micro channels were fabricated inside the package, for the required cooling during chip operation.

Therefore, analysis of multi-chip applications for high-power multi-chip products is necessary. In Year 2007, Sofia [8] used of thermal resistance measurements [9-11] and combined methods and analysis related to application of the electrical method for junction temperature measurement to thermally characterize packaged semiconductor devices, including using thermal transient data [12-15] to build the electrical thermal resistance measurements for hybrids and multi-chip packages. However, the illuminations of LEDs vary with junction temperature variation due to self-heating of LEDs and variation of ambient temperature. Hence, the thermal effect will affect both illumination intensity and output color of LED. Masana [16] derived a RC thermal model for a general semiconductor package. Muthu et al. [17] proposed a constant luminous model which ignores the thermal effect. Farkas et al. [18] developed a thermal model for luminous output and thermal I resistance in monochromatic light-emitting unit. Huang et al. [19, 20] derived a system dynamics model of a luminaire to relate the energy input to LED junction temperature.

II. OBJECTIVES OF ANALYSIS

First, this study focused on simulating the thermal resistance of an LED single-chip package, and the temperature distribution of an LED chip with a heat source on a copper plate. Error in thermal conduction of spherical coordinates was calculated. Then, the input power of this thermal resistance simulation of an LED single-chip package is divided into three levels, three various power inputs. Whether the temperature of an LED chip with the same position and structure as thermal resistance coincides with the superposition principle is discussed. Finally, four LED chips are arrayed at 2x2 pitches. Only one LED chip is illuminated to calculate thermal resistance based on the pitch between the copper plates. The four LED chips undergo linear temperature superposition, and then compared with four simulated LED chip temperatures when all are illuminated to verify the predicted accuracy of the four LED chips at 2x2 pitches.

A. Simulation of the CFdesign program

Single-chip LED illuminated with different power inputs.To verify CFdesign this program, a flat copper plate with four edge surfaces at 25^{o}C, top and bottom surfaces are insulated based upon Sofia's hypothesis (LED chip as point heat source without heat sink) was simulated and compared with the heat transfer calculation using spherical coordinates. This program is feasible for analyzing this LED multi-chip package module problem (Fig. 1). To verify whether the superposition principle model is suitable for LED chip cases, an LED single-chip is input with different powers to determine whether the temperature distribution is linearly proportion with respect to distance from top to bottom.

Multiple LEDs illuminated separately at a fixed LED pitch distribution.Although the package module has four LEDs, if the LEDs are arrayed symmetrically (Fig. 2), only one needs to be illuminated to determine temperatures of the other LEDs. The temperature difference between the LED chip interface and environment is utilized to calculate the temperature superposition and attain the final temperature of each chip when all four chips are illuminated simultaneously under the same power. The four chips illuminated simultaneously under the same power are simulated for verification.

Each LED chip in the package module is heated by current. According to thermal conduction theory, as the distance of an LED chip from a neighboring LED increases, the temperature drop increases. That is, the self-heating LED chip and the thermal effects of neighboring LED chips determine final temperature. Taking the four LED chips at 2x2 pitches as an example, the regular matrix distance is fixed at 8mm. This distance is the best choice discussions related to multi-chip temperature.

B. Establishment of the finite volume model and hypothesis

The CFdesign is adopted for finite element calculation of heat transfer. Temperature and heat flux of an LED chip module are also calculated.

Structure of and material in the chip module, notably, LED chips sized 1mmx1mm are typically studied. A blue sapphire 0.1mm thick in GaN chip structure is used to represent the current model (Fig. 2). The top surface of the structure 0mm in thick is the heat source surface

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setting that simplifies the heat source of the 5μm-thick epitaxial layer. Transparent silicone package material measuring 2 mm thick covers the LED chip to protect the chip and for light conduction. The base of the blue sapphire is attached to the copper plate. The copper plate is a commonly sold in markets. Size of it is simplified into a rectangle measuring 20mm long 20mm width, and 2mm thick. The copper plate dissipates heat. Heat is also conducted to the copper fin below it. Natural convection between the copper fin and atmosphere helps module thermal dissipation. Table lists the properties of materials.

Boundary conditions: Electrical power (1W) is considered when the model comes to input luminance. The Internal Quantum Efficiency (IQE) is 20%; the remainder, 0.8W, is released as heat. As luminance surface of the LED epitaxial layer down when the heat sink faces upward. The atmospheric temperature is set at 25 °C for natural convection. The computational domain of the LED light module is surrounded 7-times by the entire atmospheric layer as the simulation condition of natural convection.

C. *Equations for calculating thermal resistance between chips*

We assume the total thermal resistance of modules in a chip package is as follows:

$$R_{total}=R_{die}+R_{bonding}+R_{base}+R_{fin}+R_{fin-ambient} \quad (1)$$

which, R_{die} : LED chips thermal resistance,

$R_{bonding}$: Die layer thermal resistance,

R_{base} : Copper plate thermal resistance,

R_{fin} : Heat sink thermal resistance,

$R_{fin-ambient}$: Heat sink to atmospheric thermal resistance (thermal convection).

Although each LED chip does not heat up itself, neighboring LED chips will also be heated. However, the longer pitch distance, the less likely it is for neighboring LED chips to be affected. Thus, the chip pitch thermal resistance of LED multi-chip R_{pitch} is as shown in Fig. 3. Assuming LED chip area is small as compared to the entire package module, it may be regarded as a point heat source. Thermal conduction resembles a sphere that conducts heat outwards. The equation of pitch thermal resistance value for LED chip on copper plate surface may be estimated using spherical coordinates. It is inferred as follows:

Thermal conduction equation of spherical coordinates(r, Φ, and θ)

$$\frac{1}{r^2}\frac{\partial}{\partial r}\left(kr^2\frac{\partial \mathrm{T}}{\partial \mathrm{r}}\right)+\frac{1}{r^2\sin^2\theta}\frac{\partial}{\partial\phi}\left(k\frac{\partial \mathrm{T}}{\partial\phi}\right)+\frac{1}{r^2\sin\theta}\frac{\partial}{\partial\theta}\left(k\sin\theta\frac{\partial \mathrm{T}}{\partial\theta}\right)+\dot{q} \quad (2)$$
$$=\rho c_p\frac{\partial T}{\partial t}$$

Sphere radius r: internal radius is expressed as r_1 and external radius is expressed as r_2. Under a static condition, when the thermal conduction material is homogenous and isotropic and when the Azimuth angle Φ and polar angle θ are symmetrical structure. The simplified Eq. (1) is:

$$\frac{d}{dr}\left(r^2\frac{dT}{dr}\right)=0 \quad (3)$$

The integral solution is,

$$T(r)=\frac{a}{r}+b \quad (4)$$

Boundary conditions: heat flux is set as q_1" at $r=r_1$ and the heat source is the internal sphere surface. Temperature is set as T_2 at $r=r_2$ to define the temperature of the external sphere surface.

Fourier's Law:

When the heat source is at r_1

$$q_1''=-k\frac{dT}{dr}\Big|_r=r_1 \quad (5)$$

$$a=r_1^2\frac{q_1''}{k} \quad (6)$$

$$b=T_2-\frac{q_1''r_1^2}{k}\frac{1}{r_2} \quad (7)$$

Substituting Eq. (5) ~ Eq. (7) into Eq. (3) to yields

$$T(r)=\frac{q_1''r_1^2}{k}\left(\frac{1}{r}-\frac{1}{r_2}\right)+T \quad (8)$$

Thermal resistance is

$$R_{th}(r_1-r_2)=\frac{T_1-T_2}{q_1}=\frac{r_1^2}{A_1k}\left(\frac{1}{r_1}-\frac{1}{r_2}\right) \quad (9)$$

III. RESULTS AND DISCUSSIONS

Based on simulation results, this study determines whether the temperature distribution is coincident with the linear superposition principle. Finally, four LED chips arrayed at a 2x2 *pitch* are used to ensure temperature prediction accuracy.

A. *Temperature depression curve is nonlinear*

After obtaining numerical simulation results of a single LED-chip, heat sink possesses geometric structural direction (Fig. 4). The direction of heat sink is expressed as vertical direction (V) while the other direction is expressed as parallel direction (P). Therefore, the contribution ratio of thermal conduction is higher compared with thermal convection (Figs. 5 and 6). However, the area of the LED from center to outer periphery is roughly 4mm, and has a symmetrical temperature distribution. This symmetrical temperature distribution is caused by the 2mm-thick copper plate and the 0.3mm-thick heat sink. They conducted heat symmetrically to the outside in a hemispherical manner.

After obtaining Eq. (8) results for thermal conduction of spherical coordinates (denote cal) and numerical simulation results of a single LED chip, the temperature decline is consistent with that of analytical calculation (Fig. 7). In other words, the heat sink has certain physical effects in thermal conduction. Nevertheless, since thermal convection is involved, the thermal dissipation mechanism is complex and requires further study.

B. *Linear superposition of copper plate temperature at the same position as below the LED*

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After simulating results for three LED single-chip watt settings, the temperature of the copper plate below the LED (0.8mm) minus the environment temperature of 25°C serves as basis for reference. The 1/2-fold and 2-fold temperatures are added to the environment temperature to obtain results of copper plate temperature distributions of numerical simulation (by the superposition principle) and analytical calculation by the Eq. (8) for a LED single-chip package module under different powers (Fig. 8). Although these results may deviate by 2~7°C, estimation results still serve as reference. Among analysis, higher watts tend to result in overestimation of calculation values, because the temperature difference between fins of the heat sink and the atmosphere increases, heat dissipation increases, and the yielded temperature decreases to achieve thermal equilibrium.

C. Thermal resistance comparison between a chip with and without attached soldering tin at same position of an LED chip

Thermal resistance of a LED single-chip is simulated. The temperature differences between the LED (heat source) top surface and bottom surface, both attached soldering tin copper plate. They are consistent with calculated values by equations of formulas. Consequently, the thermal resistance yielded by equations of 1-D spherical coordinates is suitable for use for LED temperature predictions.

D. Comparison of thermal resistance by numerical simulation and analytical estimation between an LED multi-chip

In terms of thermal resistance of the entire LED chip module, the heat sink is subject to the greatest natural convection heat resistance *R(fin-a)*. The four LED chip symmetrical case shows that if one LED chip temperature can be measured, the thermal resistance equation can be used to calculate the temperature difference between the chip and copper plate (Fig. 2). The thermal resistance value from the first LED chip luminance surface to the second LED chip luminance surface is calculated as

$$R_{j1-j2} = R_{die1} + R_{bonding1} + R_{pitch}\left(= R_{th}\left(r_1 - r_2\right)\right) + R_{bonding2} + R_{die2} \quad (10)$$

When the heat source of LED chips is expressed as die1, based on result of one of the 0.8W chips, the heat flux of the contact surface between the LED and resin is only 0.0029W. This heat flux is negligible as it is too small. We hypothesize that all power is conducted from die1 to the copper plate and the thermal resistance of the pitched copper plate below of the first LED chip to the copper plate below the second LED chip; thus R_{pitch} is calculated by Eq. (9). When heat is conducted to die2, the thermal dissipation area of this LED is negligible as it is too small. The heat flux shows that the attached soldering tin heat flux below the non-heat source LED chip is negligible as it is too small. Therefore, the contribution of this thermal resistance can be neglected. Thus, Eq. (10) is expressed as

$$R_{j1-j2} \fallingdotseq R_{die1} + R_{bonding1} + R_{pitch} \quad (11)$$

Calculations for the symmetrical four LED chips at 2x2 pitch array are as follows :

$R_{j1-j2} = 3.492 + 1.222$

$R_{j1-j3} = 3.492 + 1.245$

$R_{j1-j4} = 3.492 + 1.222$

ΔT_{p2} = Temperature difference between horizontal chips

ΔT_{p3} = Temperature difference between adjacent chips

ΔT_{p4} = Temperature difference between vertical chips

$\Delta T_{p2} = \Delta T_{p4} = R_{j1-j2} \times Q = 3.77°C$

$\Delta T_{p3} = 3.79°C$

In this study, since the 8mm distance between two LED chips markedly exceeds cooper plate thickness and fin thickness (2.3mm), the temperature difference is overestimated and requires further study. In the same package, the interface temperature (T_{j1}) of input power of one LED chip is measured. Then, Eq. (11) calculates the four LED chips with the same simultaneous input power as results. The 4-fold watts greatly exceed the original 1-fold watts. Therefore, the junction interface temperature difference of 20°C at 111.9°C (numerical simulation) and 132.07°C (superposition calculation) is produced (Fig. 9). Although the single LED chip is overestimated, we infer to be attributed to the temperature difference between junction and heat sink. It is especially true for heat sink and atmospheric temperatures. The higher temperature difference between junction and heat sink is, the higher cooling efficiency will be. Therefore, the error in temperature calculated by superposition is related to heat generation of the high power. As the power increases, the likelihood of overestimating calculation will be. In the future, factors contributing to this error be examined to ensure accurate estimations

In view of the above results, it shows that the thermal resistance of different LED chip packages varies and that thermal dissipation devices (copper plates and heat sinks) have different mechanisms, therefore, thermal dissipation need to be calculated separately. The Eq. (10) is used to calculate the thermal resistance of the LED multi-chip to obtain the temperature of the LED multi-chip. Eq. (10) is expressed in matrix below:

$$\left(\left[R_{die}\right] + \left[R_{bonding}\right] + \left[R_{pitch}\right]\right) \times \left[Q\right] = \left[\Delta T_{junction-base}\right] \quad (12)$$

Thermal convection $R_{fin-ambient}$ will be incorporated in the calculation in the future to derive accurate estimations.

IV. CONCLUSIONS

Due to superposition of the LED multi-chip thermal distribution, calculation of heat dissipation becomes difficult. Arrangement of thermal management will likely increase difficult too. After systematic parameter analysis, we have increased knowledge of LED multi-chip package properties. Conclusions are summarized as follows.

(1) Simulation results for LED chip thermal dissipation indicate that the copper plate temperature depression curve distance away from the chip is non-linear.

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(2) Under different powers, the temperature of the copper plate below the LED is feasible for superposition principle. Analytical estimation using addition is acceptable; however, as power inputs increases, calculated values will be overestimated. In this study, the interface temperature (T_{j1}) of input power of one LED chip is measured. Then, analytical calculates the four LED chips with the same simultaneous input power. The 4-fold watts greatly exceed the original 1-fold watts. Therefore, the junction interface temperature difference of 20°C at 111.9°C (numerical simulation) and 132.07°C (superposition calculation) is produced. The percentage of deviation is approximately 10%.

(2) Calculating the thermal resistance of 1-D spherical coordinates is suitable for use in predicting temperature differences in an LED structure.

(3) When the thickness of a copper plate is limited, LED multi-chip pitch thermal resistance of the copper plate can be calculated using equations of thermal resistance in 1-D spherical coordinates; however, the high wattage tends to result in overestimation of calculated values of thermal resistance.

(4) Comparison between the thermal resistance estimation and numerical simulation of LED multi-chip pitch shows that thermal resistance of an LED chip combined with a thermal dissipation copper plate should be calculated separately. The equation of thermal resistance is valuable as a reference.

V. ACKNOWLEDGEMENTS

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Figures

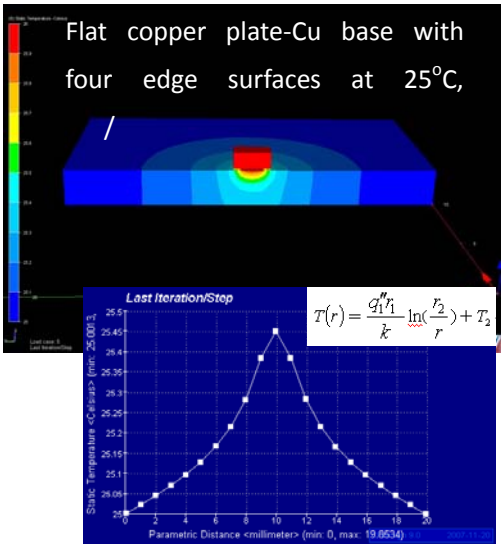


Fig. 1 Flat copper plate-Cu base (LED chip as a point heat source without a heat sink) the heat transfer calculation using spherical coordinates.

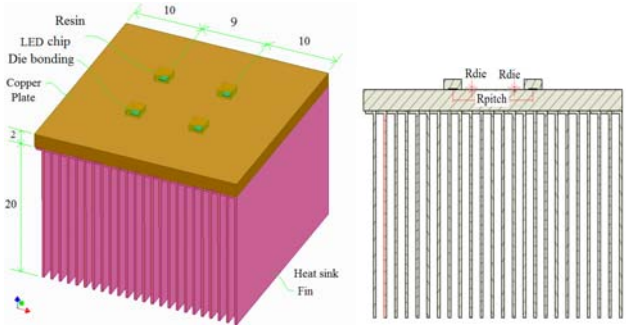


Fig. 2 Geometrical dimensions and materials of an LED 4-chip package module

Fig. 3 Schematic diagram of thermal resistance of an LED 4-chip package module

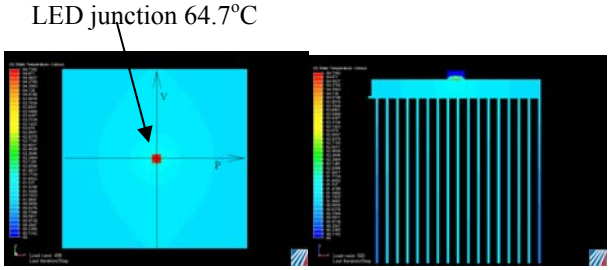
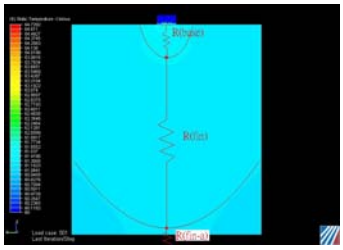


Fig. 4 Geometrical structure direction and temperature field of an LED single-chip package module (top view)

Fig. 5 Temperature field of an LED single-chip package module (front cross-sectional view)

$$T(r) = \frac{q_1'' r_1^2}{k}\left(\frac{1}{r} - \frac{1}{r_2}\right) + T_2$$



$$R_{th}(r_1 - r_2) = \frac{T_1 - T_2}{q_1} = \frac{r_1^2}{A_1 k}\left(\frac{1}{r_1} - \frac{1}{r_2}\right)$$

Fig. 6 Temperature field and analog circuit of thermal resistance for an LED single-chip package module (side view)

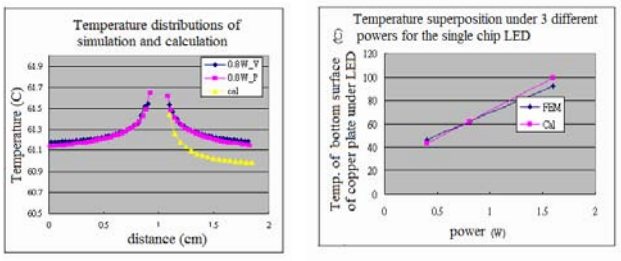
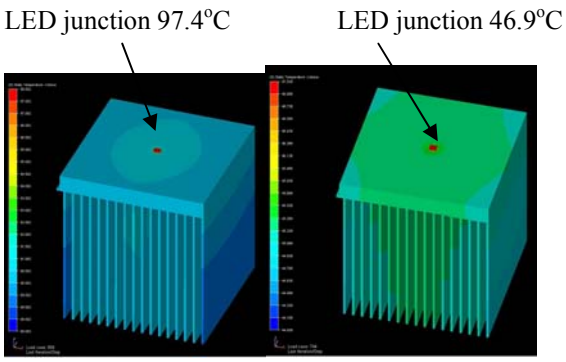


Fig. 7 Copper plate temperature depression curves by numerical simulation and analytical calculation by Eq. (8) for an LED single-chip package module



Single-chip LED 1.6W Single-chip LED 0.4W

Fig. 8 Copper plate temperature distributions by numerical simulation (via the superposition principle) and analytical calculation by Eq. (8) for an LED single-chip package module under varying power.

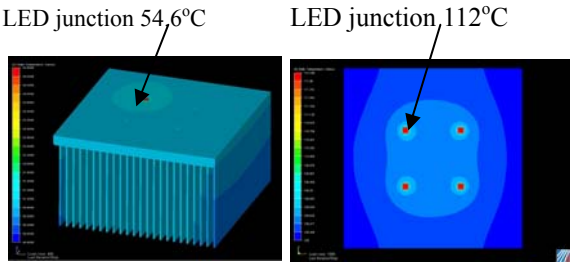


Fig. 9 Junction interface temperature distributions of a single-chip module and an LED 4-chip package module

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