

An Improvement in the “Virtually Isolated Transformerless Off - Line Power Supply”

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Abstract: – This paper describes a circuit improving the “Virtually Isolated Transformerless Off - Line Power Supply”, presented in a previous publication [1]. The circuit, in reference, used a new method of isolation between ac mains and dc voltage output. It consisted of two Buck converters connected in series, each one using a pair of MOSFET transistors. Each pair of transistors was conducting at different time intervals - this under the assumption that the impedance of an OFF state MOSFET is practically infinite - there is transfer of energy from the ac side to the dc without actual ohmic continuation in the circuit. If the maximum limit of the drain to source voltage is not exceeded, the power supply is virtually isolated, making the transformer in classic power supplies redundant. The circuit in reference however, had limitations at the maximum output voltage, as each Buck converter gave a maximum output voltage half of the input voltage. As a result, the maximum practical limit of the output voltage for operation from $230 \pm 10\%$ Volt mains supply was 54 Volts dc. Dealing with this problem in the present study, the freewheeling diode and large inductance of the first Buck converter are substituted by a diode in antiparallel with a small inductance whose function is to limit the rate of charging current to the capacitor which provides the energy to the output buck converter. The outcome of the changes above is the production of a much higher output voltage and higher efficiency. The analysis and derived simulated results of the proposed circuit are cited in this paper.

Key-words: - Power supply, Buck converter, transformer, voltage isolation, transformerless isolation, high efficiency power supply.

1 Introduction

Traditionally, the isolation of power supplies was achieved by using a transformer. A previous publicized study introduced an Off Line dc power supply, which make the large impedance of OFF state MOSFETs equal the impedance between the ac and dc side. The circuit consisted of two Buck converters, connected in series, each one using a pair of two MOSFET transistors as shown in Fig.1.

There were four repeated modes in steady state operation.

Mode I

Tr_1 and Tr_2 closed with Tr_3 , Tr_4 opened. Capacitor C_3 is charged through L_5 and $Tr_1 - Tr_2$.

Mode II

Tr_1 and Tr_2 are open with Tr_3 , Tr_4 open. Current freewheels through L_5 , D_7 , C_3 keeping the voltage variation of C_3 at low levels.

Mode III

Tr_1 and Tr_2 are open with Tr_3 , Tr_4 closed. Capacitor C_4 is charged through the partial discharge of capacitor C_3 , which also increases the energy stored in L_8 .

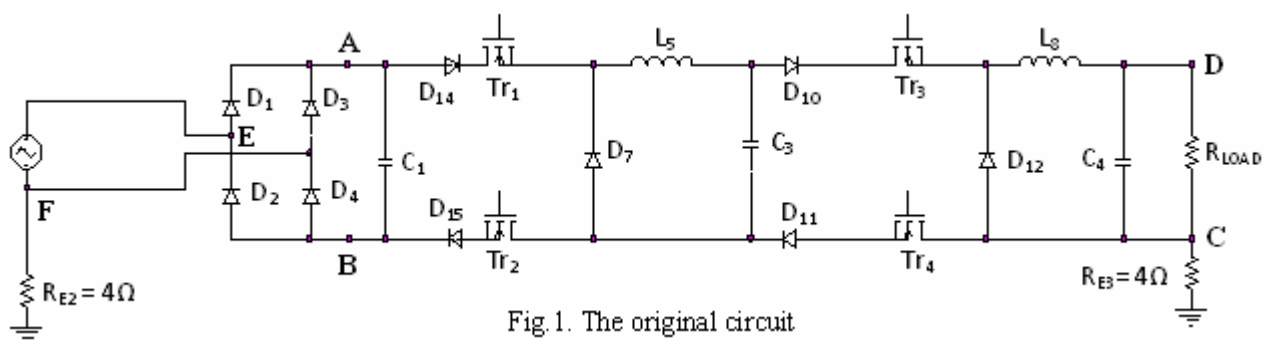


Fig.1. The original circuit

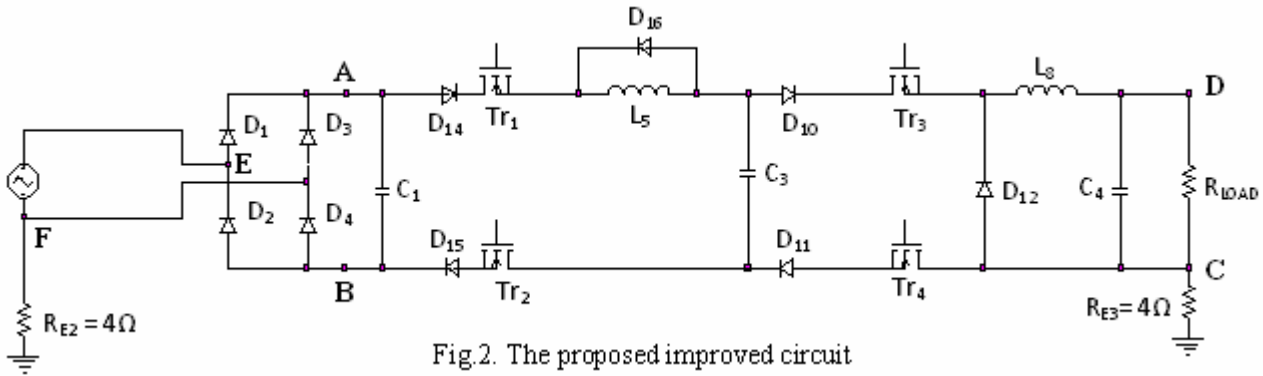


Fig.2. The proposed improved circuit

Mode IV

Tr₁ and Tr₂ are open with Tr₃, Tr₄ open. Current freewheels through D₁₂ and L₈, keeping the load voltage variation at low levels.

Since there is no simultaneous conduction between the two pair of MOSFETs Tr₁ - Tr₂ and Tr₃ - Tr₄, the impedance between ac mains input and dc output is equal to the impedance between Drain – Source of two non conducting MOSFETs.

In the present study, an improvement has been made to the above initial circuit. The new proposed circuit is shown in Fig.2.

The transistors Tr₁ – Tr₂ (Fig. 2) that used to form the first Buck converter are now operating as switches charging C₃ through the inductance L₅. The function of the inductance is to improve the form factor of the current charging C₃, thus minimizing the power losses in Tr₁ – Tr₂. The action of diode D₁₆ is to freewheel the current in case that capacitor C₃ is not fully charged by capacitor C₁, when transistors Tr₁ – Tr₂ are open.

2 Circuit design and operation

A theoretical model of the proposed circuit has been developed in ORCAD environment. Due to the absence of a transformer and operation with higher output voltage, high efficiency at higher power is anticipated. The purpose of this design is to produce an output stabilized voltage at high powers and show the principle of operation, rather than producing an optimized power supply, where all factors – such as optimized control, soft starting, current limiting and suitably optimized values of components – are taken in to account.

The requirement of the theoretical model is to produce a circuit fed by the mains supply with $230 \pm 10\%V_{RMS}/50Hz$ giving an isolated output of 100V/20A/2000W.

Apart from the standardized ORCAD components, such as the MOSFETS used (IRFP 360)-three in parallel to form each transistor, diodes (MUR 1560), the PWM control integrated circuit (SG 1525A/25C) and the bipolar transistors (BC 546A), assumed

values of the resistive lossy components of the inductors and capacitors are taken into account, approaching realistic values of laboratory components.

The general circuit layout is shown in Fig. 2, with the actual circuit developed in ORCAD which is not shown in the present work due to its complexity. The use of diodes D₁₀, D₁₁, D₁₄, and D₁₅ is necessary due to the earth loop of the supply. This earth loop is created because the neutral of the mains supply is usually earthed. Thus considering Fig. 2, point F is the reference voltage of about zero Volts. Point E perturbrates between the positive and negative of maximum mains voltage with points A and B following this perturbation. If we consider that points C or D at the output are earthed or earthed through a resistance such as a human’s body, current will flow from the output to points A or B through the antiparallel diodes integrated in all MOSFETS. Diodes D₁₀, D₁₁, D₁₄, and D₁₅ are blocking this current.

2.1. PWM Control

The control method is based on the integrated circuit 1525A shown in Fig. 3.

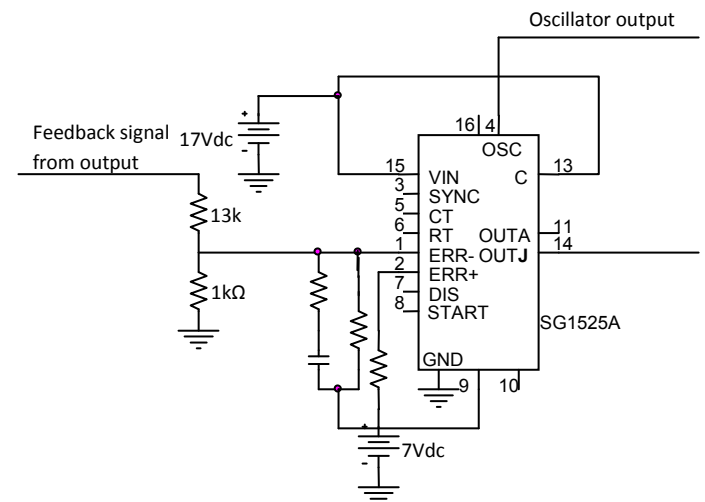


Fig.3. PWM control circuit

Here, the output J is used to produce the two pulses driving the two pairs of MOSFETs ($Tr_1 - Tr_2$ and $Tr_3 - Tr_4$). The first pulse drives directly the circuit of Tr_3 and Tr_4 and, being modulated, produces the constant load voltage. The pulse driving the other pair of input MOSFETs must be in antiphase with the previous one, and for reasons of stability, must have constant maximum width of 50% of the period which the 1525a operates. These requirements are satisfied by the circuit shown in Fig.4.

The antiphase nature of the pulses is achieved via the circuit shown in Fig.4. The pulse derived from output J is differentiated through C_5 and R_9 . R_{10} and R_{11} bring the amplitude of this pulse to appropriate voltage levels, feeding the clear input of the counter 74HC193. This zeroes all outputs of the counter. The clocking of this counter is provided by the oscillator output of the 1525A circuit. The oscillator output is independent of the 1525A control circuit and always gives two pulses of short duration during one period, so that even if output J is zeroed due to current limiting or other reasons, the oscillator output will provide the inverter 74HC04 with a pulse. The inverter output is fed to the UP count of the counter, driving the output A of the counter high. Here, it must be noted that the clear input of the counter, needs only to be applied once, since odd number of pulses will drive output A of the counter high and even number of pulses will drive the output low. While, Fig. 5 shows waveforms in various parts of the antiphase circuit.

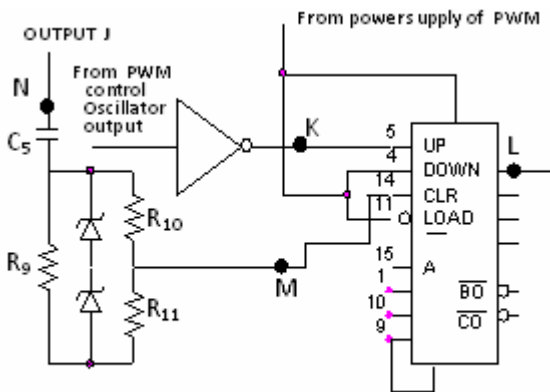


Fig4. Antiphase circuit

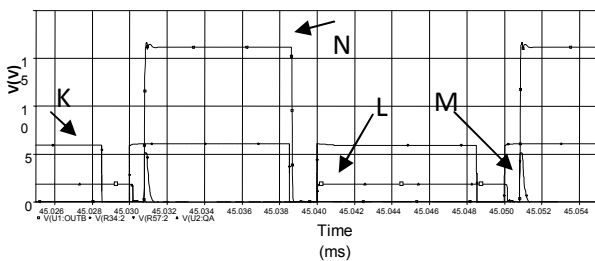


Fig5. Voltage waveforms at various points of the antiphase circuit.

2.2 Transistor drive circuits

The requirement is to drive the MOSFETs through four isolated circuits, two for every MOSFET pair. Two identical drive circuits were designed as the one shown in Fig. 6. Fig. 7 shows the waveforms of the pulses applied to the drive circuits and Gate to Source voltages of transistors Tr_1 and Tr_2 .

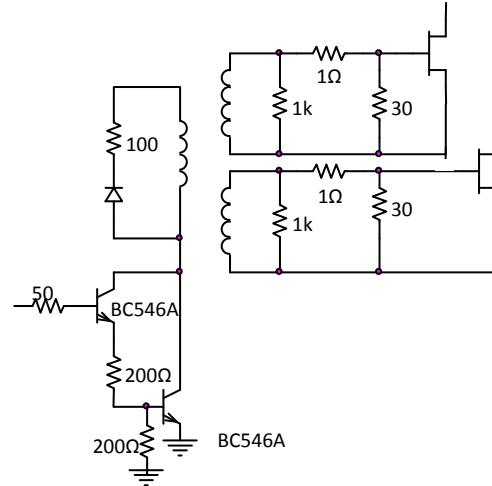


Fig.6. MOSFETs drive circuit

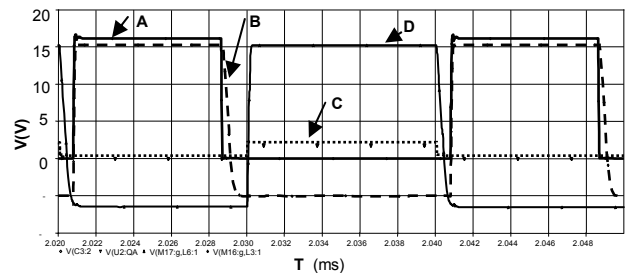


Fig.7.

A: Pulse input to driver of Tr_1 B: V_{GS} of Tr_1
C: Pulse input to driver of Tr_3
D: V_{GS} of Tr_3

2.3 Snubbers

Due to the high values of current spikes, two snubbers were necessary for improving the circuit operation. The first is concerning the charging of capacitor C_3 with the schematic being as in Fig.8. The second concerns the diode D_{12} with the schematic being as in Fig.9.

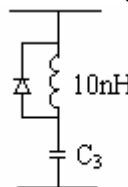


Fig 8.

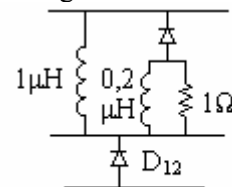


Fig.9.

3 Simulation results

There are two distinct modes of operation depending on whether the output is earthed or not. Earthing has a significant impact on voltage stress of MOSFETs and insignificant effect on all other parameters. Thus, there are three sets of results taken through repeated runs made on the theoretical model. The first set is for common parameters concerning both modes of operation, the second is for voltages appearing across the MOSFETs for unearthed output and the third for voltages with earthed output.

The requirements of this power supply is to produce a circuit operating from $230 \pm 10\%$ Volts mains supply, giving a regulated dc output of 100 Volts/ 20 Amps/ 2000 Watts. As the voltage stress of the components is of major importance, it was decided to produce results for operation from an ac supply of $230 + 10\%$ Volts or 253 Volts RMS giving an output current of 20 Amps.

The final values of the major power passive components in connection to fig. 2 were:
 $L_3 = 100 \text{ nH}$ which can be formed practically by a single turn of wire on a toroidal core.

$C_3 = 30 \text{ }\mu\text{F}$ non-electrolytic due to the high ripple current

$C_1 = 1410 \text{ }\mu\text{F}$, $L_8 = 100 \text{ }\mu\text{H}$, $C_4 = 660 \text{ }\mu\text{F}$

Fig. 10 and Fig. 11 show the stabilizing effect of the voltage control loop. The output voltage ripple does not exceed $\pm 0,15\%$.

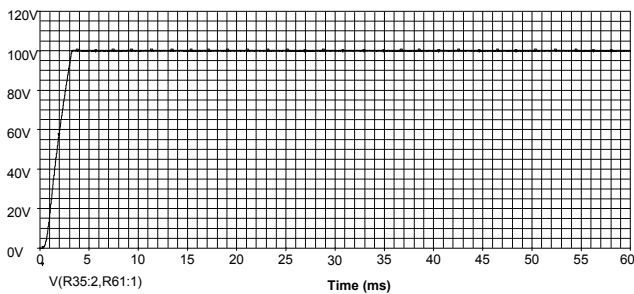


Fig.10. Regulated output voltage.

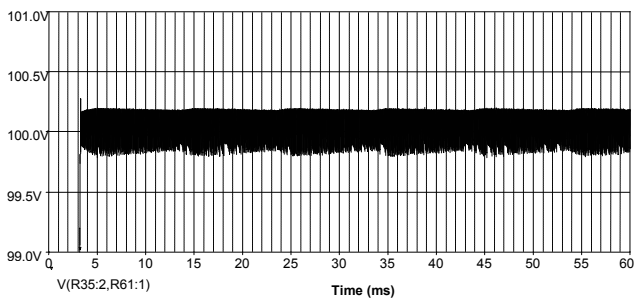


Fig.11. Output voltage at higher resolution.

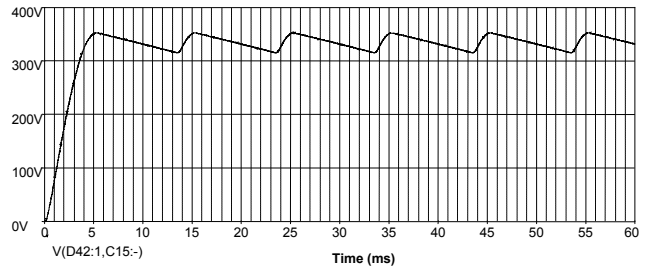


Fig.12. Voltage at capacitor C_1 .

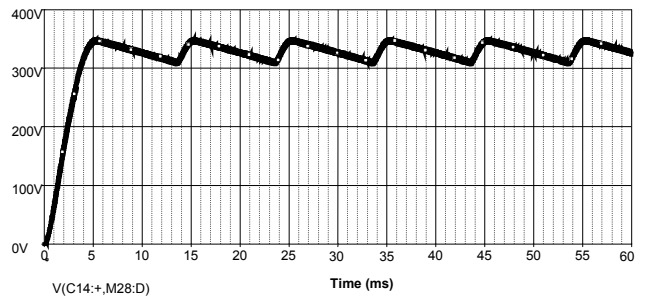


Fig.13. Voltage at capacitor C_3 .

The positive values of current in capacitor C_3 , as shown in Fig. 14, represent its charging from capacitor C_1 , while the negative values show its discharge.

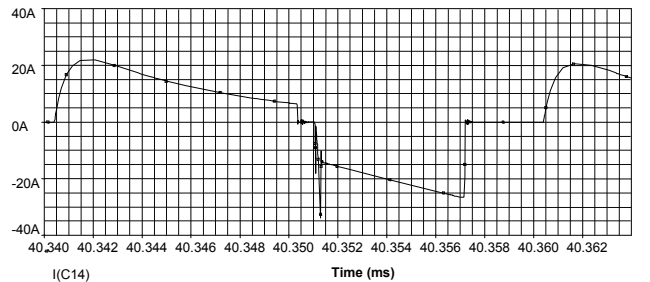


Fig.14. Current in capacitor C_3 .

The current in diode D_{12} , as shown in Fig. 15, is a typical waveform of the freewheeling current in a Buck converter.

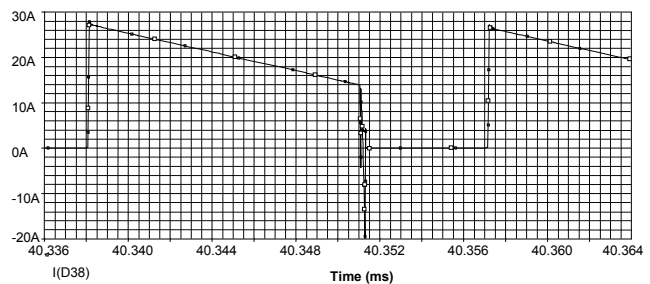


Fig.15. Current in diode D_{12} .

The voltage between Drain and Source of transistor Tr_1 , as shown in Fig. 16, for unearthed output, does not exceed 10 Volts and is identical to the voltage across Tr_2 . The small value of this voltage is due to the voltage drop of MOSFETs $Tr_1 - Tr_2$, small inductor L_8 , and is the difference between the waveform shown in Fig. 12 and that shown in Fig. 13.

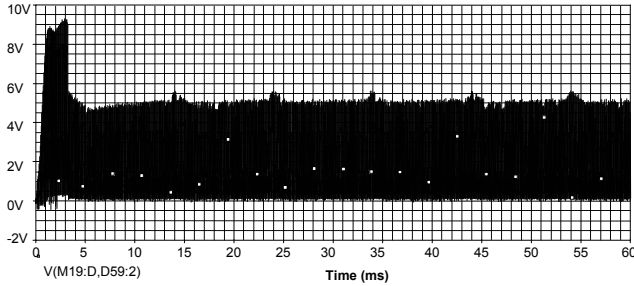


Fig.16. Voltage V_{DS} at Tr_1 with unearthed output.

Again for unearthed output, the voltage between Drain and Source of Tr_3 which is identical to Tr_4 , due to symmetry, is shown in Fig. 17.

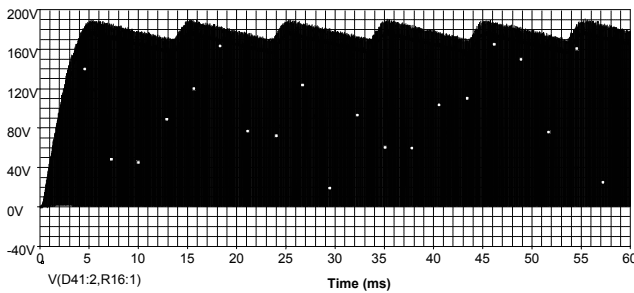


Fig. 17. Voltage V_{DS} at Tr_3 with unearthed output.

Fig.18. shows the voltage across the freewheeling diode of the Buck converter. The small overshoot of about 15 Volts shows the effect of the snubber circuit.

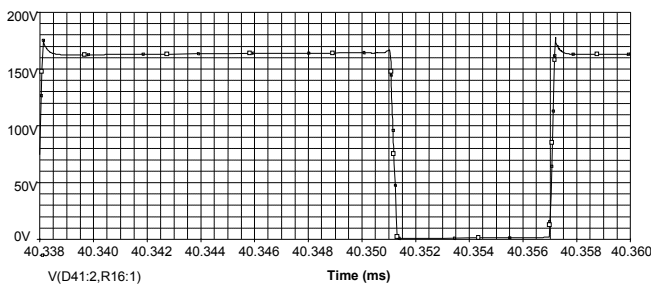


Fig. 18. Voltage across diode D_{12} .

Earthing the output for safety reasons, has the effect of increasing the voltage stress in all transistors, as the input mains supply and output voltage have the same reference voltage of earth. The voltage waveforms as shown in Figs. 19, 20, 21, 22, are complex due to the alternation in transistor switching and circuit configuration. Their maximum values, however, do not exceed 360 Volts in any of

the four transistors. At this voltage, there are many commercially available devices with high current ratings and small $R_{DS\ ON}$ resistances.

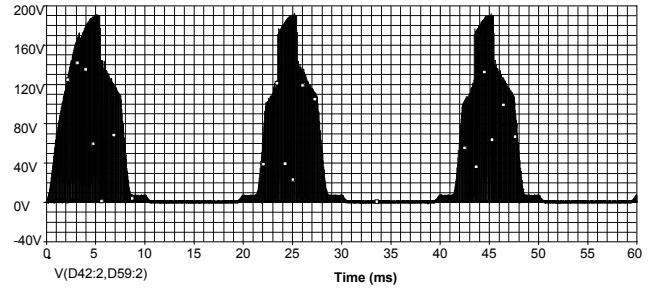


Fig.19. Voltage V_{DS} at Tr_1 with earthed output.

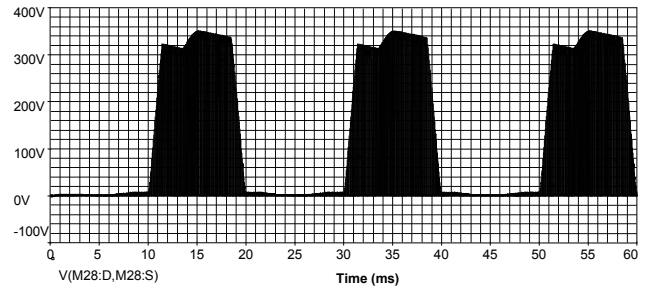


Fig. 20. Voltage V_{DS} at Tr_3 with earthed output.

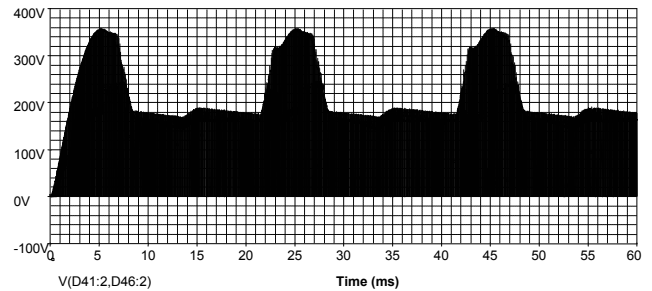


Fig. 21. Voltage V_{DS} at Tr_3 with earthed output.

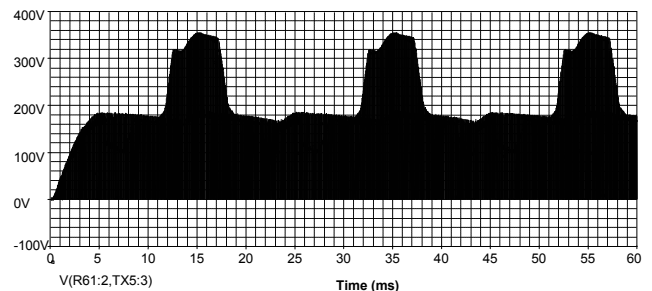


Fig. 22. Voltage V_{DS} at Tr_4 with earthed output.

Figs. 23 and 24 demonstrate the isolation principle of this power supply. Fig. 23 shows the current from the mains, to earth and output of the supply from starting, to 60ms (current through R_{E3}). Even though at steady state the current reaches peak values of ± 4 Amperes, if seen at higher time resolution, as in Fig.24, this current is constituted from short duration (100nsec) pulses associated with the capacitive nature between Drain and Source of

MOSFETs during switching. The energy associated with these spikes is very small and easily filtered using commercial type filters associated with power electronic circuits. However, these spikes will not trip a leakage current relay even if remained unfiltered as the manufacturers of standard type leakage current relays have assured the author.

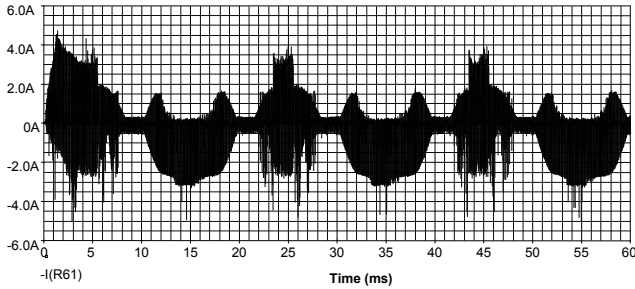


Fig. 23. Current to earth at output.

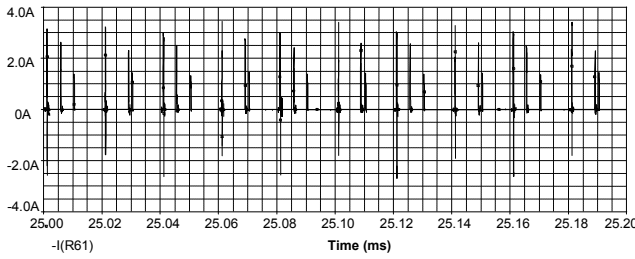


Fig. 24. Current to earth at output (higher resolution).

Fig. 25 shows the voltage across diode D_{14} with earthed output. For unearthed output, it is near zero volts, but here, however, the introduction of the earth loop produces switching reverse voltages across the diode, which approaches 350 volts. The voltages across D_{15} , D_{10} and D_{11} do not exceed 200 volts.

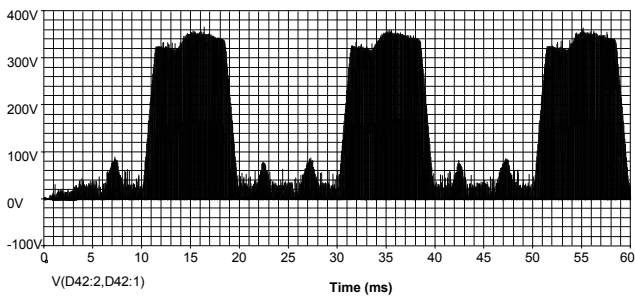


Fig. 25. Voltage across diode D_{14} with earthed output.

Finally, a very important parameter in all power supplies is efficiency. Repeated program runs were made for various load resistances and the results for

100 volts output were plotted in Fig. 26. For the power range between 250 and 3000 watts, the efficiency is better than 88%. For possible application of this power supply in telecommunications, the output voltage was lowered to 56 Volts and the efficiency as a function of output power was plotted in Fig. 27. For power range between 250 to 2500 watts, the efficiency is better than 80%.

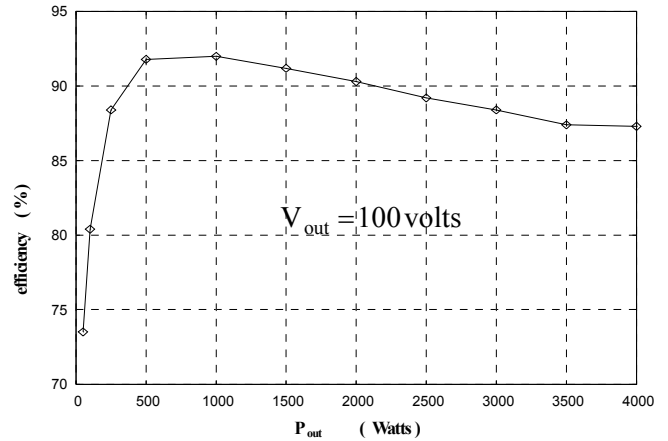


Fig. 26. Variation of efficiency with output power for output voltage = 100 Volts.

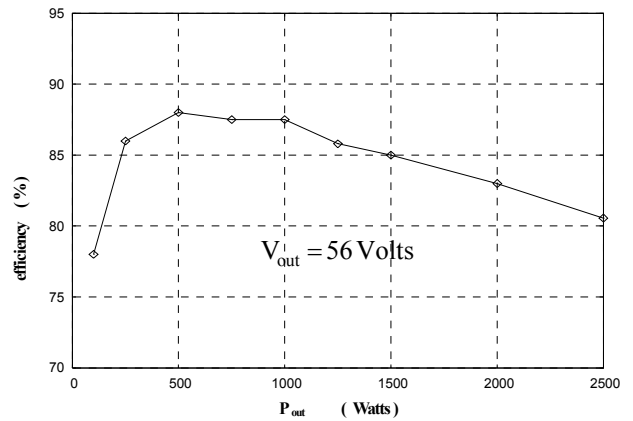


Fig. 27. Variation of efficiency with output power for output voltage = 56 Volts.

4 Considerations in practical applications

4.1 Protection

Personnel and equipment safety is ensured by earthing the output and connecting a classic blow fuse in the ac mains. Circuit malfunctioning due to simultaneous conduction of “primary” and “secondary” transistor or shorting the transistor will blow this fuse. The leakage current relay of the installation provides additive security.

Transient mains overvoltage can be suppressed using voltage dependent resistors, voltage crowbar protection, or other techniques.

4.2 Maximum output voltage

Due to the nature of Buck converters, the maximum output voltage in the previous publication was limited to one quarter of the ac line rectified voltage. This is because simultaneous conduction of “primary” and “secondary” transistors of the two Buck converters was prohibited and each Buck converter produced a maximum output voltage which was half of the input. In this paper, the “primary” Buck converter was substituted by switches charging the capacitor that provides energy to the “secondary” Buck converter through a small inductor. So, if we assume that the ac mains rectified voltage is 300V, the maximum theoretical output voltage is now 150 Volts, which covers most dc applications including telecommunications.

5 CONCLUSION

This paper describes an improvement in the new method of isolation between a.c. mains and d.c. voltage output without the use of a transformer. The necessity of using four transistors, makes this configuration attractive for output powers above 50Watts. As the power increases, the cost and complexity of handling the magnetizing current and leakage reactance energy of transformers used in rival half and full bridge converters, makes this circuit more attractive, especially for higher voltage and power applications. The proposed configuration has been presented and analyzed. The results from simulation have confirmed the theoretical predictions. The comparison between this power supply and its rival, the full bridge converter, is left for future publication which will also include experimental results.

References:

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