Low-Voltage-Low-Power Current Conveyor for Battery Supplied Memristor Emulator

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Abstract: - The paper presents a synthesis of low-voltage low-power current conveyor of the second generation (CCII) and transimpedance amplifier (TIA) from commercial integrated circuits. The main motivation was the necessity of constructing battery-supplied memristor emulator which uses current conveyors as important active elements, and also the fact that the commercially available CCIIs do not provide rail-rail low-voltage low-power operation. The CCII/TIA implementation can be also useful for fast prototyping of various sensor circuitries, filters, oscillators, and other circuits which require precise current conveyors with very small *x*-terminal resistances.

Key-Words: - Memristor, emulator, mutator, controlled source, current conveyor, instrumentation amplifier.

1 Introduction

The paper [1], published in Nature in 2008, triggered great interest in the simulation models of the memristor, the fourth fundamental passive element, theoretically predicted in 1971 by Leon Chua [2]. Recently, other similar „mem-elements“ such as memcapacitors and meminductors have come to be considered by many researchers [2-7]. Since these elements are still not available as off-the-shelf two-terminal devices for common experimenting, the importance of their simulation models [8-18] and particularly of their hardware emulators [19-22] grow steadily.

The general approach of the memristor emulation is described in the original work [2]: Using the so-called M-R mutators, the memristor with a prescribed charge-flux constitution relation can be emulated via nonlinear resistor with similar current-voltage characteristics. Analogously, memcapacitors and meminductors can be emulated via MC-MR and ML-MR mutators, terminated by memristors, as described in [16]. The common point of these methods is that such mutators are linear two-ports with their terminal behavior being modeled via controlled sources. As shown in [16, 17, 20], it is useful to implement them via current conveyors of the second generation (CCIIs), or, more specifically, via CCII followed by the voltage buffer, thus via TIA (Transimpedance Amplifier) [23].

One example of the mutator for transforming nonlinear resistor *R* into memristor, proposed in [23], is shown in Fig. 1. It uses two commercial TIAs, namely AD844, and one additional operational amplifier (OpAmp) AD826. Details are given in [23].

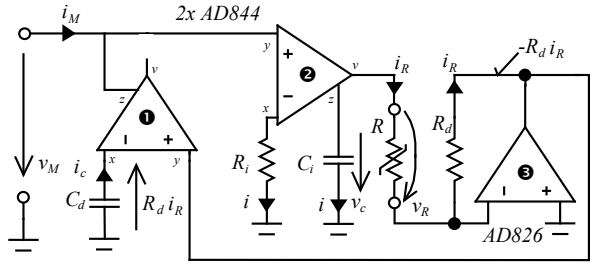

Fig. 1. Example of mutator transforming nonlinear resistor *R* into memristor on (v_M, i_M) port [23].

A disadvantage of the above solution appears if the mutator together with the nonlinear resistor were to be designed as an autonomous battery powered device, resembling the classical two-terminal component. Due to low-voltage low-power (LV LP) requirements, LV LP rail-rail amplifiers must be used. However, such commercial current conveyors (with accessible *z* terminal) are not available on the market. This fact can be generalized to the conclusion that today's designers are faced with the problem of implementing LV LP hardware from commercial integrated circuits, which use current conveyors. Such requirements are frequent, for example, in the areas of sensor-processing circuits, filters, and oscillators. AD844, a typical representative of commercial CCII with accessible *z*

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terminal, is not LV LP, and not rail-rail amplifier. In addition, the well-known effect of the nonzero resistance of the *x* terminal (50 Ohms typically of AD844) can be a limiting error factor in several applications.

Presently, if we avoid the possibility of designing and fabricating a custom IC, the only viable way of building LV LP CCII applications is making current conveyors from the off-the-shelf LV LP amplifiers. Such amplifiers are usually of lower bandwidth. Fortunately, the bandwidth is not a critical parameter for quite a number of precise LV LP applications. For example, memristor mutators are low-frequency circuits since the typical hysteresis effects are dominant at low frequencies, typically up to tens or hundreds of hertz, and these effects cease with increasing the frequency.

This paper deals with the above problem of CCII/TIA synthesis. It describes the basic circuit idea of such a synthesis via classical and instrumentation OpAmps in the first step. Finally, two concrete circuits are shown and their typical CCII characteristics are presented, demonstrating the key parameters of implemented conveyors. These CCIIs/TIAs were successfully used for constructing battery-powered LV LP memristor emulators based on the principle in Fig. 1.

2 Circuit Idea of Implementing Low-Voltage Low-Power CCII/TIA

The proposed principle of implementing CCII/TIA via two conventional OpAmps (Nos ❶ and ❸) and one high-input-impedance difference amplifier (No ❷) is demonstrated in Fig. 2.

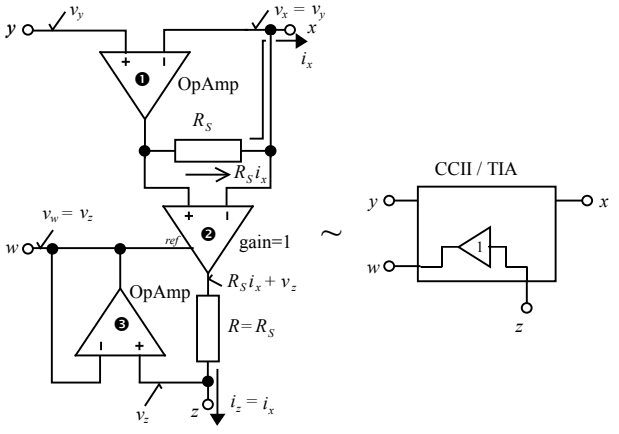

Fig. 2. Circuit idea of implementing CCII/TIA via two OpAmps and one instrumentation amplifier.

Due to the negative feedback of OpAmp No ❶, the voltage v_x precisely follows the voltage v_y, which is the first basic feature of CCII [24]. Note that the equality $v_x = v_y$ also minimizes the *x*-terminal intrinsic resistance R_x to zero. In reality, this resistance will be decreased to zero with the gain of OpAmp No. ❶ tending to infinity. Within the OpAmp bandwidth, R_x is much lower than for the commercial CCII.

The current i_x, flowing out of the output terminal of the voltage follower, causes a voltage drop at resistor R_s, which is also the input voltage of the difference amplifier No ❷. The *ref* pin of this amplifier is used for the well-known implementation of the voltage-controlled current source i_z: The output voltage of the difference amplifier is a sum of the difference input voltage and the voltage at the *ref* pin. This pin is bootstrapped by voltage v_w, which is a buffered copy of the voltage v_z, and v_z is the output voltage of the difference amplifier decreased by the voltage drop at resistor *R*. As a result, the current i_z is equal to the current i_x multiplied by the ratio of resistances R_S and *R*. For $R_S = R$, i_z is simply a copy of i_x, which is the second basic feature of CCII.

Since the OpAmp No ❸ operates as voltage buffer, the voltage v_w is a buffered copy of the *z*-terminal voltage. It is a basic feature of TIA [25].

3 CCII/TIA Implementation

The above circuit idea was implemented via two different circuits.

The first one is exactly the same as in Fig. 2, with $R_s = R = 1\text{k}\Omega$. OpAmps Nos ❶ and ❸ were obtained via a 5 MHz low-voltage low-power rail-rail dual OpAmp AD8632. An AD8221 precision instrumentation amplifier was selected as amplifier No ❷. All the active devices were supplied by ±3.6 V.

The second version of the circuit configuration is shown in Fig. 3. Note that the only difference in comparison with the circuit in Fig. 2 is the replacement of instrumentation amplifier No ❷ by two classical OpAmps ❷', ❷'' and four 10 kΩ resistors. Two 36 pF capacitors serve for the necessary frequency compensation. OpAmp No ❷' provides high-impedance buffering of the *x* terminal. The quad OpAmp LMV 554 is supplied by ±3.6 V.

The reason for designing the second circuit in Fig. 3 consists in achieving lower power consumption since LMV554 is a micro-power OpAmp with a quiescent current of only 37μA per amplifier.

DC characteristics $V_x(V_y)$ and $I_z(I_x)$ of both circuits are shown in Figs 4 and 5, respectively. They were measured for *x* and *z* outlets terminated by grounded resistors 10 kΩ and 10 Ω, respectively. Linearity within the OpAmp saturations is excellent.

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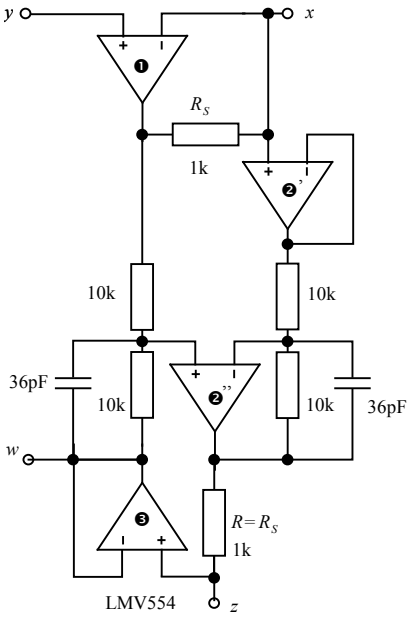

Fig. 3. CCII/TIA implementation via one low-power quad OpAmp.

The total power consumption is 6.9 mW for circuit No 1 and 1.1 mW for circuit No 2.

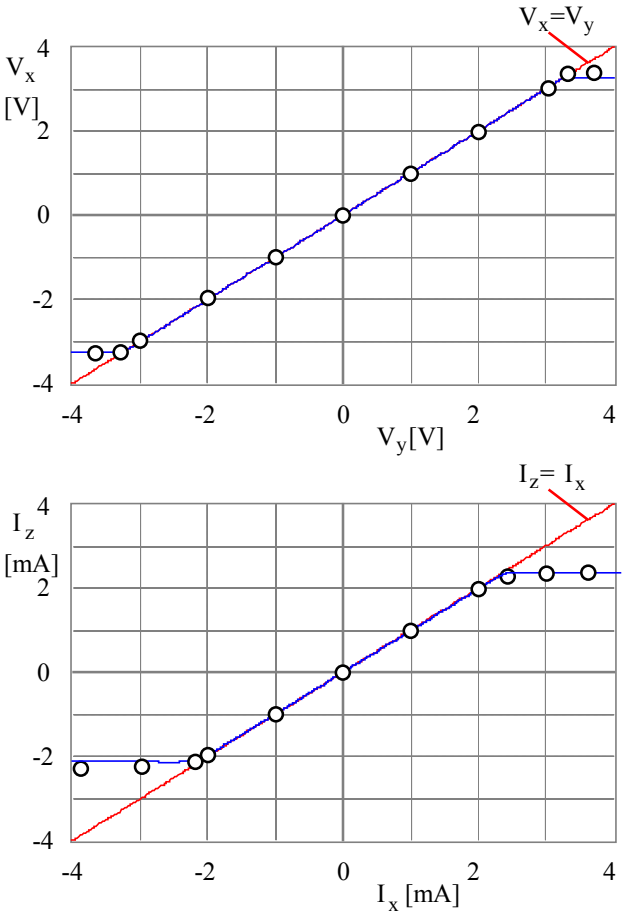

Fig. 4. DC characteristics $V_x(V_y)$ and $I_z(I_x)$ of CCII/TIA in Fig. 2, _ simulated, o measured.

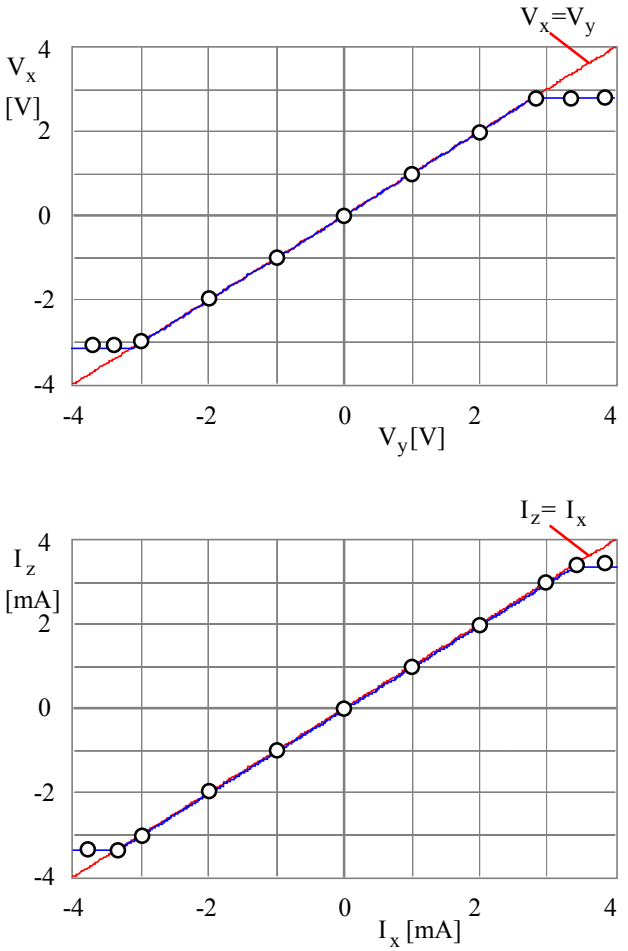

Fig. 5. DC characteristics $V_x(V_y)$ and $I_z(I_x)$ of CCII/TIA in Fig. 3, _ simulated, o measured.

The following Fig. 6 demonstrates the dependence of the bandwidth of the input voltage buffer with the transfer function V_x/V_y on the resistance of external load connected to the x terminal. Note that the bandwidth decreases with decreasing this resistance, and that the buffer in circuit 2 is rather faster than in circuit 1.

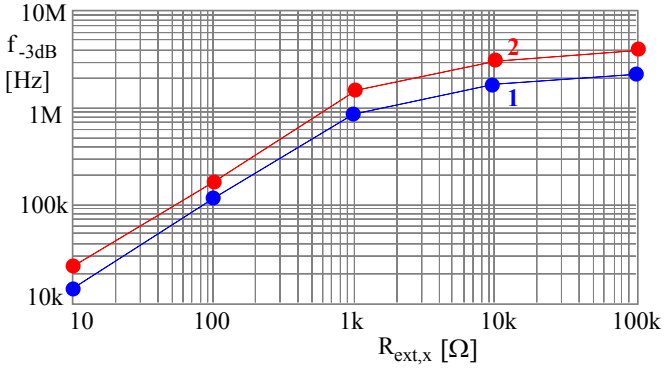

Fig. 6. Measured -3dB cutoff frequency of voltage gain V_x/V_y versus external resistance at x terminal, circuits in Figs 2 (1) and 3 (2).

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Figure 7 compares the two proposed circuits from the point of view of the attainable bandwidth of the current transfer I_z/I_x for various resistances of the load connected to the z terminal. Note that the bandwidth decreases with increasing this load resistance, and that this current stage is faster for circuit No 1 for the low-frequency region. The bandwidth of the other circuit is more stabilized due to its frequency compensation.

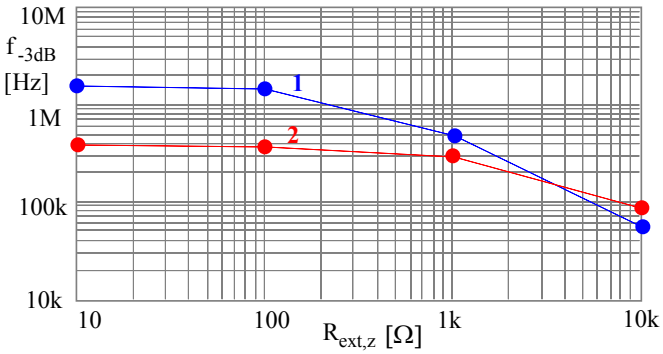

Fig. 7. Measured -3dB cutoff frequency of current gain I_z/I_x versus external resistance at z terminal, circuits in Figs 2 (1) and 3 (2).

PSPICE simulation was performed, analyzing the frequency dependence of parasitic x-terminal impedance and also decomposing this impedance into resistive and reactance parts. The resistive part shown in Fig. 8 should be completed with the information that this impedance is of inductive character for both circuits, with serial inductances of ca 120µH and 72 µH for circuits 1 and 2, respectively. Both inductances slightly decrease with increasing frequency. A detailed analysis of this phenomenon reveals that the low-frequency value of R_x is given by the ratio of R_s and DC open-loop gain of OpAmp No ❶, whereas the low-frequency value of series inductance is a ratio of R_s and GBW of this OpAmp.

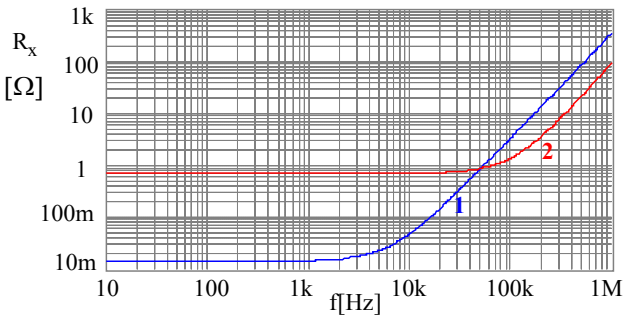

Fig. 8. Simulated frequency dependence of parasitic x-terminal resistance, circuits in Figs 2 (1) and 3 (2).

Similar to Fig. 8, Fig. 9 compares both circuits according to the parasitic z-terminal resistance. Note that circuit No 2 exhibits a lower value of low-frequency R_z but this value is preserved within a larger frequency range. A more detailed analysis reveals that low-frequency R_z is approximately equal to the product of R=R_S (see Figs 2 and 3) and DC open-loop gain of OpAmp No ❸.

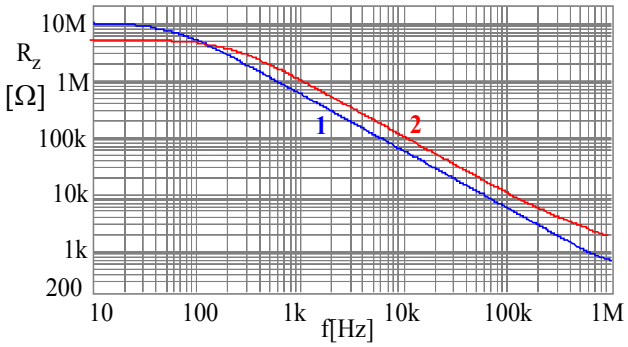

Fig. 9. Simulated frequency dependence of z-terminal parasitic resistance, circuits in Figs 2 (1) and 3 (2).

4 Conclusion

The paper describes a simple circuit which can implement the current conveyor of the second generation (CCII) including the voltage buffer connected to the z terminal of CCII. In other words, this circuit can mimic the behavior of transimpedance amplifier (TIA) with accessible z terminal. The complete schematic can consist of two OpAmps and one instrumentation amplifier plus two resistors, or, alternatively, of one quad OpAmp plus six resistors. In this way, CCII/TIA with specific parameters which are not available via the off-the-shelf CCIIs/TIAs can be easily constructed. Low-voltage low-power CCIIs/TIAs are demonstrated in this article, finding their applications in battery powered memristor hardware emulators.

Acknowledgment

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