Symbolic Simplification by means of Graph Transformations

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Abstract: The paper deals with an effective method for approximate symbolic analysis of linear circuits based on nontrivial transformations of voltage and current graphs. The method is based on eliminating the low-voltage branches from “high-voltage” loops and the low-current branches from “high-current” nodes, which simplifies circuit equations and the final symbolic formula. This allows reaching a higher degree of simplification in comparison with the simple edge deletion or contraction used in previous methods. The paper describes how the branches with low voltage or current can be identified and removed.

Key-Words: Symbolic analysis, Topology reduction, Two-graph method, Linear circuits, Circuit theory, CAD tools

1 Introduction
Recently, we have seen growing interest in the symbolic analysis of large multi-physics systems; see [1], [2], and references therein.

The applicability of exact symbolic analysis is constrained to relatively small linear systems, as the size of the resulting expression grows exponentially with the number of components. If we appropriately restrict the range of frequency and network parameters, the majority of symbolic terms can be removed from large expressions without any significant numerical error [3]. Negligible symbolic terms are identified numerically, based on the known parameters of circuit components.

The simplification methods can be divided into three classes according to the stage of analysis at which the simplification is performed: Simplification Before Generation (SBG), Simplification During Generation (SDG), and Simplification After Generation (SAG) [3]. The SAG methods are simple but very expensive in terms of computation and storage. Pure mathematical methods of the SDG type may have problems with the interpretability of resulting expressions [4]. The SBG methods simplifying the circuit equations or graphs are the most effective ones, as they work with a relatively small number of circuit equations [4].

A method, published as Sifting Approach [5], is based on a heuristic algorithm consisting in device parameter elimination from numerator and denominator submatrices separately. Another method [6], called Two-graph Simplification, modifies the voltage and current graphs constructed for the numerator and the denominator separately. The simplification consists in deleting or contracting edges representing a network parameter with sensitivity-based control strategy. The matrix-based method from [7] is based on removing individual matrix elements to obtain a simplified solution. However, in some cases the matrix simplification may surprisingly add symbolic terms that were not present in the original expression.

We have proposed a different approach based on the two-graph method. Instead of simply deleting or contracting the graph edges it modifies the graph structure in order to decrease the number of common spanning trees. The respective graph-theoretical proofs were published in [8]. This paper deals with a practical method for identifying low-voltage or current branches that can be removed from high-voltage loops or high-current nodes.

2 Application of Two-Graph Method
2.1 Basic Principle
The basic idea of the two-graph method consists in formulating separately Kirchhoff’s Voltage Law and Kirchhoff’s Current Law by means of two graphs – the voltage graph $G_V$ and the current graph $G_I$ [9]. Each circuit element of the admittance type (RLCgm) is represented in each graph by just one edge. Other elements are modeled using equivalent models [9].

The determinant of the nodal admittance matrix is

$$
\det Y = \sum_{t \in T(G_V) \cap T(G_I)} \varepsilon(t) Y^0(t)
$$

where $Y^0(t)$ is the tree-admittance product of tree $t$, $T(G_V)$ and $T(G_I)$ are the sets of all spanning trees of voltage and current graphs. The intersection $T(G_V) \cap T(G_I)$ represents the common spanning
trees of $G_1$ and $G_V$. $\varepsilon(t) = \pm 1$ is the tree sign. The technique of augmented circuit [9] allows computing both the numerator and the denominator of any network function. Fig. 1 shows an example for the voltage transfer ratio, where the VCVS is represented by a suitable admittance model [9].

Fig. 1 Augmented circuit for voltage transfer ratio.

The determinant of the admittance matrix is

$$\Delta = \Delta_1 + A\Delta_2,$$  

$$K_V = \frac{\Delta_2}{\Delta_1}. \quad (3)$$

Since $A$ is a symbol, the terms belonging to $\Delta_1$ or $\Delta_2$ are easy to recognize.

2.2 Example Circuit

Let us limit ourselves to the SBG methods only. Fig. 2 shows a simple circuit, whose network parameters are: $R_B = 36k\Omega$, $r_x = 4k\Omega$, $g_m = 35mS$, $R_L = 4k\Omega$. Let us suppose that all negligible elements have already been eliminated from the circuit, i.e. a parametric SBG cannot proceed further in circuit simplification.

Fig. 2 Simple small-signal model.

The exact formula for the voltage transfer ratio is

$$K_V = \frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{r_x}{R_B + r_x} g_m R_L. \quad (4)$$

As $R_B >> r_x$, the formula can be further simplified, but resistor $r_x$ cannot be simply removed or its terminal shorted. Both operations would cause an unacceptable error.

Fig. 3a shows voltage and current graphs for the augmented circuit. Edges “1” and “A” model the VCVS [10]. Let the voltage across input edge “1” be 1V. Then the voltage across $r_x$ is 0.1V. The voltage can be neglected in loops $\{1-G_B g_s\}$ and $\{1-G_B g_m\}$ but not in loop $\{g_x g_m\}$. A simple modification in Fig. 3b removes $g_x$ and $g_m$ from the “high-voltage” loops only. The simplified formula for the voltage transfer ratio obtained using (2) and (3) is then

$$K'_V = -\frac{r_x}{R_B} g_m R_L. \quad (5)$$

An inspection of the voltage and current graphs from Fig. 3b shows that they represent a CCCS instead of $r_x$ and VCCS.

Fig. 3 a) Original and b) modified graphs.

This simple example shows the basic principle of the method – selective removal of the low-voltage edges from the “high-voltage” loops. Similar transformations can be found for the current graph.

3 Topological Simplification

3.1 Basic Definitions

Let $G$ be a graph. Then $V(G)$ is a set of its vertices, $E(G)$ is a set of its edges, and $T(G)$ is a set of its trees. The incidence of edge $e$ in graph $G$, $\rho(e,G) = (i, j)$, assigns two vertices $i$, $j$ to edge $e$. Graph $G$ is said to be separable if there is a vertex whose removal splits the graph into two or more components. A block is the maximal nonseparable subgraph. For example, the voltage graph in Fig. 3a has two blocks while the current graph has three blocks.

**Definition 1**: Separation of a connected subgraph $G_S$ from a graph $G$ is an operation that transforms $G$ into

$$G' = \bar{G} \cup G_S,$$  

where $\bar{G}$ is a subgraph whose edge set is $E(\bar{G}) = E(G \setminus G_S)$. The incidence $\rho(e,\bar{G}) = (v_r, v_j)$ of any edge $e \in E(\bar{G})$ is transformed into $\rho(e,\bar{G}) = (f(v), f(v_j))$, where $f$ is

$$f(v) = \begin{cases} 
  v_c & \text{if } v \in V(G_S) \\
  v & \text{otherwise}
\end{cases} \quad (7)$$

$v_c$ is an arbitrary but fixed vertex $v_c \in V(G \setminus G_S) \cap V(G_S)$. The operations will be
denoted as follows:

\[ G = G \Rightarrow G_S, \quad G' = G \triangleright G_S. \] (8a,b)

![Diagram](image)

**Fig. 4** Separation of \( G_S = \{e_1, e_2, e_3\} \): a) graph \( G \); b) graph \( \tilde{G} = G \Rightarrow G_S \); c) \( G' = G \triangleright G_S \).

Fig. 4 demonstrates the separation of \( G_S = \{e_1, e_2, e_3\} \). The transformation does not change the number of edges and vertices, and decreases the number of spanning trees of \( G' \). Proof can be found in [8].

### 3.2 Loop and Cut Simplification

Let a circuit be represented by the current graph \( G_i \) and the voltage graph \( G_V \) with edges \( e_1, e_2, \ldots, e_b \), whose weights are the magnitudes of branch currents \( i = [i_1, i_2, \ldots, i_b]^T \) and voltages \( v = [v_1, v_2, \ldots, v_b]^T \) for a particular frequency. Let us additionally suppose that all negligible elements have already been removed from the circuit.

Let \( L_1, L_2, \ldots, L_b \subseteq G_V \) be all loops of the voltage graph \( G_V \). The voltage \( v(e) \) of an edge \( e \in E(L) \) will be considered numerically negligible in loop \( L \) if

\[ |v(e)| < \varepsilon_v \max_{e \in E(L)} |v(e)|, \] (9)

where \( \varepsilon_v \in (0, 1) \) is a threshold value. Such an edge is a candidate for being removed from \( L \) [8].

Let us assume that the voltage graph \( G_V \) can be decomposed into two edge-disjoint subgraphs \( G_V^{H} \) and \( G_V^{L} \) and that the condition

\[ \max_{e \in G_V^{H}/L} |v(e)| < \varepsilon_v \max_{e \in L} |v(e)| \] (10)

holds for any loop \( L \subseteq G_V \) that is contained in both subgraphs. Then it is possible to remove the low-voltage edges of \( G_V^L \) from high-voltage loops by separation

\[ G'_V = G_V \triangleright G_V^L. \] (11)

In the example from Section 2, \( G_V^L = \{g_x, g_m\} \).

It can be also shown that removing small-current branches from high-current cuts leads to decomposing \( G_i \) with respect to a threshold value \( \varepsilon_i \in (0, 1) \) into two edge-disjoint subgraphs \( G_i^H \) and \( G_i^L \) [8]. If for any loop \( L \subseteq G_i \) contained in both subgraphs the condition

\[ \min_{e \in E(L)} |v(e)| < \varepsilon_i \min_{e \in E(G_i^{H}/L)} |v(e)| \] (12)

holds, then it is possible to perform the separation

\[ G'_i = G_i \triangleright G_i^H. \] (13)

### 3.3 Algorithms

The error-control strategy of the method is similar to the method of [1]. The error criterion is based on comparing the numerical solution before and after each transformation for each of \( m \) test frequencies

\[ \varepsilon_a = \max_{i=1,m} \frac{20 \log[E(\omega_i)]}{\Delta M_{\omega_i}} + \frac{\arg(E(\omega_i))}{\Delta \Phi_{\omega_i}}, \] (14)

where \( E(\omega) = F_a(\omega)/F_b(\omega) \), \( F_b(\omega) \) is the reference network function, and \( F_a(\omega) \) is the function after graph transformations, i.e. it accumulates errors introduced by all the simplification steps made.

The simplification process is a sequence of elementary operations. Operations causing the lowest error are performed first. The main cycle of the procedure is shown in Fig. 5. The result is a simplified circuit model, which is then analyzed symbolically.

```plaintext
compute reference numerical solution;
while \( \varepsilon_a < \varepsilon_{\text{max}} \) do
    generate all possible operations;
    compute error of each operation;
    perform operation(s) with the lowest error;
    update accumulated error \( \varepsilon_a \);
    update numerical solution;
    undo last operation;

Fig. 5 Main cycle of simplification.
```

The generation of elementary graph transformation will be explained on the voltage graph in Fig. 6a, where the numbers show voltage magnitudes on a particular frequency.

The generation of subgraphs for separation that fulfill (10) or (12) starts with the generation of their blocks (see definitions in Section 3.1).

Let the graph be **connected** and have \( n \) vertices and \( b \) edges. Any spanning tree \( t \) consists of exactly \( n-1 \) edges - twigs. The remaining edges will be called **chords** [11]. Fig. 6b shows a tree with the lowest voltage-magnitude product (edges \( t \)) and the remaining chords sorted in ascending order (edges \( c \)).
The application of the algorithm from Fig. 7 for \( \varepsilon_V = 0.1 \) to the graph from Fig. 6a generates the following three blocks: \( B_1 = \{c_1, t_3, t_5\} \), \( B_2 = \{c_2, t_4, t_6\} \), and \( B_3 = \{c_1, c_2, c_3, c_4, t_1, t_2, t_3, t_4, t_5, t_6\} \). Note that the blocks contain low-voltage edges in comparison with the rest of the graph.

Subgraph separation (11) can be divided into elementary operations exploiting the block structure of both \( G^V \) and \( \widetilde{G}^V = G \Rightarrow G^V \). Condition (9) has been formulated for loops contained in both subgraphs. Let us assume that \( G^V \) is separable with blocks \( B^V \). As there is no loop contained in two or more blocks, the separation of any block \( B^V \), which is considered the elementary operation, satisfies (9) as well. This is shown in Figs 6c, 6d, and 6e.

In fact, \( G^V \) should be separated at least into two blocks. Graph \( \widetilde{G}^V \) may also be separable. The subgraphs contained in the separable \( \widetilde{G}^V \) form disjoint subsets. It is possible to augment blocks \( B^V \) with a suitable subgraph to make \( \widetilde{G}^V \) nonseparable.

The separation of \( G^V \) is a valid operation, leads to a separable \( \widetilde{G}^V \) with two blocks \( \widetilde{B}_1 = \{t_1, t_2, c_3, c_4\} \) and \( \widetilde{B}_2 = \{t_7, c_5, c_6\} \). Augmenting \( G^V \) with the complement of \( \widetilde{B}_1 \) results in a nonseparable \( \widetilde{G}^V \), Fig. 6f. Augmenting \( G^V \) with the complement of \( \widetilde{B}_2 \) results in the already generated separation in Fig. 6e.

4 Example Analysis

The capabilities of the topological transformation are demonstrated on the analysis of a simple amplifier, Fig. 8. All transistors were modeled using the standard Gummel-Poon Spice model. The aim was to simplify the circuit model for the voltage transfer ratio. The required accuracy was ±1 dB for magnitude and ±3° for phase, checked at frequencies of 100 Hz and 50 kHz.

The parametric preprocessing reduced the original 27 network parameters to 6 \( (g_{m1}, R_{C1}, R_{C2}, C_{d}, g_{m2}, R_{C2}) \). The topological procedure was able to further reduce the number of terms in the numerator and the denominator. Candidates for separation were generated for \( \varepsilon_V = \varepsilon_1 = 0.2 \). The topological algorithm separated one subgraph from the voltage graph:

\[
\{ g_{m1}, 1/R_{C1}, g_{m2} \}
\]

and one subgraph from the current graph:

\[
\{ g_{m2}, 1/R_{C2} \}
\]

The final symbolic formula
could not be further simplified even if using the SAG method.

Fig. 8 Simple BJT amplifier.

Table I  Results of simplification

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<th>TSBG</th>
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*) Estimation using the Binet-Cauchy theorem [12].

References: