Fractional Frequency Synthesizers Based on Flying Adder Principle
Description and Simulations Results

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Abstract: - Frequency synthesis is one of the most important and most actively researched subjects in the field of VLSI mixed-signal circuit design. Among the existing techniques in this area, phase locked loop fractional architecture is a widely used one for generating frequencies which are not integer multiple of the input reference frequency. Flying-Adder architecture is an emerging technique which is based on a new concept time-average-frequency, to generate frequencies. This paper presents fractional frequency synthesizer architecture based on concept flying-adder and phase locked loop principle. The simulation results concerning this system are presented.

Key-Words: Direct digital synthesis, fractional synthesizer, flying adder, frequency synthesis, phase locked loop, sigma delta.

1 Introduction
Along the history of frequency synthesis development, Phase-Lock Loop (PLL) based synthesis method is the mostly used approach. Within this approach, there are several milestone techniques: Integer-N architecture, Fractional-N architecture and Sigma-Delta Fractional-N architecture. Integer-N PLL is commonly used in the cases where frequency requirement is straightforward. Fractional-N PLL is a technique which can generate output frequencies that are fractional multiples of the input reference frequency. This is important step forward from the Integer-N PLL. However, this advancement is accompanied with a serious drawback. It degrades the spectrum purity of the output frequency. To overcome this problem, Sigma-Delta Fractional PLL was developed [1-5].

The Flying-Adder architecture is an emerging technique in the field of frequency synthesis. The proof of concept was constituted in 2000 [6]. It was built on the foundation of a new concept: Time-Average-Frequency. The theoretical foundation was established in 2008 [7, 8]. The more in-depth study is delivered in [9, 10]. The most distinguished features of this technique are its instantaneous response speed and the capability of generating arbitrary frequency [6]. In this paper, the architecture of fractional flying adder (FFA) is used with conjunction of PLL. Compared to the pure structure FFA frequency synthesizer, the proposed approach can achieve the same frequency resolution with reduced fractional spurs.

Fig. 1. The block diagram of fractional flying adder (FFA) frequency synthesizer consist of: N-phase clock generator (frequency $f_{CLK}$), multiplexer MUX, D-flip-flop, digital adder with control frequency word $FW$, register and truncation which convert $n$-bit word to $r$-bit word. Output frequency of FFA is $f_{FA}$.
2 Flying Adder Synthesizer

The FFA [6, 7], which is also referred to as direct digital period synthesizer or digital-to-frequency converter (DFC), is an independent frequency synthesis. The FFA shares some functionality with circuits that involve phase-switching prescalers and digital phase accumulators. The block diagram of basic FFA is shown in Fig. 1. The system is driven by the $N = 2^m$ clock phases with frequency $f_{CLK}$, one of which is selected by the $N$-to-1 multiplexer (MUX). The rising edges of MUX’s output (signal $m(t)$) is a trigger for the $n$-bit register changing its value from

$$x_{k+1} = (x_k + FW) \mod 2^n \tag{1}$$

where $FW$ is the $n$-bit long frequency control word and $k$ is integer variable which presents counts of the rising edges of signal $m(t)$. The register value $x_k$, is then truncated by taking the first $r$, most significant bits to $y_k$ according (2).

$$y_k = \frac{x_k}{2^{n-r}} \tag{2}$$

The $y_k$ controls the MUX and therefore chooses the input phase that passes through the MUX. The signals $m(t)$ which is a sequence of pulses, or spikes is fed to the D-Flip-Flop which acts as a frequency divider by-2 providing the output signal $f_{FA}$.

FFA employs a multiphase generator to generate multiple clock signals evenly distributed in a full clock cycle. These same-frequency-but-different-phases clock signals are used to synthesize desired frequency. The synthesized signal is directly related to the phase difference “$\Delta$” among the multiple phase outputs from the generator (Fig. 2). The frequency control word $FW$ sets the number of $\Delta$ before the synthesized clock toggles. The frequency of the clock output is given by the following expression [10]:

$$f_{FA} = \frac{1}{FW \cdot \Delta} = \frac{1}{FW} \cdot \frac{1}{f_{CLK} \cdot N} = \frac{f_{CLK}}{FW} \tag{3}$$

where $N$ is the number of VCO stages. It is important to note that value $x_k$, eq. (1) in Register is limited to $2^n - 1$ (function $\mod 2^n$) and therefore $y_k$, eq. (2) is also limited. Unlike the conventional PLL, the FFA consists of digital circuitry such as multiplexers, adders, and flip-flops, thereby resulting in fast switching time and wide tuning range. Specifically, an FFA architecture with an $N$-stage VCO has a frequency range of $0.5 \cdot f_{CLK}$ to $0.5 \cdot N \cdot f_{CLK}$ [5]. Due to its wide tuning range and instant response time, the FFA frequency synthesizer is highly suitable for many System-on-Chip applications. The frequency control word could be an integer or a fractional number when high frequency resolution is desired. When $FW$ is an integer, the FFA synthesizer can be viewed as a phase divider which can achieve finer resolution than frequency divider does.

![Fig. 2: Example of signals of multiphase generator (8 phase generator, but only 4 phases are displayed) with phase difference $\Delta$ among the multiple outputs.](image)

![Fig. 3: The block diagram of first fractional frequency synthesizer which consists of FFA and PLL placed in output.](image)
effectively reduce the spurs, this approach comes at the cost of increased overall noise.

Fig. 4. The output frequency of FFA, as function of control frequency word $FW < 4; 31>$, for $n=5$.

Fig. 5. The time diagram of signals in synthesizer for $n=5$, $r=3$, $N=8$ and control frequency word $FW = 31$. A – 8th phase clock $f_{CLK}$, B – Register value ($y_k$), C – Truncation value ($y_k$), D – MUX output $m(t)$, E – D Flip-Flop output $f_{FA}$, F – PLL output $f_O$.

3 First Frequency Synthesizer

The FFA synthesizer has a wide tuning range and a quick response time but has frequency spurs in the output spectrum when working in the fractional mode to achieve higher resolution. On the other hand, PLL technique can help reduce the spurs but fractional-N PLL architecture is complicated. This work introduces a frequency synthesizer architecture that incorporates the advantages of the FFA and conventional PLL architectures but avoid the drawbacks of each. The block diagram of first synthesizer is shown in Fig. 3. This system contain also frequency control block which is used for coarse frequency setting in $N$-phase clock (signal $FPC$) and also in PLL (signal $FPLL$) and fine frequency setting (signal $FW$) connected to FFA. For coarse frequency setting the different principles can be used (depends on the types of system, e.g. oscillators switching etc.) and aren’t described in this paper.

Fig. 6. The time diagram of signals in synthesizer (zoom of Fig. 5).

Fig. 7. The frequency spectrum of first synthesizer output $f_O$ with PLL.
The simulation results for 8 phase clock ($N=8$), 8 input $MUX$ (3 bit address, $r=3$), 5 bit register ($n=5$) and conventional PLL with charge-pump phase detector and voltage controlled oscillator with sinus signal output are presented. The output frequency of $FFA$ as function of control frequency word $FW$ (for $n=5$, $r=3$) is shown in Fig. 4. The $FW$ step is 1, size of $\langle 4; 31 \rangle$. For better frequency resolution is possible to extend register, (increase of $n$), which means extend floating part of the number. The FFA architecture can generate any frequency, providing that there are sufficient fraction bits in the accumulator-register. On the other hand, the pulses on FFA output aren't equally distributed. The time diagram of signals in synthesizer are shown in Fig. 5 and zoom of this figure is shown in Fig. 6. The example of frequency spectrum of first frequency synthesizer is shown in Fig. 7. The spurious spikes of FFA are filtered by PLL low-pass filter. In wide range of frequency synthesizer, not only the voltage controlled oscillator frequency is changed, but also the PLL low-pass filter cutoff frequency must be changed.

### 4 Second Frequency Synthesizer

The block diagram of the second fractional frequency synthesizer based on flying adder principle and PLL is shown in Fig. 8. The synthesizer consists of: Reference clock, charge-pump phase detector, $N$-phase voltage controlled oscillator (controlled by $V_{VCO}$), multiplexer MUX, frequency divider (divide by number $D$), digital adder with control frequency word $FW$, register and truncation which convert $n$-bit word to $r$-bit word. Output frequency of FFA is $f_{fa}$. The synthesizer output frequency is $f_{OUT}$. The output frequency of this synthesizer is given by (4).

$$f_{OUT} = f_R ND \left(1 - \frac{FW}{2^n}\right)$$

(4)

where $f_R$ is frequency of reference oscillator, $D$ is divider number, $N$-number of phases of voltage controlled oscillator and $FW$ is control word and for $\langle FW \rangle mod 2^n \in <2^n-N, 2^n>$

$$f_{OUT} = f_R ND \left[N - 1 - \frac{FW}{2^n} - (N - 2)\right]$$

(5)

The output frequency as function of $FW$ for $f_R=1.35$ [Hz], $D=4$ and $N=8$ is shown in Fig. 9. The maximal output frequency is 5.4 [Hz].

![Fig. 8. The block diagram of second fractional frequency synthesizer based on PLL and FFA principle. The synthesizer consists of: Reference clock, $N$-phase voltage controlled oscillator (controlled by $V_{VCO}$), multiplexer MUX, frequency divider (divide by number $D$), digital adder with control frequency word $FW$, register and truncation which convert $n$-bit word to $r$-bit word. Output frequency of FFA is $f_{fa}$. The synthesizer output frequency is $f_{OUT}$. The output frequency of this synthesizer is given by (4).

![Fig. 9. Output frequency $f_{OUT}$ of second fractional frequency synthesizer as a function of control frequency word $FW$ for $f_R=1.35$, $D=4$, $N=8$ and $n=5$.](image-url)
The main advantage of second fractional frequency synthesizer is linear dependence of output frequency versus control word and good spectral properties (depend on lowpass filter of VCO). The frequency spectrum (in steady state) for $FW=17$ is shown in Fig. 10.

![Fig. 10. The frequency spectrum of second frequency synthesizer for $FW=17$.](image)

The voltage of PLL low-pass filter and output frequency time responses on step $FW$ change are shown in Fig. 11 and Fig. 12 (for $FW=25$ and $f_R=1.35$, $D=4$, $N=8$, $n=5$). The low-pass filter is $4^{th}$ order Butterworth type.

For fine tuning of output frequency the switching between $FW1$ and $FW2$ can be used. The block diagram of such synthesizer is shown in Fig. 13, and frequency spectrum in Fig. 14. The block diagram used for second frequency synthesizer simulation is shown in Fig. 15.

![Fig. 11. PLL lowpass filter response on $FW$ step.](image)

![Fig. 12. The time response (step response) of the frequency synthesizer (from zero to 9.45) for $FW=25$ and $f_R=1.35$, $D=4$, $N=8$, $n=5$ and 4-th order low-pass filter.](image)

![Fig. 13. The frequency synthesizer with switching control word $FW$.](image)

![Fig. 14. The frequency spectrum of frequency synthesizer (Fig. 13) with switching $FW$ between 24 and 25.](image)
5 Discussion
The simulation results of fractional frequency synthesizer based on flying adder used in feedback and phase locked loop shown good spectral properties and time responses. In comparison with others types of fractional synthesizers, presented principle is much simpler. The maximal and minimal frequency ratio is given by (6).

\[
\frac{f_{\text{OUT MAX}}}{f_{\text{OUT MIN}}} = N
\]  

(6)

and minimal frequency step \(\Delta f\) (without \(FW\) switching) is

\[
\Delta f = f_R ND \frac{1}{2^n}
\]

(7)

When the \(FW\) switching is used the minimal frequency step is \(\Delta f/2\), but frequency spectrum contain more spurious lines.

6 Conclusion
Flying-Adder architecture is an innovative method for frequency synthesis. The effenctness of this technic has been proven by many commercial products in the past few years. The great advantage is that Flying-Adder architecture consists of pure digital circuitry such as multiplexers, adders, and flip-flops, thereby resulting in fast switching time, wide tuning range and therefore enables simple programmable logic construction. In this paper, a two simple frequency synthesizers with a wide tuning range and reduced fractional spurs has been presented and simulated. The proposed approach uses Flying-Adder technique in cooperation with Phase Locked Loop. The trade-off of this approach is that Flying-Adder loses its "instant response" advantage, because in a Phase Locked Loop low-pass filter is included. Consequently, the response time will depend on the settling time of the Phase Locked Loop.

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