Solar Inverter with Multi Stage Filter and Battery Buffering

K. H. Edelmoser,
Institute of Electrical Drives and Machines
Technical University Vienna
Gusshausstr. 27-29, A-1040 Wien
AUSTRIA
kedel@pop.tuwien.ac.at

F. A. Himmelstoss
Technikum Wien
University of Applied Science
Hoechstaedtplatz 5, A-1200 Wien
AUSTRIA
himmelstoss@technikum-wien.at

Abstract: - In common single-phase inverter applications the current of the solar array shows a remarkable ripple due to power pulsation on the grid. This entails two significant disadvantages: Reduced over-all efficiency due to dynamic maximum power point mismatch and reduced lifetime of the panels due to additional component stress. So the elimination of high frequency ripple current on input- and output side is an increasingly important topic. Furthermore in environments with several solar strings operating in parallel to reach the goal of a very close MPP operation, a distributed current source arrangement has to be chosen. On the other hand, several measurements have also to be taken into consideration to keep the output-harmonics in an acceptable range. The proposed topology discussed in this paper uses separated active filters to fulfill the given requirements: Minimized input current ripple of the cells, string-optimized maximum power point tracking and optimal power quality of the supplying grid. The topology presented in this paper shows a remarkable improvement of the over-all efficiency as well as a significantly enhanced EMC. Consequently, it is well suited for solar power inverter applications.

Key-Words: - EMI-Reduction, Inverter, Switching Leg, Solar Energy, PWM, Losses

1 Introduction

State-of-the-art switching mode solar converters arrangements for parallel string operation with input ripple minimization realized with active filtering techniques (c.f. Fig. 1) are well known in the field of power conversion for renewable energy applications.

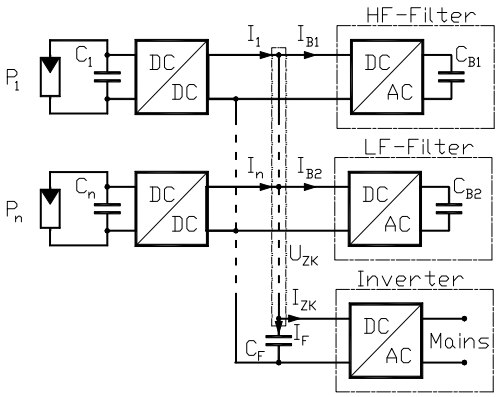

Fig. 1. Innovative solar inverter array with active input ripple compensation, separated to low frequency and high frequency sections and power-line interfacing

The starting point of our investigations was a multi-string solar array with common current sourced DC-link and a mains coupling inverter operating at the European power grid (230V) with an additional active DC-link buffer (back-up battery), given in Fig. 2. In this paper the full concept, using additional energy storage elements is shown, which in-creases the efficiency and the converter output voltage quality to meet high mains quality and reduce EMC problems. To overcome the problem of energy storage in each input cell, an improved current sharing topology with dedicated storage elements was derived based on Figure 1 leading to the pro-posed converter structure depicted in Fig. 3.

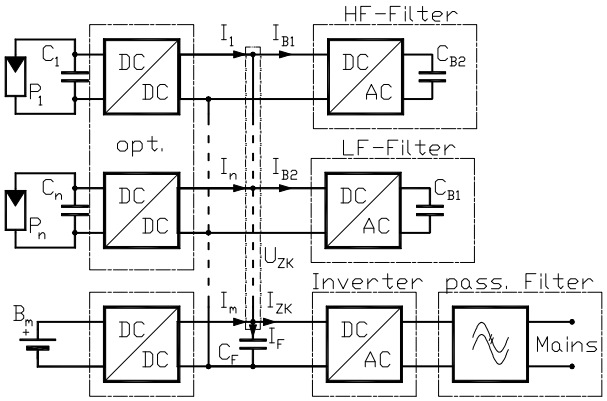

Fig. 2. Topology with additional storage cell on DC-link, first approach with separated filter cells and battery stage

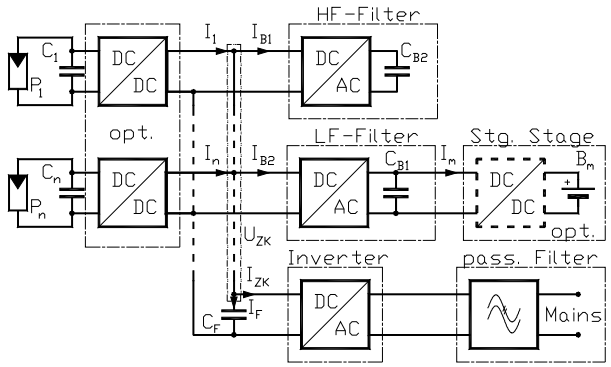

Fig. 3. Suggested topology with additional storage cell on DC-link, second approach: specific HF-filter and combined energy storage and LF-filtering cell

Figure 3 shows a topology with several solar sources adapted by separated MPP-tracking DC-to-DC converters feeding a common DC-link. Based on current summation technique an active filter for low frequency distortion (LF) was used to keep the input current ripple of the solar strings in a tolerable range (2% typically). In addition, another active filter (HF) was added to furthermore reduce the power-line harmonics and eliminate the ripple injected by the LF-filter, so that all EMC requirements can be fulfilled. This filter is supported by the battery cell giving us the feasibility to do a "long time averaging" of the energy flow.

2 The Basic Problem

Solar arrays can be realized in two modes: hard-wired (series-parallel connection of solar strings) and inverter coupled (each string uses its own MPP-tracking inverter), as depicted in Figs. 1, 2 & 3. In this paper a simple hard wired arrangement was used for better demonstration. In most other cases well-known buck current source converters where used to supply the DC-link. Each stage has to be operated on its own MPP to maximize the over all system efficiency [1,2,3,11]. The result is the same as of the used simple arrangement.

In each case, due to the varying array-current, a respectively large averaging energy buffer (C_{IN}) is needed to smoothen the solar arrays current. A standard gauge of approximately 5000µF / kW-peak at 200V solar voltage range is a good starting point to keep the voltage ripple within the recommended 2% of the MPP-voltage [6]. The active filtering lead to a possible reduction of about 1000µF / kW without any further derating.

For mains-interfacing a simple current sourced push-pull inverter topology was used. In our application a transformer isolated main interface is chosen [4,5].

2.1 The Basic Filter Topology

The advantage of this topology is the simplified filter structure for both filters, the low-frequency input-ripple buffer and the medium-frequency ripple filter. A topology as depicted in Fig. 4 will be chosen for the low-frequency filter operating at a rather low switching frequency of 2.5kHz to eliminate switching losses. The main job of this filter is to eliminate the 100Hz (120Hz) current ripple. The second filter, implemented to eliminate the injected low frequency ripple from the previous stage, operates at 25kHz and uses a topology given in Fig. 5.

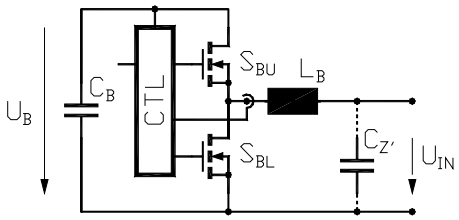

Fig. 4. Proposed active LF filter circuitry, self powered topology

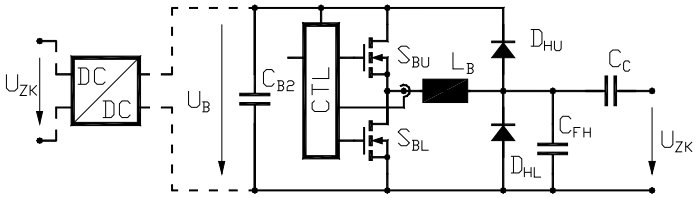

Fig. 5. Proposed active HF filter circuitry with auxiliary loss-covering converter (optional)

Alternatively a combined series cell topology can be used for the LF-filter. The structure given in Fig. 6 shows a possible solution in multi cell arrangement.

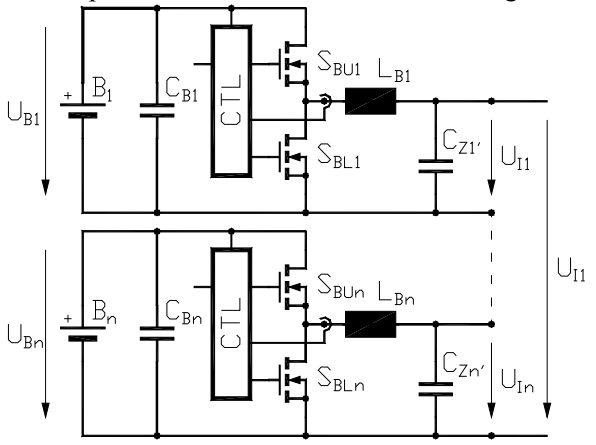

Fig. 6. Proposed battery stage: Cell oriented series topology optimized for battery sharing

Here a significantly reduced current at lower voltage levels has to be maintained. For both stages the simple current mode regulator control principle can

be used leading to an easy to handle solution. The simple principle of current summation is used in combination of an energy storage at higher voltage levels (in our case 400V) (ref.: $W_C=C*U^2/2$). Also a much higher voltage ripple across the filter capacitor can be used without any disadvantage to the circuit behavior. (ref.: $\Delta W_C=C.U.\Delta U$).
Alternatively the battery stage and the filter stage can be separated to eliminate low frequency ripple from the cells. This is a well known solution for using fuel cells to improve the dynamic internal resistor.
Figure 7 depicts the control loops of the demonstration single solar string arrangement with separated MMP-tracking DC-to-DC converter in each solar sting.
The two control loops formed by S1 and S2 have different specifications:

[S1] forms the primary mains ripple cancellation loop operating at a rather low switching frequency, feed from the average solar current given by the MPPT-predictor.

[S2] is used to minimize the switching ripple injected by S1. Its goal is also to keep the high-frequency switching noise in an acceptable range which can be filtered in the mains stage. In our case a simple bang-bang control concept was used. The feeding controller R(s) was used to maintain the LF-filters DC-link to be kept at defined values.

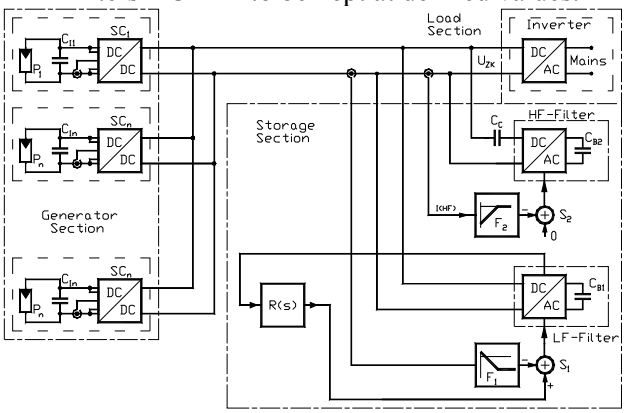

Fig. 7. Compensator control principle for a multi string solar stage system with dedicated MPP-converters (SC1..SCn) and ripple cancellation filtering (inner loop: HF-filter, second loop: LF-filter with optional averaging controller R[s]).

Alternatively to R(s) a band-pass filter can be used to keep the frequency range of the DC-link 100(120)Hz at a minimum.

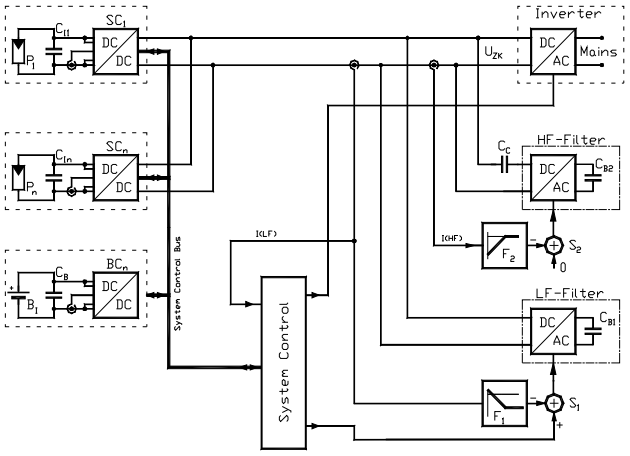

Fig. 8. Compensator control principle for a multi string solar stage system with dedicated MPP-converters (SC1..SCn), additional energy storage cell (BC1) and ripple cancellation filtering (inner loop: HF-filter, second loop: LF-filter with over-all energy management control.

Figure 8 depicts the full topology with separated energy storage cells. In this case a system control section is required to maintain correct energy flow and to control the state of charge of each cell.
It should be noted, that for optimum plant efficiency a load sharing control system should be established. The simple principle of the parallel operation of controlled current sources forms a robust and fault-tolerant system. The proposed topology can be used as an alternative to multi-stage converters with a constant DC-link voltage and an active switching DC-to-AC inverter.

3 System Simulation

To clarify the advantages of the proposed topology, the simplified filter structure for both filters, the low-frequency input-ripple buffer and the medium-frequency output filter a detailed simulation was performed.
As one can be seen in Fig. 9. a state of the art 1.2kW solar string operating at full load has a rather huge cell voltage ripple (about 9% here), even with a rather large storage capacitor (1000µF in this case). A significant improvement of the voltage ripple can be achieved when an active filter stage was used (c.f. Fig. 10). This leads to an improvement of about 10% of the over-all efficiency at the maximum load point.

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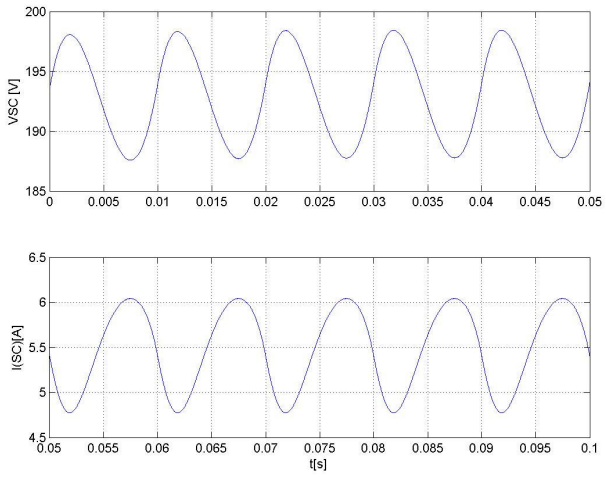

Fig. 9. Input current stress (lower trace) and voltage ripple (upper trace) of a conventional solution delivering 1056W at MPP with 1.2A current ripple (C1 = 1000µF)

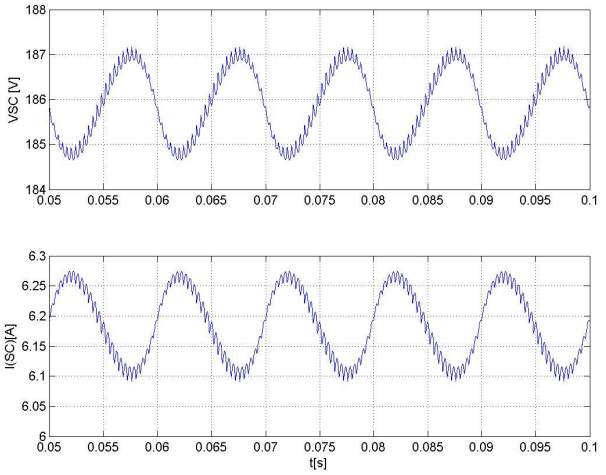

Fig. 10.Input current stress (lower trace) and voltage ripple (upper trace) of a fully ripple compensated system (HF & LF filtering) delivering 1150W at MPP with less than 0.12A current ripple (C1 = 1000µF)

It should be noted that the over-all efficiency, measured on DC-side, rises from 87.5% (conventional) to 96% (full compensation) To clarify the advantages Fig. 11 shows the power density spectrum of the current-DC-link.

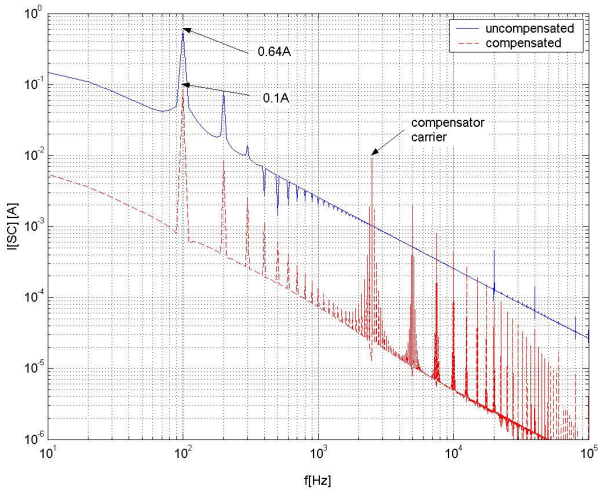

Fig. 11. Comparison of the uncompensated system to the fully compensated solution: As one can see in case of active filter usage the system harmonics are reduced by more than 30dB leading to a rather simple mains interface.

To clarify the behavior of the system Figure 12 shows the input characteristics of the cells. One can see the rather smooth input current and the resulting low input voltage ripple (the goal of less than 2% was reached).

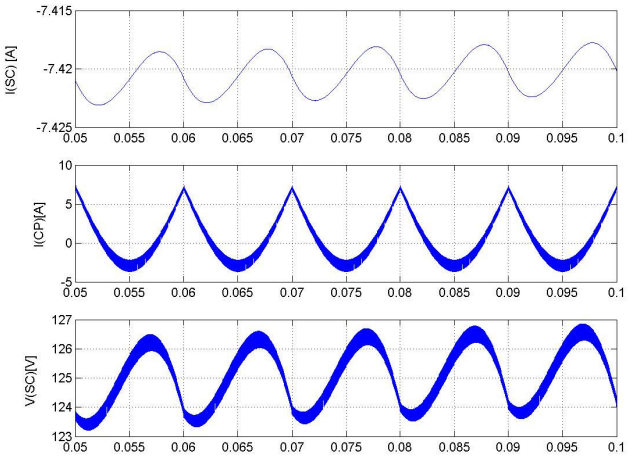

Fig. 12. Conventional compensator arrangement Input current stress, compensation filter current, array voltage ripple (from top to bottom) (P1=1.2kW, 25kHz active bang-bang filter stage)

Here the current is optimally shared between the two filter stages. One can see the significantly smoothed array current leading to an nearly optimal maximum power point with less deviation due to mains current ripple.

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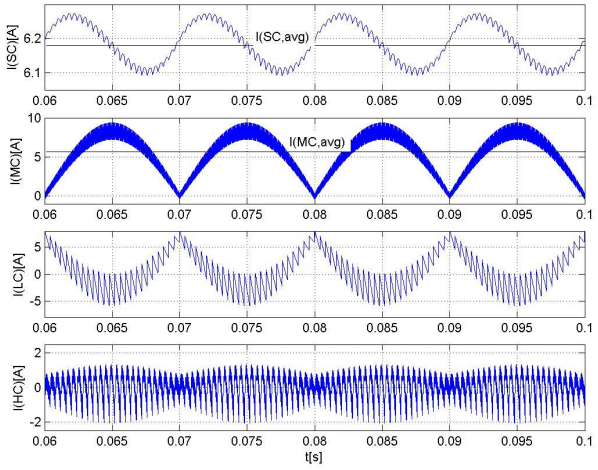

Fig. 13. System behavior of the two-loop compensator: input current stress I(SC), input current of the mains inverter I(MC), LF- and HF-compensation current I(LC), I(HC), (from top to bottom) (P_{SC}=1145W $P_{LF,AVG}$=0W, $P_{HF,AVG}$=0W, P_{MC}=1121W).

Figure 13 shows the operating system without long time energy storage active. One can see that there is no resulting average energy delivered or consumed from the cells or mains. Contrary to this settings in Fig. 14 the low-frequency filter is used to deliver power from the batteries into the mains.

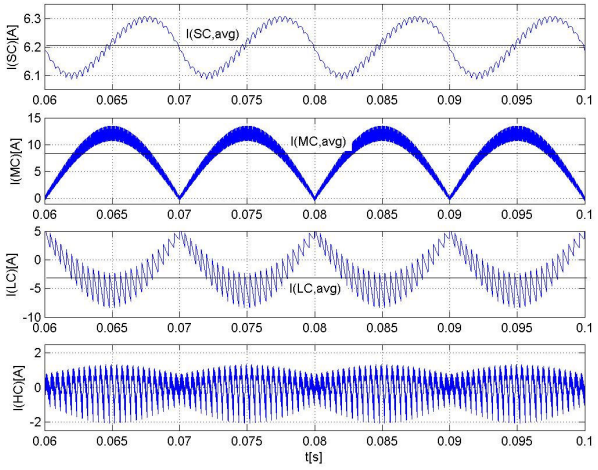

Fig. 14. Detailed system behavior of the two-loop compensator with energy storage in the LF section (battery buffer): input current stress I(SC), input current of the mains inverter I(MC), LF- and HF-compensation current I(LC), I(HC), (from top to bottom) (P_{SC}=1090W $P_{LF,AVG}$=363W, $P_{HF,AVG}$=0W, P_{MC}=1311W).

Due to the current disposing in two stages a significant improvement of the efficiency as well as component reliability in solar-, fuel cell- and battery fed inverter applications by an active reduction of the source current ripple can be achieved.

As a result the source is only loaded with a nearly perfect DC-current, which helps to hit the maximum power point without any dynamic distortions. Furthermore, the input capacitor can be decreased, because a common energy storage element is used operating at higher voltages with higher efficiency. Here under several circumstances also batteries can be used giving the possibility of building an redundant UPS-system,.

The power stage of the used filter consists of a simple half bridge arrangement feeding the ripple cur-rent. The converter is operated at several 1kHz and 10kHz respectively leading to a tolerable low out-put current ripple.

The effective usage of multi-phase input cells coupled with an active filter show us the capability to reach the goal of high efficiency, reduced current harmonics and improved EMC.

4 Conclusion

The proposed solution improves efficiency as well as component reliability in solar-, fuel cell- and battery-fed inverter applications by an active reduction of the source current ripple. As a result, the source is only loaded with a perfect DC-current, which helps to hit the maximum power point without any dynamic distortions. Furthermore, the input capacitor can be decreased, because a common energy storage element is used operating at higher voltages with higher efficiency. It should be noted, that for optimum plant efficiency a load sharing control system should be established. The simple principle of the parallel operation of controlled current sources forms a robust and fault-tolerant system. The pro-posed topology can be used as an alternative to multi-stage converters with a constant DC-link voltage and an active switching DC-to-AC inverter.

The power stage of the used filter consists of a simple half bridge arrangement feeding the ripple cur-rent. The converter is operated at several 10kHz leading to a tolerable low output current ripple. Cheap TO-247 or even TO-220 or cheap surface mount packages can be used leading to a compact and efficient system design [6,7,8,9,10].

The effective usage of multi-phase input cells coupled with an active filter shows us the capability to reach the goal of high efficiency, reduced current harmonics and improved EMC.

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Furthermore, it should be noted that the parallel structures are forming a redundant system which can be used to increase the systems reliability by building a fault tolerant arrangement. All these advantages can simply be realized in software and do not affect the hardware.

The simple control principle of the power stages can easily be implemented using state-of-the-art microcontrollers without additional logic support for the pulse pattern generator; a simple PWM stage fulfills all the requirements. Also the maximum power point tracking for the solar generator can be easily implemented by monitoring the system signals (i_1 .. i_N , and i_{ZK}.).

The topology presented in this paper is a simple and effective solution for small to medium power grid coupled applications. The concept is well suited for wind-, solar- and renewable energy as well as for aerospace applications.

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