

Optimized Design of Decimator for Alias Removal in Multirate DSP Applications

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Abstract: - Decimator is an important sampling device used for multi-rate signal processing in wireless communication systems. In this paper optimized decimator has been presented to improve the implementation complexity. The proposed decimator is implemented using Matlab as standard FIR, Half Band FIR and Nyquist FIR by using the multistage design techniques. The performance of different decimator designs is compared in terms of error and hardware requirements. The results show that the performance of all designs is almost identical but their implementation cost varies greatly in terms of hardware requirements. The hardware saving of 49% to 84% can be achieved by using multistage Nyquist decimator design.

Key-Words: - DSP, Decimator, FIR, Multirate, NTSC, PAL

1 Introduction

The widespread use of digital representation of signals for transmission and storage has created challenges in the area of digital signal processing [1]. The applications of digital FIR in up and down sampling techniques are found everywhere in modern electronic products. For every electronic product, lower circuit complexity is always an important design target since it reduces the cost [2]. There are many applications where the sampling rate must be changed. Interpolators and decimators are utilized to increase or decrease the sampling rate [3]. For example, in digital audio three different sampling rates are used like 32 KHz for broadcasting, 44.1 KHz for digital CD and 48 KHz for digital audio tape. In video applications, the sampling rates of NTSC and PAL are 14.318 MHz and 17.734 MHz respectively.

The rate conversion requirement leads to production of undesired signals associated with aliasing and imaging errors. So some kind of filter should be placed to attenuate these errors [4]. There are two basic sampling rate alteration devices in addition to Conventional elements such as an adder, a multiplier, and a delay. Discrete time systems with Unequal sampling rates at various parts are called multi rate systems. Multirate systems are building blocks commonly used in digital signal processing (DSP). Their function is to alter the rate of the discrete-time signals, by adding or deleting a portion of the signal samples. They are essential in

various standard signal processing techniques such as signal analysis, denoising, compression and so forth. During the last decade, however, they have increasingly found applications in new and emerging areas of signal processing, as well as in several neighboring disciplines such as digital communications. The multirate DSP in the communication systems serves to provide additional degrees of freedom in the design of the receiver. Another important class of multirate structures is used at the transmitter side in order to introduce the redundancy in the data stream. This redundancy generally serves to facilitate the equalization process by forcing certain structure on the transmitted signal. If the channel is unknown, this procedure helps to identify it; if the channel is ill-conditioned, additional redundancy helps avoid severe noise amplification at the receiver, and so forth.

The digital signal processing application by using variable sampling rates can improve the flexibility of a software defined radio. It reduces the need for expensive anti-aliasing analog filters and enables processing of different types of signals with different sampling rates. It allows partitioning of the high-speed processing into parallel multiple lower speed processing tasks which can lead to a significant saving in computational power and cost. Wideband receivers take advantage of multirate signal processing for efficient channelization and offers flexibility for symbol synchronization.

2 Decimators

Typically lowpass filters are used for decimation and for interpolation. When decimating, lowpass filters are used to reduce the bandwidth of a signal prior to reducing the sampling rate. This is done to minimize aliasing due to the reduction in the sampling rate. When decimating, the bandwidth of a signal is reduced to an appropriate value so that minimal aliasing occurs when reducing the sampling rate.

Down sampler is basic sampling rate alteration device used to decrease the sampling rate by an integer factor [5]. An down-sampler with a down-sampling factor M , where M is a positive integer, develops an output sequence $y[n]$ with a sampling rate that is $(1/M)$ -th of that of the input sequence $x[n]$. The down sampler is shown in Fig1.

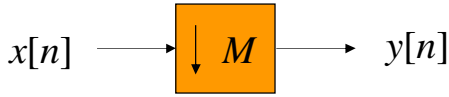


Fig.1 Down Sampler

Down-sampling operation is implemented by keeping every M^{th} sample of $x[n]$ and removing $M-1$ in-between samples to generate $y[n]$. The input and output relation of down sampler can be expressed as:

$$y[n] = x[nM] \tag{1}$$

Applying the z -transform to the input-output relation of a factor-of- M down-sampler, we get

$$Y(z) = \sum_{n=-\infty}^{\infty} x[Mn] z^{-n} \tag{2}$$

The expression on the right-hand side of Eq (2) cannot be directly expressed in terms of $X(z)$. To get around this problem, a new sequence $x_{\text{int}} [n]$ can be expressed as:

$$x_{\text{int}} [n] = \begin{cases} x[n], & n = 0, \pm M, \pm 2M, \dots \\ 0, & \text{otherwise} \end{cases} \tag{3}$$

Then

$$\begin{aligned} Y(z) &= \sum_{n=-\infty}^{\infty} x[Mn] z^{-n} = \sum_{n=-\infty}^{\infty} x_{\text{int}} [Mn] z^{-n} \\ &= \sum_{k=-\infty}^{\infty} x_{\text{int}} [k] z^{-k/M} = X_{\text{int}} (z^{1/M}) \end{aligned} \tag{4}$$

Now, $x_{\text{int}} [n]$ can be formally related to $x[n]$ as follows:

$$x_{\text{int}} [n] = c[n] \cdot x[n] \tag{5}$$

Where

$$c[n] = \begin{cases} 1, & n = 0, \pm M, \pm 2M, \dots \\ 0, & \text{otherwise} \end{cases} \tag{6}$$

A convenient representation of $c[n]$ is given by

$$c[n] = \frac{1}{M} \sum_{k=0}^{M-1} W_M^{kn} \tag{7}$$

Where

$$W_M = e^{-j2\pi/M}$$

Taking the z -transform of Eq.(5) and by making use of Eq.(7), we get

$$X_{\text{int}} (z) = \frac{1}{M} \sum_{n=-\infty}^{\infty} \left(\sum_{k=0}^{M-1} W_M^{kn} \right) x[n] z^{-n} \tag{8}$$

$$= \frac{1}{M} \sum_{k=0}^{M-1} \left(\sum_{n=-\infty}^{\infty} x[n] W_M^{kn} z^{-n} \right) \tag{9}$$

$$= \frac{1}{M} \sum_{k=0}^{M-1} X(z W_M^{-k})$$

The spectrum of a factor-of-2 down-sampler with an input $x[n]$ is shown in Fig2.

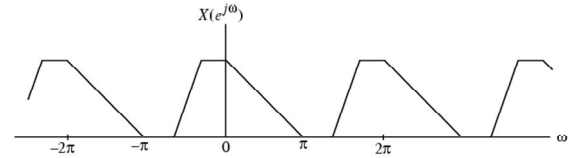


Fig.2 Spectrum of Down Sampler

The DTFTs of the output and the input sequences of this down-sampler are then related as

$$Y(e^{j\omega}) = \frac{1}{2} \{ X(e^{j\omega/2}) + X(-e^{j\omega/2}) \} \tag{10}$$

The second term in above equation is simply obtained by shifting the first term $X(e^{j\omega/2})$ to the right by an amount 2π as shown in Fig3. The two terms have an overlap due to which original “shape” of $X(e^{j\omega/2})$ is lost when $x[n]$ is down-sampled. This overlap causes the *aliasing* that takes place due to under-sampling. There is no overlap, i.e., no aliasing, only if

$$X(e^{j\omega}) = 0 \quad \text{for } |\omega| \geq \pi/2 \tag{11}$$

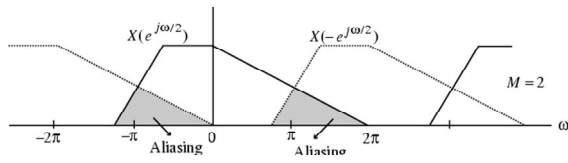


Fig.3 Aliasing Effect

In general, Aliasing is absent if and only if

$$X(e^{j\omega}) = 0 \text{ for } |\omega| \geq \pi / M \quad (12)$$

To overcome the effect of aliasing decimation filters are used. The specifications for the lowpass decimation filter are given by

$$|H(e^{j\omega})| = \begin{cases} 1, & |\omega| \leq \omega_c / M \\ 0, & \pi / M \leq |\omega| \leq \pi \end{cases} \quad (13)$$

3 Proposed Decimator Design

When decimating, the bandwidth of a signal is reduced to an appropriate value so that minimal aliasing occurs when reducing the sampling rate. An acceptable transition width needs to be incorporated into the design of the lowpass filter used for decimation along with passband ripple and finite stopband attenuation. In this proposed work decimator is designed using 0.01 transition width, 0.02dB pass band ripples, 60dB stop band attenuation and decimation factor of 8.

Equiripple based decimator has been designed and analyzed using Matlab [6] for single stage, two stages and multi stages with Nyquist and standard techniques. It can be seen from the results of Fig4 that proposed Nyquist multistage design provide same stop band attenuation and transition width with a much lower order.

The main advantage of multistage over single stage designs is that longer filters are costly and can be operated at lower sample rates while shorter filters are operated at higher sample rates. An L th-band filter for $L = 2$ is called a half-band filter. The transfer function of a half-band filter is thus given by

$$H(z) = \alpha + z^{-1}E_1(z^2) \quad (14)$$

with its impulse response satisfying

$$h[2n] = \begin{cases} \alpha, & n = 0 \\ 0, & \text{otherwise} \end{cases} \quad (15)$$

In Half band filters about 50% of the coefficients of $h[n]$ are zero. This reduces the number of multiplications required in its implementation significantly. The comparison of standard FIR decimator, half band decimator and Nyquist decimation is shown in Fig4.

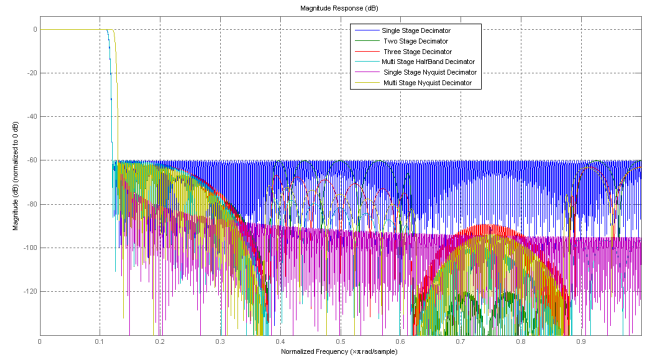


Fig.4 Performance comparison of all designs

Half band filters can be implemented using FIR and IIR design techniques. FIR designs have an additional advantage in that every other coefficient is equal to zero.

Let the signal to be filtered has a flat spectrum. Once filtered, it acquires the spectral shape of the filter. After reducing the sampling rate, this spectrum is repeated with replicas centered on multiples of the new lower sampling frequency. Fig.5 shows that the replicas overlap, so aliasing is introduced. However, the aliasing only occurs in the transition band.

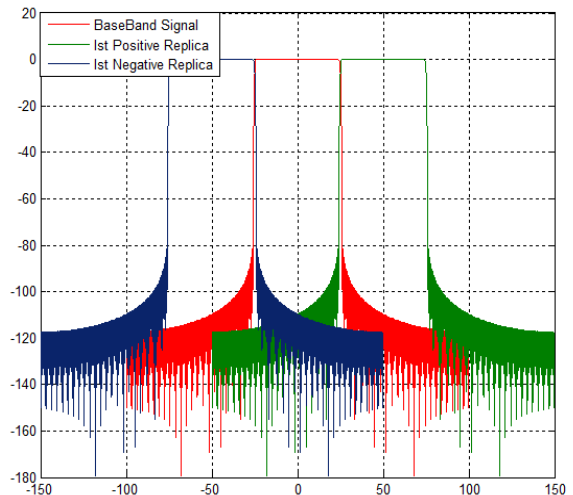


Fig.5 Aliasing due to down sampling

In Fig.6, although we have used the same transition width as with the earlier low pass design but retaining the maximum usable band by using the Nyquist method.

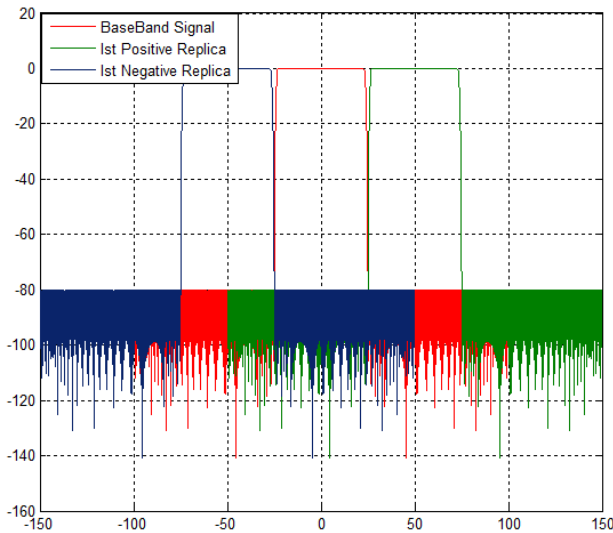


Fig.6 Alias Removal by Nyquist Design

4 Implementation Results & Discussions

The implementation cost of all the six designs have been analyzed and compared. The performance of the all designs is almost identical but their implementation cost varies greatly, as shown in the table1. The Nyquist multi stage design provides significant savings both in terms of hardware and operations per sample as compared to other designs. The proposed Nyquist multistage decimator results in 84% hardware saving as compared to Nyquist single stage, 49% as compared to standard multistage design and 48.9% as compared to half band multistage design.

Table1. Implementation Cost

Design	Implementation Cost Comparison			
	Mult	Add	MPIS	APIS
Std. Single Stage	649	648	81.12	81
Std. Two Stage	199	197	28.25	27.87
Std. Multi Stage	195	192	29.9	28.62
HB Multi Stage	188	185	27.25	26.37
Nyq Single Stage	637	636	79.62	79.5
Nyq Multi Stage	99	96	15.37	14.5

The results also show significant improvement in MPIS (Multiplications Per Input Sample) and APIS (Additions Per Input Sample) in case of Nyquist multi stage design as compared to other designs.

5 Conclusion

In this paper, decimator is implemented and analyzed using different designs. The results show that performance of the all designs is almost identical but their implementation cost varies greatly in terms of hardware requirements. The Nyquist multistage decimator design results in alias removal and improved area utilization ranging from 49% to 84%. So multistage Nyquist decimators are the best to perform down sampling and provide cost effective solutions for DSP based wireless communication applications.

References:

- [1] Vijay Sundararajan, Keshab K. Parhi, "Synthesis of Minimum-Area Folded Architectures for Rectangular Multidimensional", IEEE TRANSACTIONS ON SIGNAL PROCESSING, pp. 1954-1965, VOL. 51, NO. 7, JULY 2003.
- [2] ShyhJye Jou, Kai-Yuan Jheng*, Hsiao-Yun Chen and An-Yeu Wu, "Multiplierless Multirate Decimator / Interpolator Module Generator", IEEE Asia-Pacific Conference on Advanced System Integrated Circuits, pp. 58-61, Aug-2004.
- [3] Shahriar Emami "New Methods for Computing Interpolation and Decimation Using Polyphase Decomposition", IEEE TRANSACTIONS ON EDUCATION, pp. 311-314, VOL. 42, NO. 4, NOVEMBER 1999.
- [4] Amir Beygi, Ali Mohammadi, Adib Abrishamifar. "AN FPGA-BASED IRRATIONAL DECIMATOR FOR DIGITAL RECEIVERS" in 9th IEEE International Symposium on Signal Processing and its Applications, pp. 1-4, ISSPA-2007.
- [5] S K Mitra, Digital Signal Processing, Tata Mc Graw Hill, Third Edition, 2006.
- [6] Mathworks, "Users Guide Filter Design Toolbox-4", March-2007.