Design of Integrated CMOS LNA using Suspended MEMS Inductor for Wireless Applications

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Abstract: - The interest in low-cost, low-power, silicon-based transceiver designs for radio frequency (RF) applications, such as cell phones and wireless sensor networking, has prompted research in wireless circuit design techniques using complementary-metal-oxide-semiconductor (CMOS) technology. A critical limitation in obtaining fully integrated CMOS wireless systems is the lack of high quality of the on-chip passive components, and in particular, on-chip inductors. In this paper design of integrated CMOS LNA using suspended MEMS Inductor for wireless applications is presented. Modeling and designing of the on-chip spiral inductor is the main objective of this work. Measurements and characterization results are presented in this work.

Key-Words: - Spiral inductor, MEMS inductor, MEMS technology, High Q-factor.

1 Introduction

Wireless communication triggers the research and development of RF integrated circuits (RF IC), and the rapid growing market for more portable and low cost equipments motivates the single chip with RF front-end and digital process or integrated together. This trend makes CMOS RF IC more attractive in the competition with its counterparts. CMOS low noise amplifier (LNA) is an important component in RF communication receiver. The noise performance of LNA determines the noise performance of the entire system. Therefore, to improve the sensitivity of the receiver, the noise figure of the LNA must be minimized and enough gain must be provided. Finding ways to reduce the noise figure of the CMOS LNA while using on-chip passive components becomes the greatest challenge in front of us. Its gain not only affects the linearity of the next circuit block, but also defines the overall noise performance. And its impedance matching is very important for maximum power transfer. Recently, with the rapid growth of the demands in wireless communication products such as mobile phones and wireless network, low cost and high performance on-chip radio-frequency devices are strongly needed. One important limitation in achieving higher levels of integration and further reduction of fabrication costs in the front-end of microwave transceivers is set by the difficulty of achieving high-Q on-chip inductors.

The approach used in this paper is the use of silicon micromachining techniques to remove the substrate underneath the planar inductors such that to increase both the inductor self-resonant frequency f_{srf} and quality factor Q.

LNA design used in this research from a paper "MOS COMMON-SOURCE LNA Design Tutorial" by J P Silver where the LNA circuits were simulated using ideal inductor with no losses and the output was compared to the circuit simulation using the designed MEMS inductors.

2 Inductors Design and Model

Three rectangular spiral inductors have been designed using and simulated using ADS. The spiral inductors have a 1 μm aluminum line thickness Table 1 lists the number of turns, line spacing, and line width for these di spirals.

Table 1 Spirals different geometries.

Device Number	N number of turns	S line spacing (μm)	W line width (μm)	Di Inner Diameter (μm)
1	1.5	5	10	100
2	2.5	5	20	175
3	3.5	5	20	165

The S-parameters which are calculated using ADS then transformed into the Y-parameters from which the

inductance L and Q factor can be calculated based on the following equations [13], respectively:

$$L = \mathrm{Im}(1/Y)/2\pi f \quad (1)$$

$$Q = \mathrm{Im}(1/Y)/\mathrm{Re}(1/Y) \quad (2)$$

Where: Y are the Y-parameters and f is the signal frequency.

3. Simulation Results

There exists a trade-off between the inductance and quality factor when increasing the number of turns of a spiral inductor. Table 1 shows a summery for the values of inductance L at frequency of 2.4 GHZ and maximum quality factor Q due to the change in the number of turns for the three spiral inductors. It can be seen from the table that when increasing the number of turns, the inductance increases while Q and self resonance frequency *SRF* decrease.

Figures 1, 2 and 3 show the Quality factor graph against the frequency for the three inductors.

Inductor name	Max. Quality Factor	Frequency GHZ	Inductance (nH) at 2.4 GHZ
1	24.983	17.8	0.651
2	16.978	7.2	2.616
3	13.399	5	4.23

Table 1 Summery of inductance L and Quality factor Q

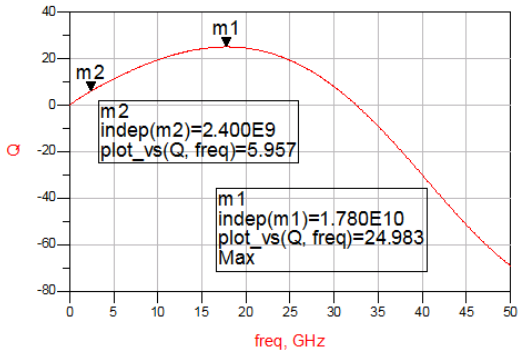

Fig 1 The Q of 1.5 turns inductor

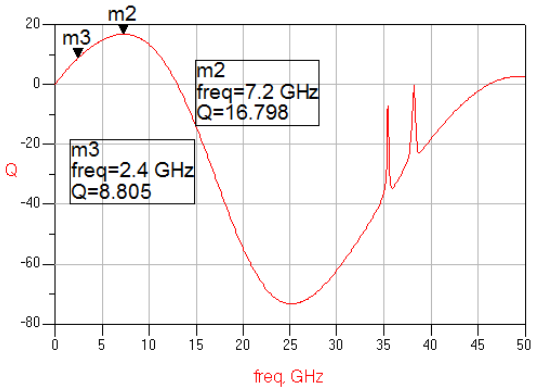

Fig 2 The Q of 2.5 turns inductor

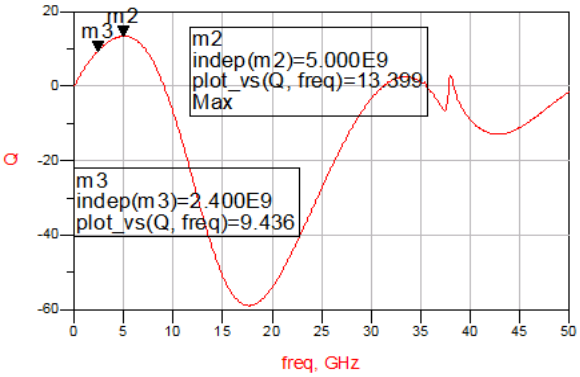

Fig 2 The Q of 2.5 turns inductor

4. Low noise amplifier

For the LNA design we will be using the Agilent CMOS14 0.5 µm process that allows a minimum gate length Lmin= 0.6 µm

Two LNA circuit were drown using ADS the first one is a single stage and the second one is after the addition of a cascode stage.

For each LNA, the simulation is performed in two steps as follows:

1) The circuit is simulated using ideal inductors where the values of the inductor meets the design requirements according to the above analysis and the results for the gain and noise figure was calculated and plotted

2) The circuit is simulated with the practical inductors designed and the results for the gain and noise figure is calculated and plotted

4.1 Single stage with Ideal inductors:

In this design Lg and Ls were calculated for input matching such that to fulfill maximum power transfer to the output.

Adding a current mirror circuit which would apply a constant current Id to the MOSFET as a biasing current in order to make the MOSFET work at the biasing point

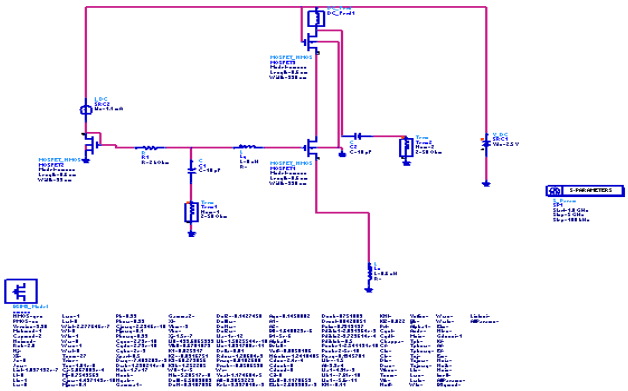

Fig 4 Single stage LNA with Ideal inductors

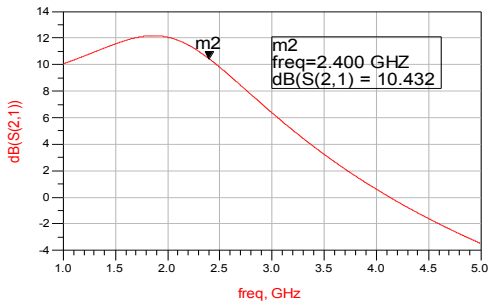

Fig 5 Simulation results for the Gain

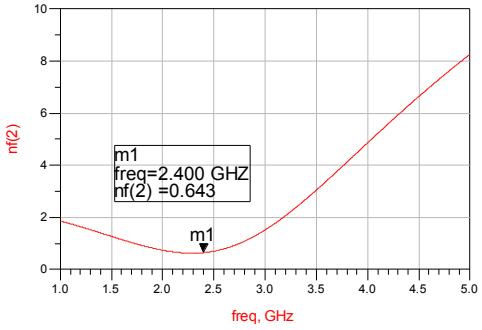

Fig 6 simulation results for Noise Figure

As shown in figure 4 and 5 the minimum noise figure of 0.643 for the single stage LNA circuit with ideal inductor was reached at frequency of 2.4 GHZ and the equivalent gain at the same frequency was 10.432 dB

4.2 Single stage with MEMS inductors:

Using the gate inductor can add significant noise to the LNA so in order to minimize the effect of the inductor on the noise figure, the size of Cgs can be increased, thus making Lg smaller, which can be done either by making the transistor wider, which perhaps can result in higher power consumption, or by adding an extra capacitor parallel to gate inductor as shown in figure 6.

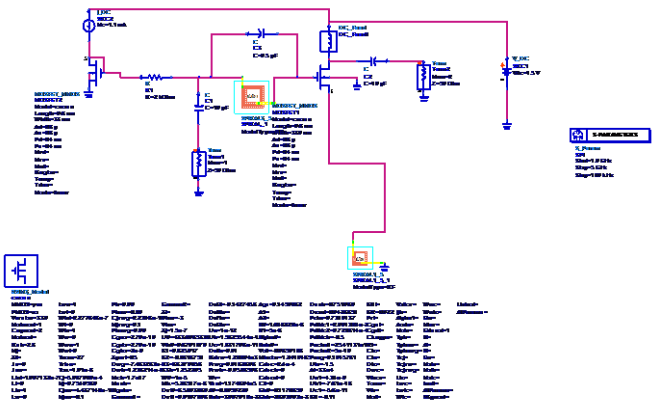

Fig 7 Single stage LNA with MEMS inductors for Lg and Ls

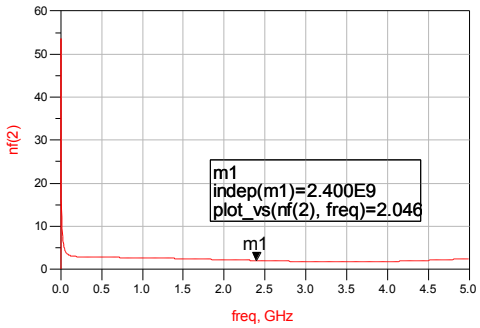

Fig 8 simulation results for the Noise figure

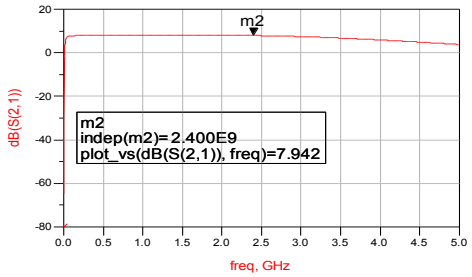

Fig 9 Simulation results for the Gain

As seen from figure 6 a shunt capacitor Cg was added to Lg and as the first part in the simulation was by using the 1.5 turns inductor as Ls and the 2.5 inductor as Lg so the shunt capacitor Cg was calculated where Cg = 1.924 pF.

As from figure 7 and 8 the noise figure of 2.04 for the single stage LNA circuit with MEMS inductor was reached at frequency of 2.4 GHZ and the equivalent gain at the same frequency was 7.942 dB.

By using the 1.5 turn inductor as Ls and the 3.5 turn inductor as Lg and the shunt capacitor Cg was calculated and inserted in the design where Cg = 0.5 pF the simulation figures is shown below.

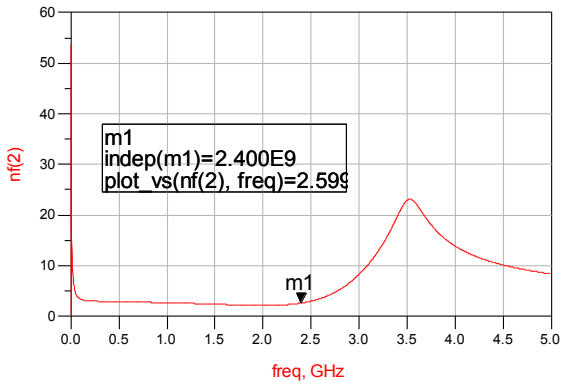

Fig 10 Noise figure for LNA

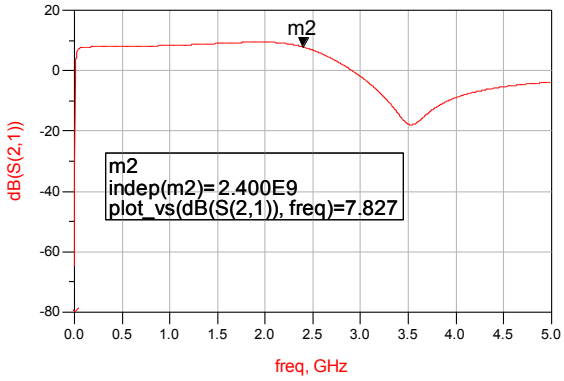

Fig 11 Gain for LNA

As in figure 9 and 10 the noise figure of 2.59 for the single stage LNA circuit with MEMS inductor was reached at frequency of 2.4 GHZ and the equivalent gain at the same frequency was 7.827 dB

4.2 Cascode stage LNA with ideal inductor

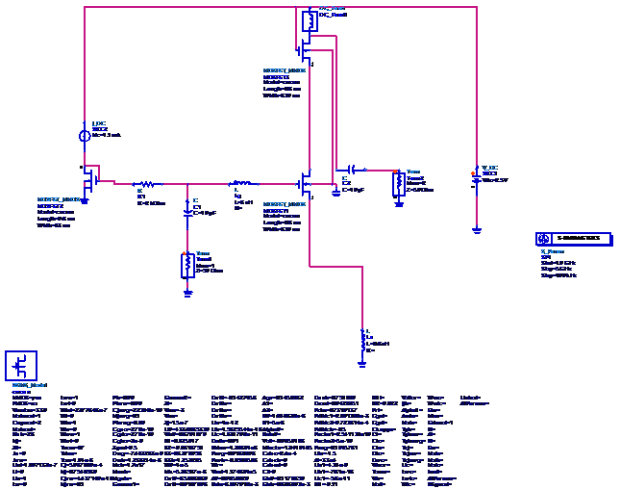

Fig 12 LNA with Cascode stage and Ideal inductors

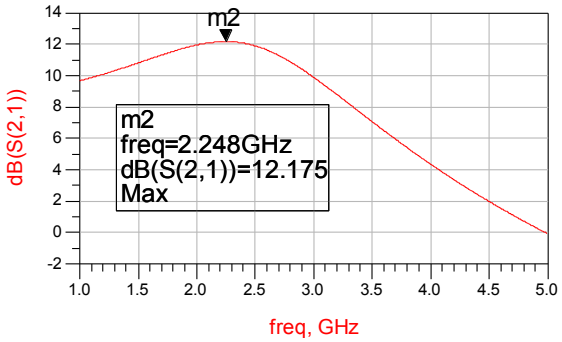

Fig 13 Gain for LNA Cascode stage

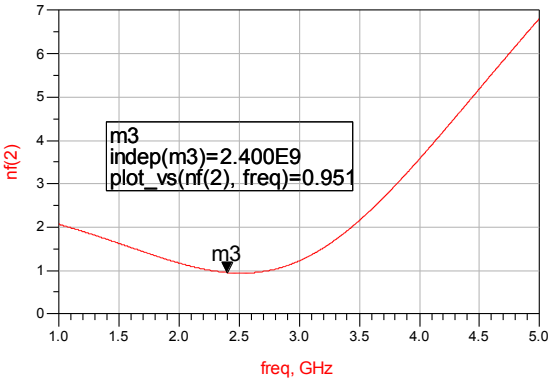

Fig 14 Noise Figure for LNA cascode stage

By applying the MEMS inductors in LNA cascode circuit and applying the simulations as above the results as follows:

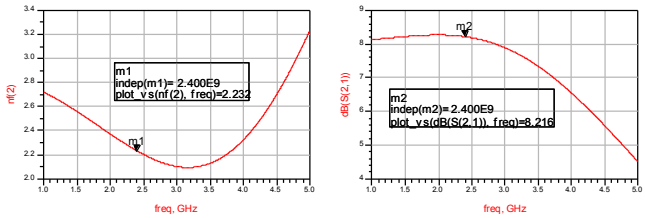

Fig 15 Simulation results for Gain and noise figure after adding MEMS inductors Ls and Lg

According to figure 15 the noise figure of 2.232 for the cascode stage LNA circuit with Lg of 2.5 turns was reached at frequency of 2.4 GHZ and the equivalent gain at the same frequency was 8.216 dB.

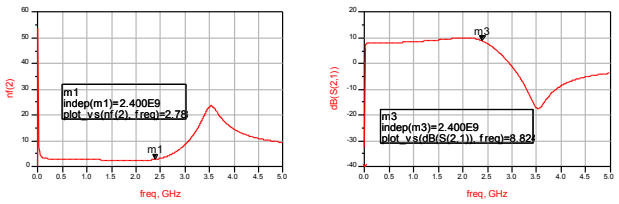

Fig 16 Simulation results for Gain and noise figure after adding MEMS inductor

As shown in figure 16 the noise figure of 2.87 in the cascode stage LNA circuit with Lg of 3.5 turns inductor was reached at frequency of 2.4 GHZ and the equivalent gain at the same frequency was 8.82 dB

5 Conclusion and Discussion

By the end of this paper one can see the possibilities of MEMS technology and the opportunities it presents. Due to its low cost and low power and its miniature sizes, it is no wonder that more and more designers are building their circuit using MEMS. Still though one main obstacle, but can be overcome as seen in this paper, is the low-quality passive components, especially the on-chip inductor. There still needs to be more research invested in this field to come up with advancements for better tools and integration. However, for the time being, the performance of the inductors is sufficient enough for today‟s systems. But as systems tend to operate at higher frequencies, better Q factors for spiral inductors need to be designed in order to operate well at these high frequencies. A possible future work, if GOD wills, is to in fact fabricate the whole LNA, including all its passive components, in particular the spiral inductor, and to actually measure its performance and compare it to the results in this paper; perhaps even try to improve its performances.

References

[1] J.P.Carmo, J.H.Correia, “low-power/low-voltage RF micro-systems for wireless sensor network”, microelectronics journal, vol. 40 (2009) 1746–1754

[2] Chik Patrick Yue “On-Chip Spiral Inductor for Silicon-Based Radio-Frequency Integrated Circuits” 1998

[3] Deepak Uttamchandani and Lijie Li “Design and Characterization of a Radio Frequency MEMS Inductor Using Silicon MEMS Foundry Process” Department of Electronic and Electrical Engineering University of Strathclyde, Glasgow G1 1XW, UK March 2008

[4] E. Hegazi, H. Sjoland and A. Abidi, “A Filtering Technique to Lower LC Oscillator Phase Noise,” IEEE International Solid State Circuits Conference, 2001.

[5] Yu Cao, Robert A. Groves, Xuejue Huang, Noah D. Zamdmer, Jean-Olivier Plouchart, Richard A. Wachnik,Tsu-Jae Ki, *IEEE*, and Chenming Hu, “Frequency-Independent Equivalent-Circuit Model for On-Chip Spiral Inductors” IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 38, NO. 3, MARCH 2003

[6] Sunderarajan S. Mohana Maria del Mar Hershenson "Simple Accurat Experssions for Planner Spiral Inductance" IEEE Journal of solid state circuits VOL ,34, No.10 October 1999

[7] Amal Zaki "Design and Fabrication of High-Q Spiral Inductors Using MEMS Technology" Electronics Research Institute Cairo, Egypt

[8] Juin J. Liou " On-Chip Spiral Inductors for RF Applications" Electrical and Computer Engineering Dept. University of Central Florida, Orlando, FL, USA

[9] Ching-Liang Dai, Jin-Yu Hong and Mao-Chen Liu, "High Q-factor CMOS-MEMS inductor", DTIP of MEMS and MOEMS, Author manuscript, published in "DTIP 2008, Nice : France (2008)"

[10] Pablo Moreno Galbis and Mohammad Hekmat, "Design of a CMOS Low-Noise Amplifier" EE314 Project Report, 2006

[11] Alam, S.K. DeGroat "A 1.5-V 2.4 GHz Differential CMOS Low Noise Amplifier for Bluetooth and Wireless LAN Applications", Circuits and Systems, 2006 IEEE North-East Workshop on

[12] Sedra,Smith "microelectronic circuits" fifth edition, New York:Oxford,2004 pp.28,pp.270-280

[13] Professor P.R. Mukund "A 2.4 GHz Low Noise Amplifier", Imre Knausz , 2004, pp.118

[14] J. P. Carmo, P. M. Mendes, C. Couto, J. H. Correia "2.4 GHz wireless sensor network for smart electronic shirts" Polytechnic Institute of Braganca, Campus Santa Apolonia, 5301-857, Braganca, Portugal University of Minho, Dept. Industrial Electronics

[16] Krzysztof Iniewski, "Wireless Technologies, Circuits, Systems, and Devices", 2008 by Taylor & Francis Group, pp.305-318

[18] Kittichai Phansathitwong Henrik Sjöland, "A 0.18um CMOS Dual-Band Receiver Front end", Analog and RF Group CCCD

[19] J P Silver, "MOS COMMON-SOURCE LNA Design Tutorial".