A sub-1V Bandgap Reference with area reduction

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Abstract: - Bandgap Reference (BGR) is a circuit which generates voltage to be independent of PVT (process, voltage, temperature). This circuit is used in most of analog circuits. This paper proposes a new BGR circuit using resistance and BGR ratio 1:1 which decreases reference variation. The new BGR circuit also decreases the chip size. The proposed circuit was designed as a typical 0.18um CMOS process with current Mirror sizing to reduce the BJT chip area.

Key-Words: - Bandgap reference, voltage regulator, reference voltage, low voltage, CMOS bandgap, BGR, )

1 Introduction
A bandgap reference circuit generates robust voltage against temperature, power supply and process variations[1]. The circuit is widely used to provide stable current and voltage references in analog circuits as well as mixed-mode CMOS circuits. Conventional bandgap reference circuit is composed of PTAT and CTAT section. Here, \( V_{BE} \) (BJT base-emitter voltage) has a negative temperature coefficient, whereas \( V_T \) (thermal voltage) has a positive temperature coefficient. Thus, \( V_{ref} \) is controlled to be about 1.25V where \( V_{ref} \) temperature dependence becomes negligibly small. In the conventional bandgap reference circuit, the output voltage is usually about 1.25V, which is almost equal to the silicon energy gap, measured in electron volts. This bandgap reference circuit cannot be used in the latest deep-submicron technologies whose supply voltage is already in the 1-V range. So, the low voltage bandgap circuit has been proposed[1][2][3]. In this paper, the low voltage bandgap circuit architecture was based on designed[2][4][5][6]. And for reduce the chip area, using the PNP ratio instead of current ratio.

2 Conventional BGR circuit
The conventional BGR circuit is shown in Figure 1. This circuit is made up of CMOS OP-Amp, BJT and resistance. The input voltages of OP-Amp, \( V_a \) and \( V_b \) are controlled by the same voltage. It is expressed as (1).

\[
dV_{BE} = V_{BE1} - V_{BE2} = V_T \cdot \ln\left(\frac{V_T - R_B}{R_1}\right)
\]

The output voltage \( V_{ref} \) is expressed as

\[
V_{ref} = V_{BE1} - \frac{R_2}{R_2} \cdot \frac{dV_{BE}}{V_{BE}} - V_{ref} - \alpha V
\]

\( V_{BE1} \) has a negative temperature coefficient, whereas \( V_T \) as a positive temperature coefficient, so that \( V_{ref} \) is determined by the ratio of the resistance as well as are ratio of the bipolar transistor. This circuit topology can generate the reference voltage of 1.25V by adjusting the resistor ratio and BJT’s area ratio. However, this topology is not used in low supply voltage operation.

Conventional bandgap reference circuit cannot be used in supply voltage is already in the 1-V range \( V_{ref} \) hold the value 1.2V. So design is limited to conventional architecture. The circuit in Figure 2 bandgap circuit can be operated low voltage. The input voltages of OP-Amp, \( V_a \) and \( V_b \), are controlled to be the same voltage. And the gates of MOSFETs \( P_1, P_2 \) and \( P_3 \) are connected to a common node forming a current mirror and therefore the currents \( I_1, I_2, I_3 \) are of same value. Also \( R_1 \) and \( R_2 \) are the same, and the PNP BJT of \( Q_1 \) and \( Q_2 \) are equal.
Fig. 2 Conventional low voltage BGR circuit

It is expressed as
\[ I_1 = I_2 = I_3 \]  
\[ J_1 = J_2 = J_3 = J_{2b} \]  
\[ dV_{ref} = V_{g3} - V_{g3} = V_T \cdot \ln(N) \]  
\[ I_{ax} = \frac{dV_{g3}}{R_3} = \frac{V_T \cdot \ln(N)}{R_3} \]  
\[ I_{bx} = \frac{dV_{g3}}{R_3} \]  
\[ J_2 = \frac{R_{2a}}{R_2} \cdot \frac{dV_{g3}}{R_3} \]  
\[ I_{ref} = R_4 \left( \frac{V_{g3}}{R_2} + \frac{dV_{g3}}{R_3} \right) = V_{ref-prop} \]  
\[ V_{ref-prop} = \frac{R_4}{R_3} V_{ref-raw} \]  

Output voltage \( V_{ref-raw} \) is available to change \( V_{ref-prop} \) of resistor ratio of \( R_2 \) and \( R_4 \).

3 Proposed low voltage BGR circuit

Proposed bandgap reference circuit is shown in Figure 3. That is consisted of OP-Amp that is operated in 1V power supply voltage, PNP BJT, PMOS and two resistors.

Flowing current in I1, I2 and I3 is same in the proposed bandgap circuit of Figure 3. If PNP BJT and resistor ratio is 1:N, flowing current of Q1 and Q2 is expressed as
\[ I_1 = I_2 = I_3 \]  
\[ J_1 = J_2 = J_3 = J_{2b} \]  
\[ dV_{g3} = V_{g3} - V_{g3} = V_T \cdot \ln(N) \]  
\[ I_{ax} = \frac{dV_{g3}}{R_3} = \frac{V_T \cdot \ln(N)}{R_3} \]  
\[ I_{bx} = \frac{dV_{g3}}{R_3} \]  
\[ J_2 = \frac{R_{2a}}{R_2} \cdot \frac{dV_{g3}}{R_3} \]  
\[ I_{ref} = R_4 \left( \frac{V_{g3}}{R_2} + \frac{dV_{g3}}{R_3} \right) = V_{ref-prop} \]  
\[ V_{ref-prop} = \frac{R_4}{R_3} V_{ref-raw} \]  

If PNP BJT and resistor ratio is 1:1, flowing current of Q1 and Q2 is expressed as
\[ I_1 = I_2 = I_3 = \frac{V_{g3}}{R_3} \]  
\[ J_1 = J_2 = J_3 = \frac{V_{g3}}{R_3} \]  
\[ dV_{g3} = V_{g3} - V_{g3} = V_T \cdot \ln(N) \]  
\[ V_{ref-raw} = R_4 \left( \frac{V_{g3}}{R_2} + \frac{dV_{g3}}{R_3} \right) + V_{ref}\]  

In case size of BJT is same, N is 1. In the end, \( V_{ref} \) is can be written as
\[ V_{ref} = V_T \cdot \ln(N) + \frac{2 V_{g3} \cdot \ln(N) \cdot J_2}{R_1 \cdot \ln(\text{Cox}) \cdot W \cdot L} + V_{in} \]  

PTAT voltage is generated by \( R_1 \) and \( V_T \). And CTAT voltage is generated by \( V_{in} \) and \( W/L \). So, robust \( V_{ref} \) voltage against PVT is generated in the BGR. Using ratio of current in place of using size ratio of Q1 and Q2, size is reduced and performance is same with conventional BGR circuit. That is, if current ratio of 1:K is used in place of BJT size ratio of 1:N, size is can be reduced and performance is equal.
4 Simulation result

Fig. 4 BGR simulation result

Fig. 5 characteristic of temperature simulation result

The performances of the proposed bandgap reference are verified through Spectre simulation of Cadence. The simulation uses standard 0.18μm CMOS process. The bandgap can be operated with a supply voltage as low as 1V and provides an output voltage of 690mV over a temperature range from 0°C to 80°C as shown in Figure 4. Figure 5 shows the reference voltage variation is only 2.5mV in that temperature range. Table 1 is shown temperature variation of $V_{\text{ref}}$ in operation voltage 1V.

<table>
<thead>
<tr>
<th>Temperature</th>
<th>$V_{\text{ref}}$</th>
<th>$V_{\text{ref}}$</th>
<th>$V_{\text{ref}}$</th>
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<tbody>
<tr>
<td>0°C</td>
<td>0.69040mV</td>
<td>0.69025mV</td>
<td>0.69191mV</td>
</tr>
<tr>
<td>25°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80°C</td>
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Table 1 BGR temperature simulation result

The figure 6 shown in conventional low voltage bandgap layout and figure 7 is proposed bandgap layout. As a result, If using the PNP BJT ratio 1:N instead of ratio 1:1 and flowing current ratio 1:N, the layout area reduced about twice and drawing easily.

5 Test result

Fig. 6 Conventional architecture BGR layout

Fig. 7 Proposed architecture BGR layout

Fig. 8 Chip test result

Chip test result is shown in Figure 8. Test result shows that the proposed circuit is capable to work with supply voltage down to 1V and The $V_{\text{ref}}$ voltage shows stable voltage of 0.5V. $V_{\text{DS}}$ variation in pmos on account of resistance error is influenced the change of $V_{\text{ref}}$. In addition, We can be expected to change $V_{\text{ref}}$ for the change $I_3$ current.

6 Conclusion

Despite the change of PVT, BGR is providing the critical circuit blocks for a stable voltage. So BGR circuit is very important circuit in the most analog circuit. The proposed
CMOS voltage reference circuit consists of a traditional bandgap circuit based on the use of PMOS transistors and current ratio 1:N. This paper proposes the new BGR circuit using PMOS and BGR ratio 1:1 which decreases reference variation. The new BGR circuit is also decreases the chip size. And New BGR is providing a stable $V_{ref}$ voltage in 1V. Conventional architecture $V_{ref}$ and proposed architecture $V_{ref}$ is same. Therefore the circuit is widely used to provide stable voltage references in flash memory, DRAM and many types of analog circuits.

References: