A 3.4Gbps Transmitter for Multi-Serial Data Communication using Pre-emphasis Method

KANGJIK KIM[1], KISANG JUNG[1], CHIMIN PARK[1],
WONKI PARK[2], SUNGCHUL LEE[2], SEONGIK CHO[1]

[1]The Department of Electronics Engineering
Chonbuk National University
664-14 1GA DUCKJIN-DONG JEONJU JEONBUK
SOUTH KOREA
[2]Korea Electronics Technology Institute

kkangjik@chonbuk.ac.kr, kisang@chonbuk.ac.kr, chimin@chonbuk.ac.kr
wkpark74@keti.re.kr, leesc@keti.re.kr, sicho@chonbuk.ac.kr

Abstract: - This paper is intended as design of a 3.4Gb/s transmitter (TX) for multi-channel communication. It can be applied high-speed serial link system such as DVI, HDMI etc. This TX circuit can be classified into three main blocks and one additional block: a PLL (Phase Locked Loop) block for a clock distribution, a MUX (multiplexer) block as a data serializer and an output buffer stage for a driving of output data stream. The additional block is a PRBS circuit for a separated PHY verification. The output buffer consists of three parts (pre-driver, CML main driver and pre-emphasis driver). Especially, the pre-emphasis method is applied to improve the effect of ISI. The fabricated TX was designed using 0.18μm 1P5M CMOS technology and was verified on 3.4Gbps output data rate by measurement results. An eye-opening is shown about 0.8UI/700mV on output data. The fabricated chip has been designed and laid using 0.18μm 1P5M CMOS technology.

Key-Words: - Transmitter (TX), PHY (Physical Layer), Phase Locked-Loop (PLL), Multiplexer (MUX), CML driver, Pre-emphasis

1 Introduction

Recently, high-speed serial data link system such as DDI (Digital Display Interface) is demanding higher accuracy and huge transmission capacity due to the growth of data transmission [1]. The display devices are required higher resolution and deeper color depth gradually. In other words, the reliable bandwidth is needed in the interface PHY.

The most challenging issue in telecommunication is an overcoming limitation of data transition speed without a data distortion. The distortion is due to ISI (Inter-Symbol Interference) mainly. The distortion of ISI is caused by a signal in which one symbol interferes with subsequent symbols. That is to mean it appears in the previous symbols as critical noise and its attenuation reduces signal quality. Consequently, it introduces data error in the receiver stage. The cause of ISI is commonly the serializing MUX stage or a band limited channels [2][3] .

In this TX PHY, the output buffer stage applies pre-emphasis as an equalizer to minimize the effects of ISI. It could achieve delivering the higher data rate to the receiver via channels with the smallest error rate. This paper presents a design for a high-speed TX with pre-emphasis. The TX has application in HDMI TX PHY [4]. The first part of this paper investigates the overall architecture and describes detailed blocks. After ascertaining the major blocks, the next section focuses on the verification by experimental results. Finally, the conclusion is given in the last section.

2 Overall Architecture

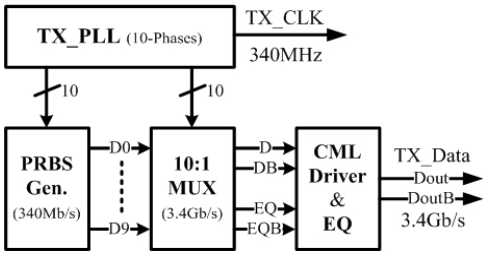

Fig. 1. Block diagram of the TX PHY

The total TX circuit consists of four parts, as shown above fig.1: the10-phase PLL which distributes to the TX stage (10:1 MUX, PRBS Gen.) and a receiver stage for a reference clock, the 10:1 MUX stage as a data serializer and a controller of pre-emphasis, the output driver stage with the pre-emphasis as an equalizer and the PRBS generator which can make a random NRZ (Non-Return to Zero) data pattern. The description of detailed block will be examined further in the next subsection respectively.

2.1 10-Phases PLL

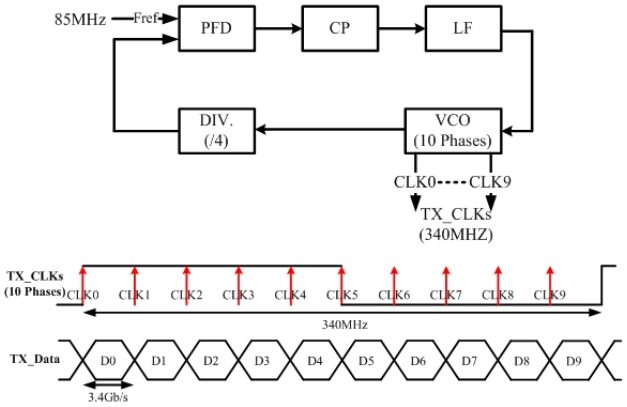

Fig. 2. Block diagram of the 10-phases PLL

A Block diagram of the PLL as a clock generator of TX stage is shown in Fig. 2. This PLL is required an 85MHz input reference frequency and a 1/4 divider for a verification of 3.4Gb/s maximum data rate. It has a ring type VCO (Voltage Controlled Oscillator) which consists of five differential delay stages for generating 10-clocks (CLK0~9) and fan-out buffer stages considered driving multi-path.

2.2 PRBS Generator and Serializer

Fig. 3 shows the block diagram of the PRBS (Pseudo Random Binary Sequence) generator and Serializer using a 10:1 MUX stage. The PRBS generator is separated of two parts: The PRBS stage makes a 340Mb/s random NRZ data steam and a D-FF stage makes 10 data steam copies as a forged parallel host data. Each 10 parallel data (340Mb/s) through the 1:10 multiplexer is serialized into one differential data (3.4Gb/s). In the Mux stage, a binary tree type that is multiplexing techniques for high-speed operation method is used [5]. However, it causes some deterministic jitter by ISI as a series of high (low) signal followed by a bit length of the low (high) signal will appear to occur. To reduce the cause of jitter as serializing applies the pre-emphasis which is controlled by logical conditions of the MUX stage. The operation of serializing and signaling is shown below Fig. 4.

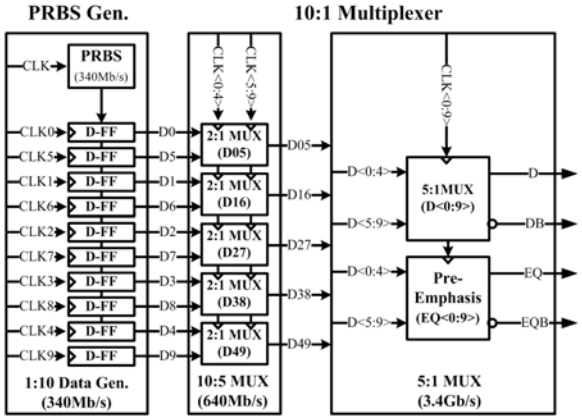

Fig. 3. Block diagram of the PRBS Gen. and Serializer (10:1 MUX)

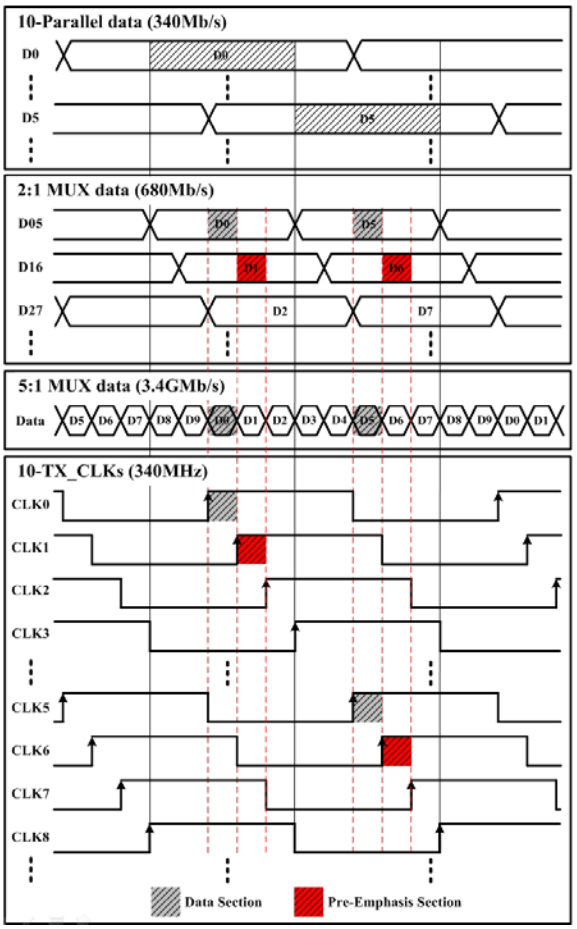

Fig. 4. Operating condition of 10:1 MUX and Pre-emphasis control.

2.3 Output Buffer

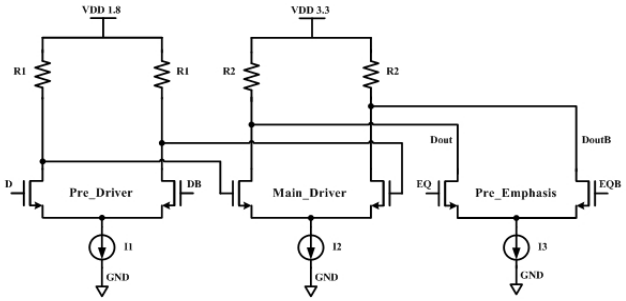

Fig. 5. Schematic of Output Buffer stage

For transmitting of TX output data, CML type buffer is implenmented as a driver. In additional pre-emphasis driver is added in main-driver output stage [6]. Each pre-driver and main-driver supply voltage are 1.8V/ 3.3V and current are about 8mA, 21mA . Giving the amplitude weighting for the driver pre-emphasis of the current one is about 3mA. Fig 5 shows a schematic of each stage CML driver. Chip pad, wires and PCB lines modeling were applied in the simulation verification. Fig. 6 shows the configured schematic to simulate for the jitter characteristics of the final TX data.

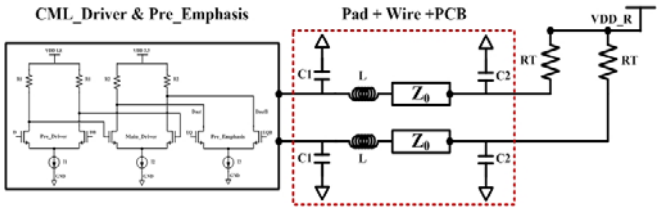

Fig. 6. The modeling of output-stage for the simulation verification

3 Measurement Results

The TX was fabricated and laid using 0.18μm 1P5M CMOS technology and the measurement was performed on COB (Chip-On-Board) condition. The characteristic of measurements is shown below figures in this section. The multi-phase clocks of PLL output appear in Fig. 7. CLK0~CLK3 were shown and the others were omitted. It shows that each clock has a 36 ° of phase difference. Fig. 8 shows clock jitter of PLL and Fig.9 shows eye-diagram of the out data at 3.4Gb/s. Each of the pk-to-pk jitter is about 33ps and 50ps. the layout darwing is shown in Fig. 10. Eventually, table 1. Summarizes the results of the measurements on the fabricated TX chip.

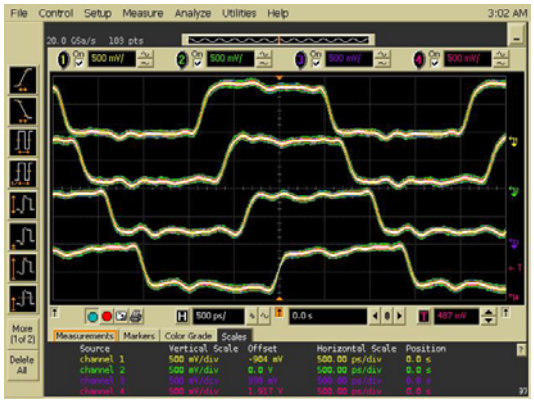

Fig. 7. Multi-phase clocks of PLL

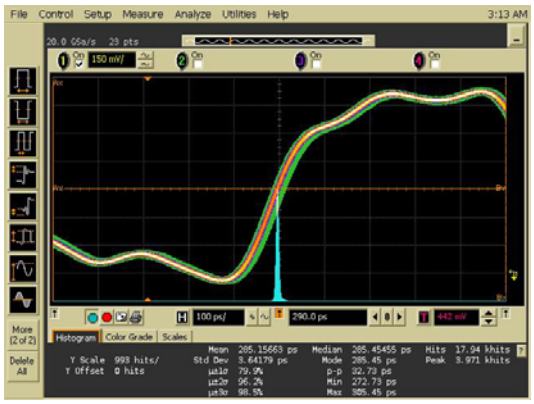

Fig. 8. Clock jitter of PLL

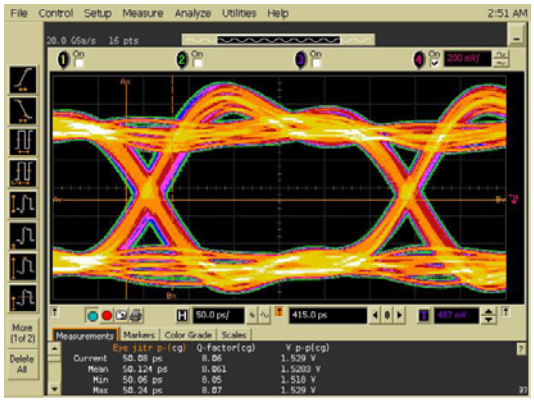

Fig. 9 Eye-diagram of the output data at 3.4Gb/s

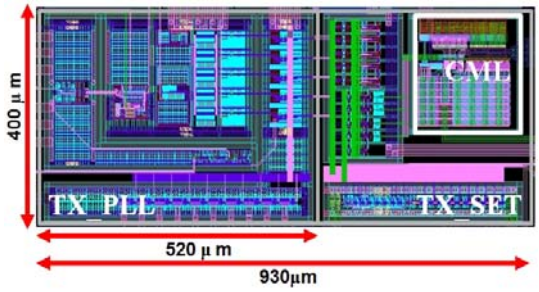

Fig. 10. Layout

Table. 1. Summary of results

Process		0.18μm CMOS
Data rate (Max.)		3.4Gb/s
Clock jitter (pk-to-pk)		33ps
Eye-diagram Features	Data jitter (pk-to-pk)	50ps
	Data jitter (RMS)	8.3ps
	Eye width	245ps (0.83UI)
	Eye height	700mV
Power Dissipation	1.8V Supply	120mW
	3.3V Supply	174mW
Chip Size		0.372mm^2

4 Conclusions and Future works

In this paper, the 3.4Gb/s TX for the serial data communication was designed and the pre-emphsis method in the output buffer stage was adapted to improve the driving performance. The final results of measurments is summarized as shown above table 1. To sum up the main target of this paper was the TX PHY for the HDMI and the fabricated chip was satisfied with its specification on maximum data rate. However, It calls for further research as the TX PHY should cover under version data rate (Minimum: 250Mb/s) and reduce the jitter performance.

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