A 3rd 3bit Sigma-Delta Modulator with Data Weighted Averaging for Reducing Delay Time

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Abstract: - This paper presents a 3rd order sigma-delta modulator with minimize a feedback delay time of DWA(Data Weighted Averaging). The 3rd order sigma-delta modulator go through Matlab modeling for defining stable coeffietients of the integrator and limiting of non-ideality characteristics. The used fully differential switched capacitor integrator, comparator and DWA are designed transistor level by considering non-idealities. The modulator with proposed DWA structure improve timing margin about 23%. The designed sigma delta modulator with proposed DWA performs maximum SNR(Signal to Noise Ratio) of 79 dB, DR(Dynamic Range) of 78 dB and power consumption of 120mW in sampling frequency of 82.8 MHz

Key-Words: - Sigma-Delta Modulator, Multibit Sigma-Delta, DWA, Data Weighted Averaging

1 Introduction

The sigma-delta modulator is one of architecture that is being examined for use in low power, high resolution, moderate speed application. Conventionally, sigma-delta modulator is used for low frequency application requiring high resolution, such as digital audio or high precision instrumentation.[1]. Recently, due to rapid development of VLSI process, it has been applied wideband communication system. In order to achieve high resolution while keeping a low oversampling ratio and thus a lower sampling clock rate, higher order sigma-delta modulators can be used. Due to the potential stability problem of higher order(>2) multiloop sigma-delta modulator with a single-bit quantizer, different alternatives have been investigated[7]. A sigma-delta modulator should be over several MHz of signal band and get high resolution at lower oversampling ratio. Increasing the quantizer resolution in a sigma-delta modulator can increase SNR, improve stability and reduce integrator power consumption. However, each added bit of quantizer resolution also causes an exponential increase in the power dissipation, required area and complexity of the DEM(Dynamic Element Matching) circuit required to attenuate digital to analog converter mismatch errors[2-4]. CLA(Clock Level Averaging), ILA(Individual Level Averaging) and DWA(Data Weighted Averaging) algorithms are included DEM technique. The DWA is a technique to remove DAC cells mismatch errors out of the band of interest.

In essence, DWA tries to choose different DAC cells for consecutive codes. In this way, less common units participate in consecutive codes and DAC error signal shows fast changes in time domain which is an indication of high-frequency content in frequency domain[5-8]. This paper proposed the new block and timing diagram of the DWA for high speed sigma-delta modulator. Through the MATLAB modeling, the modulator analyzes stability and performance. The designed sigma delta modulator implements 79 dB SNR and 12bit resolution.

2 Design Consideration

2.1 Modeling

The sigma-delta modulator consists of 3rd order multibit as shown in Fig. 1. 2nd order sigma-delta modulator is stable itself, however over 3rd order sigma-delta modulator needs stability check. To get the maximum SNR and stability, the coefficients, B2 and B3, change in the modeling. The SNR of this 3rd order multibit sigma-delta modulator has 87dB at B2=0.8 and B3=2 as shown in Fig. 2. Then the 9-level quantizer gain coefficient ‘g’ has to larger than 0.45 for stable operation as in Fig. 3.
Secondly, some non-ideality limit is set for approaching ideal characteristic in Matlab modeling as Table 1.

Fig. 1. Diagram of the 3rd order multibit sigma-delta modulator

Fig. 2. The SNR characteristic of the modulator according to the integrator gain coefficient (B1=0.33)

Fig. 3. Root locus of third-order sigma-delta modulator with integrator coefficients (0.33, 0.8, 2)

Table 1. Design specifications of modulator

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Permitted Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output swing [V]</td>
<td>±1</td>
</tr>
<tr>
<td>Amplifier gain [dB]</td>
<td>&gt;62</td>
</tr>
<tr>
<td>Slew rate of amplifier [V/μs]</td>
<td>&gt;160</td>
</tr>
<tr>
<td>Hysteresis of comparator [mV]</td>
<td>&lt;12</td>
</tr>
<tr>
<td>Capacitor ratio error [%]</td>
<td>&lt;5</td>
</tr>
</tbody>
</table>

2.2 SC integrator and DAC

The circuit of the SC (Switched Capacitor) integrator is shown in Fig. 4 with feedback DAC (Digital to Analog Converter). Ph1, ph1d, ph2, and ph2d are non-overlapping clock. Designed SC integrator use fully differential structure for improving the SNR and transmission gate switch for decreasing the nonlinearity.

The first OTA of integrator affect the sigma-delta modulator more important than 2nd and 3rd OTA. The first OTA use gain boosting technique and has rail to rail input range. The OTA designs fully differential for decreasing noise floor. The 2nd and 3rd OTA of integrator eliminate the gain boosting circuit because of unnecessary high gain.

Table 2. Performance of OTA

<table>
<thead>
<tr>
<th></th>
<th>Amp1</th>
<th>Amp2,3</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC-gain [dB]</td>
<td>88</td>
<td>65</td>
</tr>
<tr>
<td>GB [MHz] (CL=6p)</td>
<td>385</td>
<td>162</td>
</tr>
<tr>
<td>Phase Margin [Degree]</td>
<td>68°</td>
<td>62°</td>
</tr>
<tr>
<td>Output swing [V]</td>
<td>±0.85</td>
<td>±1</td>
</tr>
<tr>
<td>Slew rate [V/μs]</td>
<td>210</td>
<td>180</td>
</tr>
</tbody>
</table>

2.3 DWA

Due to the error of DAC unit capacitor, non ideality of sigma delta modulator increase noise floor. The DEM method eliminates this noise floor and rearranges the unit capacitor. If the thermometer code selects the same unit
capacitor, the SNR of sigma delta modulator is decreased. So, preventing the selection of the same capacitance and decreasing the average error, the sigma delta modulator with DWA algorithms randomize the unit capacitor. However, if the clock frequency of sigma delta modulator increases, the feedback delay time of thermometer code must quicken. If the sigma delta modulator operate clock frequency of 52.8 MHz with 1.1 MHz signal band and OSR of 24 times, the quantizer and DWA must operate ph1 time of 8 ns. Therefore, this paper proposed the DWA for optimizing the feedback delay time. Fig. 5 is the proposed DWA with new block diagram and timing diagram. Operation principle by timing visual point of Fig. 5 (b) is as following:

1. When the ph2d change '1' into '0', the 9-level quantizer samples the output of integrator.
2. The output of integrator is changed to 8 codes through comparator.
3. Thermometer code that is made by ph1d is passed to shifter1, shifter2, shifter3 by C0, C1, and C2 control signal.
4. Thermometer code that passes shifter saves 8bit buffer by signal.
5. Do not influence at all delay time, shifter's control signal that generates 3bit memory is encoded by signal. This output is expressed by unit of measure with present signal T[n] and shifter control signal.

Conventional DWA needs more timing margin because of latching the output of quantizer in ph1. But, the proposed DWA latch the quantizer output in falling time of ph1 and the control signal of shifter keep up the time of ph1. The sigma delta modulator with the proposed DWA improves stable operation and timing margin as shown in equation (2) and Fig. 6. TQ is the delay time of quantizer and DS is the delay time of shifter. The proposed DWA minimizes the feedback delay time.

\[
\frac{T_Q + T_S \times 3 + T_C}{T_{total}} = \frac{0.7 \text{ns} + 1.5 \text{ns} + 0.3 \text{ns}}{8 \text{ns}} \approx 31.25\% \quad (1)
\]

\[
\frac{T_Q - T_S}{T_{total}} = \frac{0.7 \text{ns} - 0.5 \text{ns}}{8 \text{ns}} \approx 15\% \quad (2)
\]

Fig. 5. Proposed DWA structure (a) block Diagram (b) timing diagram

Fig. 6. Output delay time of proposed DWA

Fig. 7. Output of the scramble thermometer code
3 Simulation

Fig. 7 show in 3 bit output of proposed DWA algorithms, after simulation. Therometer code operates normally being circulated. The input signal has the magnitude of 1.2 Vp-p, the input frequency of 825 KHz, and sampling frequency of 52.8 MHz. The conventional DWA structure dominate 31.25% of 8ns which is the total delay time, but proposed DWA structure dominate 15% of total delay time. So, the proposed DWA structure increases the sampling frequency to 227 MHz. The measured spectrum of sigma-delta modulator with proposed DWA is shown in Fig. 8. With 52.8MHz sampling frequency, the SNR of the sigma-delta modulator measured 75dB. Noise floor affect the SNR that has the 10dB of the difference between behavior simulation and measured data. Table 2 shows the performance of the proposed 3rd order multibit sigma delta modulator.

![Simulated output spectrum](image)

Table 3. Performance summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.35μm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal band</td>
<td>1.1 MHz</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>52.8MHz</td>
</tr>
<tr>
<td>Peak SNR</td>
<td>75 dB</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>74 dB</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>±1.65V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>120mW</td>
</tr>
</tbody>
</table>

4 Conclusion

This paper indicates design of 3rd sigma-delta modulator with Minimizing delay time of DWA. Designed sigma-delta modulator goes through the non-ideality optimizing procedures and coefficient stable procedures from Matlab modeling. And proposed DWA reduced 16.25% of total delay time. It means designed multi-bit sigma-delta modulator is able to improve over sampling rate. At last The designed sigma delta modulator performs maximum SNR of 79 dB, DR of 78 and power consumption of 120mW in sampling frequency of 82.8 MHz.

References: