A Large-Signal Analysis for a Ring Oscillator with Negative Skewed Delay

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Abstract - This paper presents a large signal analysis of ring-type oscillators with negative skewed delay scheme. The analysis yields the frequency increase factor due to negative skewed delay scheme. The large signal analysis is needed, because small signal model is limited to the initial stage of oscillation. For verification of the frequency increase factor, simulation and chip fabrication were done under the same conditions for the two different types of ring oscillators, i.e., with and without negative skewed delay scheme. Measurement results are in good agreement with predictions based on analysis and simulation.

Key-Words: - Ring Oscillator, Negative Skewed Delay, Voltage Controlled Oscillator, VCO.

1 Introduction

Phase locked loops (PLLs) have been widely used for many applications including wireless communication systems. A voltage controlled oscillator (VCO) is one of the key elements in PLLs and very critically determines the performance of the PLLs.

LC VCOs have been used for high-performance PLLs because of their reasonably good phase noise characteristics [1]-[2]. But implementing high-quality inductors in a standard CMOS process is rather difficult due to the parasitics. Moreover, the LC VCO usually has a narrow tuning range. On the other hand, a ring VCO can be easily integrated in a standard CMOS process. In addition, a wide oscillation frequency range can be obtained [3].

However, the highest possible oscillation frequency is lower for a ring VCO than for an LC VCO. Therefore a negative skewed delay (NSD) scheme was proposed to improve the operating speed of ring-type VCO [3]-[5].

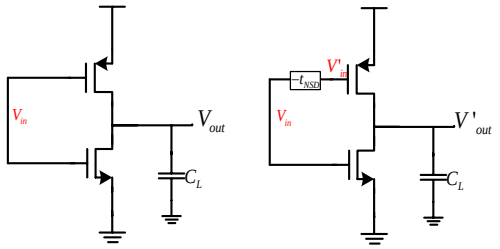
The negative skewed delay scheme has been analyzed using a small signal analysis [5]. But the small signal analysis is applicable only to the initial stage of the oscillation. So, a large signal analysis is needed for accurate analysis of the steady state behavior of the oscillator [6].

This paper presents a large signal analysis for a ring oscillator with a negative skewed delay. The frequency increase factor is obtained based on the analysis.

The predicted frequency increase factor is verified through simulations and measurements done for both the conventional ring oscillator and the ring oscillator with the negative skewed delay. Simulations and measurements show a reasonably good agreement in the frequency increase factor as predicted by large signal analysis. The chip was fabricated in a standard 0.18μm CMOS process.

2 Negative Skewed Delay Scheme

Fig. 1 illustrates the concept of a negative skewed delay. Both p-MOSFET and n-MOSFET have the same input signal in the conventional delay circuit (Fig. 1(a)), but in the NSD scheme, the input of the p-MOSFET is connected to a negative delay element so that the input signal to the p-MOSFET arrives earlier than that to the n-MOSFET (Fig. 1(b)). This is the definition of a negative skewed delay scheme [4].



(*a*) (*b*)

Fig. 1. (a)conventional delay cell (b)NSD cell

Fig. 2 shows the output waveforms of the two schemes when the square wave is input to each cell. Input signals can be divided into four regions for the sake of explanation.

In Region ①, the p-MOSFET is on and the n-MOSFET is off. At $t=t_1$, the rising transition of the input signal occurs at the gate of the p-MOSFET. This transition if advanced in time by the magnitude of the negative skewed delay, t_{NSD} with respect to the n-MOSFET input. In Region ②, the output is floating and holds the previous output voltage, because both transistors are off.

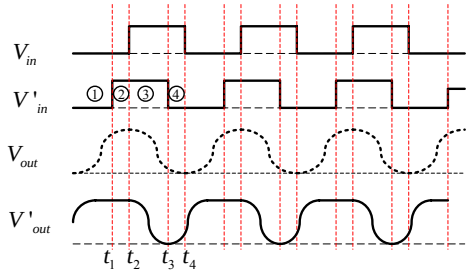


Fig. 2. Output waveforms for the conventional and the NSD cell as defined in Fig. 1.

At $t=t_2$, the n-MOSFET is turned on and the output is pulled down to the ground. There is little difference in delay time (t_{PHL}) between the conventional delay scheme and the NSD scheme. At $t = t_3$, the p-MOSFET is turned on, the output node voltage is pre-charged to some prescribed voltage. After $t=t_4$, the output voltage continues to increase up to V_{DD}.

Fig. 3 shows the waveforms of the output voltage for both the conventional and the NSD scheme in Regions ④ and ①. The NSD scheme allows the output to start charging earlier and thus reduces the low-to-high propagation delay. As a result, the oscillation frequency is increased. The final pre-charged output voltage in Region ④ is determined by t_{NSD} and sizes of the MOSFETs.

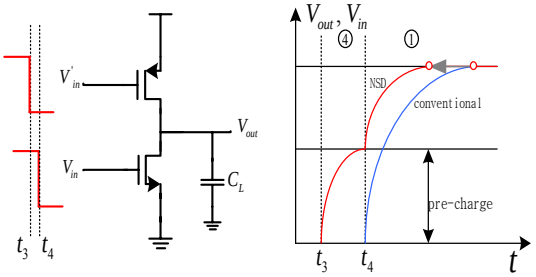


Fig. 3. Output waveforms for Regions ④ and ① in Fig.2

3 Large Signal Analysis

In Fig. 4, the waveform of the output voltage is shown for Regions ② and ③. The high-to-low transition occurs in Region ③. Initially the n-MOSFET is in saturation. When the output voltage falls below $V_{DD}-V_{th}$, the n-MOSFET will enter into the triode region. The effect of a NSD is typically negligible, because the output voltage reaches V_{DD} before being discharged. The high-to-low propagation delay (t_{PHL}) can be found [7], [8] as

$$t_{PHL}=\frac{C_L}{k_n(V_{DD}-V_t)}\left[\frac{2V_t}{V_{DD}-V_t}+\ln\left(\frac{4(V_{DD}-V_t)}{V_{DD}}-1\right)\right] \quad (1)$$

where

$$k_n=\mu_n C_{ox}\left(\frac{W}{L}\right)_n, \quad k_p=\mu_p C_{ox}\left(\frac{W}{L}\right)_p$$

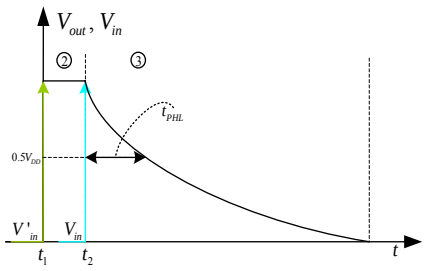


Fig. 4. Output waveform for rising input

Now let us consider the low-to-high transition in Regions ④ and ① as shown in Fig. 5. As discussed in Section 2**,** pre-charging occurs in Region ④. But there is a restriction on the pre-charging. The pre-charged output voltage cannot exceed the threshold voltage of the n-MOSFET, since it will turn on the n-MOSFET of the next stage inverter and thus disrupt the operation of the ring oscillator. The analysis of the low-to-high transition for NSD scheme is different from that for the conventional scheme, because n-MOSFET is on. In Region ④, n-MOSFET remains in the triode region and p-MOSET remain in the saturation. So the output voltage can be expressed as in (2).

$$V_{out}(t_4)=(V_{GS}-V_t)+\frac{\frac{1}{R_{np}}\times\left(1+e^{\left(\frac{1}{R_{np}C_L}\right)t}\right)}{k_n\left(1-e^{\left(\frac{1}{R_{np}C_L}\right)t}\right)} \le V_t \quad (2)$$

where

$$\frac{1}{R_{np}}=\sqrt{k_n(k_n-k_p)}(V_{GS}-V_t), \quad k_n=\mu_n C_{ox}\left(\frac{W}{L}\right)_n$$

The low-to-high propagation delay (t_{PLH}) for NSD scheme is different from that for the conventional scheme, because the NSD scheme allows pre-charging. The output voltage in Region ① can be written as in (3). The resulting low-to-high propagation delay can be expressed as (4).

$$V_{out}(t) = \frac{2(V_{DD} - V_t)}{1 + e^{\frac{t - t_{NSD}}{R_p C_L}}} \quad (\text{for } V_t \le V_{out} \le V_{DD}) \tag{3}$$

where

$$\frac{1}{R_p} = \mu_p C_{ox} \left(\frac{W}{L}\right)_p (V_{DD} - V_t)$$

Then

$$t_{PLH} = \frac{C_L}{k_p (V_{DD} - V_t)} \ln\left(\frac{4(V_{DD} - V_t)}{V_{DD}} - 1\right) \tag{4}$$

The oscillation frequency of the conventional ring oscillators without the NSD scheme can be expressed as in (5). With the NSD scheme, the oscillation frequency is increased as can be seen in (6).

$$f_{osc.conv} = \frac{1}{NC_L\left(R_n \cdot \left(\frac{2V_{th}}{V_{DD}} + \ln\left|3 - \frac{4V_{th}}{V_{DD}}\right|\right) + R_p \cdot \left(\frac{2V_{th}}{V_{DD}} + \ln\left|3 - \frac{4V_{th}}{V_{DD}}\right|\right)\right)} \tag{5}$$

$$f_{osc.NSD} = \frac{1}{NC_L\left(R_n \cdot \left(\frac{2V_{th}}{V_{DD}} + \ln\left|3 - \frac{4V_{th}}{V_{DD}}\right|\right) + R_p \cdot \left(\ln\left|3 - \frac{4V_{th}}{V_{DD}}\right|\right)\right)} \tag{6}$$

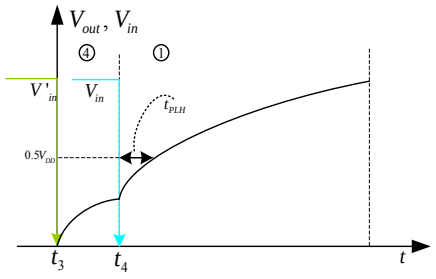


Fig. 5. Output waveform for Regions ④ and ①.

4 Conclusion

The ring oscillator using a negative skewed delay and the conventional ring oscillator have been designed and simulated in a standard 0.18μm CMOS process. The number of stages was varied from 5 to 15. The minimum number of stage is 5, because the NSD scheme yields a diode-connected PMOS load when the number of stage is 3. The oscillation frequency of each type of oscillator is plotted a function of the number of stages in Fig. 6

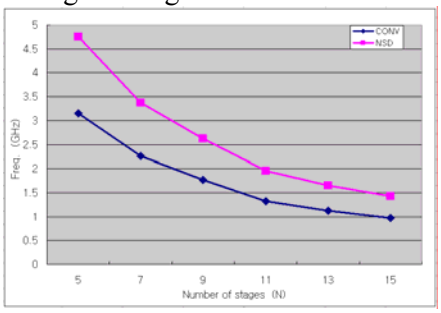


Fig. 6. The simulated oscillation frequency vs. the number of stages.

The simulated frequency increase factor for the NSD scheme is shown in Fig. 7.

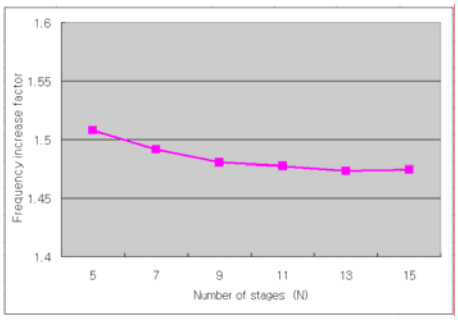


Fig. 7. The simulated frequency increase factor vs. the number of stages.

5 Measurement

The fabricated chip includes four ring oscillators: two conventional oscillators (5-stage and 11-stage) and two NSD scheme oscillators (5-stage and 11-stage). Comparisons among theoretical (based on large signal analysis) predictions, simulations, and measurements are shown in Fig. 8

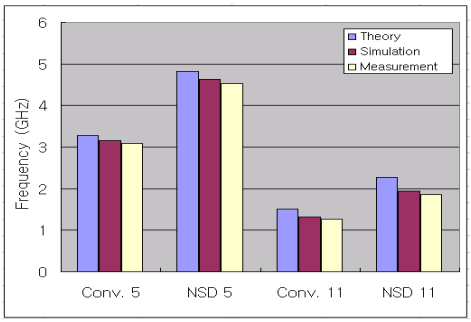


Fig. 8. Comparison among theory, simulation, and measurement.

Fig. 9 shows the variation of the oscillation frequency as a function of the control voltage for two types of 11-stage ring VCO.

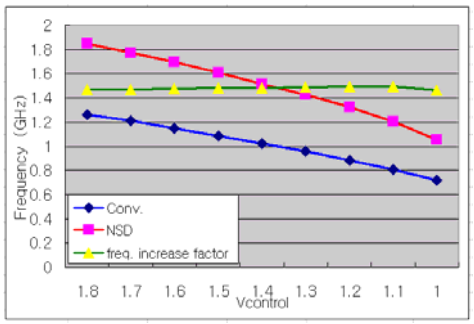


Fig. 9. Tuning characteristics of the ring VCO including the frequency increase factor.

6 Conclusion

The frequency increase factor of the oscillation frequency predicted by the large signal analysis is approximately 1.54. Simulation showed a frequency increase factor of about 1.485. The measurement of the fabricated chip yielded approximately 1.466, which is in reasonably good agreement with both the analysis and simulation.

Acknowledgment

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