CMOS Current-Mode Selectable S-Shape Correction Circuit

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Abstract: - This paper presents a CMOS current-mode S-shape correction circuit. The S-shape correction function is proposed to suit for panel-to-panel LCD displays by selecting a fractional value. Simulated results are at 1.8V supply voltage for 0.35μm CMOS process. Image quality improvement due to S-shape correction is observed. The -3dB bandwidth are about 50 MHz for the proposed circuit.

Key-Words: - LCD, S-shape curve, gamma correction, current-mode circuit, Taylor series

1 Introduction
Nowadays the color-correct visualizations of the LCD displays become more and more important. The electro-optical transfer function of an LCD display is called S-shape curve. Many digital circuits [1-3] were developed to correct the S-shape curve. In [4], an analog compensating circuit designed with BJTs was proposed to be suited in the portable equipments with TFT-LCD. In [5], a new model was developed for the S-shaped electro-optical transfer function of the LCD device. However, due to different LCD panels spectral and gamma characteristics at different monitor manufacturers, one should make different corrections.

In the past decade, analog current-mode circuits have received considerable attention due to their wider bandwidth, large dynamic range, simple circuitry, and lesser power dissipation. In many cases, digital solutions are too slow and complex, thus indicating the need for analog realizations. A current-mode square-root circuit, the simplest current-mode fractional-power circuit, is used in current-mode analog circuits such as fuzzy linguistic-hedge circuits, adaptive filters, and geometric mean circuits [6-8]. In [9], a square-root circuit and a cube-root circuit designed with BJT are applied in a current-mode gamma corrector. However, a CMOS current-mode fractional-power circuit with fractional-value being not 1/2 is hard to realize. In this paper, we develop a CMOS current-mode fractional-power circuit and a multiplier to realize an S-shape correction circuit.

The fractional-power circuit is built by a compressing circuit and an expanding circuit. The compressing circuit made by a CMOS current-mode logarithm circuit is used to form a log-domain. The logarithm function is approximated by a second-order Taylor series due to the square-law transfer characteristics of a MOS transistor. In the log-domain, current-mirror pairs are used to generate different ratios, which play a selectable S-shape role. The expanding circuit made by a CMOS current-mode exponential circuit is used to expand the log-domain. The exponential function is also approximated by a second-order Taylor series.

2 S-Shape Correction model

A CRT display and an LCD display have electro-optical transfer functions shown in Fig. 1, where the transfer function of an LCD is an S-shaped curve. As same as the gamma correction, we model a
novel correction curve called S-shape correction curve shown in Fig. 1(b) with
\[ y = s(x - 1.5)^2 + c \quad (1) \]
where \( s \) is used to scale the output brightness, \( n \) is a fractional value representing different S-shape curve, and \( c \) is a constant for level shift. Figure 2 plots (1) with different \( s \), \( n \), and \( c \) for \( x \) from 0 to 3. The variations of \( s \) and \( n \) show the characteristics of panel-to-panel LCD displays.

Fig. 2 S-shape correction curves with different \( s \), \( n \), and \( c \) for (1).

3 Correction Block Diagram

![Block diagram of the proposed circuit.](image)

To realize (1), we need design a scale circuit, a multiplier, a square circuit, and a fractional-power circuit. Figure 3 shows the block diagram of our proposed circuit. Obviously, block 2, 3, and 4 form the fractional-power function, which can be expressed as
\[ x^n = \exp(\ln(x^n)) \quad (2) \]
where \( \exp(\cdot) \) and \( \ln(\cdot) \) are the exponential function and the logarithm function, respectively. Equation (2) is a companding (compressing-and-expanding) operation. Block 2 and block 4 are the compressing block and the expanding block, respectively. Due to the logarithm characteristics, the multiplication of \( n \) and \( \ln(x) \) will equal to \( \ln(x^n) \). Therefore, from (2) we could express the fractional-power function as
\[ x^n = \exp(n \cdot \ln(x)) \quad (3) \]

It is difficult to realize an exponential function and a logarithm function due to the square-law transfer characteristic for MOS transistors operating in the saturation region for high speed applications. Considering the complexity and accuracy of circuitry, we could approximate the corresponding natural logarithm function and exponential function with second order polynomials. A second-order Taylor expanding should be used to approximate a \( \ln(x) \) at \( x = a_0 \) with
\[ \ln(x) \approx \ln(a_0) + \frac{1}{a_0}(x - a_0) - \frac{1}{2a_0^2}(x - a_0)^2 \quad (4) \]
which can be rewritten as
\[ \ln(x) \approx -2(1 - \frac{x}{2a_0})^2 + \ln(a_0) + 0.5 \quad (5) \]
In a similar way, a second-order Taylor expanding for evaluating \( \exp(y) \) at \( b_0 \) will be
\[ \exp(y) \approx \exp(b_0) + \exp(b_0)(y - b_0) + \frac{1}{2}\exp(b_0)(y - b_0)^2 \quad (6) \]
which can be rewritten as
\[ \exp(y) \approx \frac{1}{2}\exp(b_0)((1 - b_0)^2(1 + \frac{y}{1 - b_0})^2 + 1) \quad (7) \]
From (5) and (7), we can approximate the fractional-power function by (3).

4 Circuit Implementation

4.1 Basic Circuit

![Simple basic square circuit.](image)
The basic circuit shown in Fig. 4 is constructed by the back-to-back connection of M1 and M2 [10]. Suppose that M1 and M2 are operating in the saturation region. The drain currents of M1 and M2 can be expressed by the MOS square-law:

\[ I_1 = K_p (V_{gs} - |V_{tp}|)^2 = K_p (V_{DD} - V_c - |V_{tp}|)^2 \quad (8) \]

\[ I_2 = K_n (V_{gs} - V_{in})^2 = K_n (V_c - V_{in})^2 \quad (9) \]

where \( K_p = \frac{1}{2} \mu_p C_{ox} W_1 / L_1 \) and \( K_n = \frac{1}{2} \mu_n C_{ox} W_2 / L_2 \) are the transconductance parameters of M1 and M2, respectively. Because of \( I_2 = I_1 + I_x \) and the assumption of \( K = K_p = K_n \), we will have

\[ V_c = \frac{(V_{DD} - |V_{tp}| + V_{in}) + I_x}{2K(V_{DD} - |V_{tp}| - V_{in})} \quad (10) \]

Substituting (10) into (8) and (9) gives

\[ I_1 = K(V_{DD} - |V_{tp}| - V_{in}) - \frac{I_x}{2K(V_{DD} - |V_{tp}| - V_{in})}^2 \quad (11) \]

\[ I_2 = K(V_{DD} - |V_{tp}| - V_{in}) + \frac{I_x}{2K(V_{DD} - |V_{tp}| - V_{in})}^2 \quad (12) \]

If we set \( V_0 = \frac{V_{DD} - |V_{tp}| - V_{in}}{2} \), then

\[ I_1 = KV_0^2 (1 - \frac{I_x}{4KV_0^2})^2 \quad (13) \]

\[ I_2 = KV_0^2 (1 + \frac{I_x}{4KV_0^2})^2 \quad (14) \]

\[ V_c = V_0 + V_{in} + \frac{I_x}{4KV_0} \quad (15) \]

We observe that \( I_1 \) and \( I_2 \) are the quadratic functions of \( I_x \), which means the basic circuit is a current-mode quadratic circuit. To guarantee M1 and M2 operating in saturation, the simple constrains are \( V_c > V_{in} \) and \( V_{DD} - V_c > |V_{tp}| \). Therefore, from (15) we have \( I_x > -4KV_0^2 \) and \( I_x < 4KV_0^2 \).

### 4.2 S-Shaped Correction Circuits

Figure 5 shows the logarithmic circuit and the exponential circuit. In Fig. 5(a), we assume that \( I_{out} \) has the characteristic of \( \ln(x) \), that is \( I_{out} = I_0 \ln(x) \), where \( I_0 \) is a constant current. If \( I_0 \) is mirrored from \( I_4 \) with a scale factor \( 1 \), then \( I_{out} \) will be \( I_0 + I_x \), that is

\[ I_{out} \ln(x) = -2KV_0^2 (1 - \frac{I_x}{4KV_0^2})^2 + I_b \quad (16) \]

Comparing (16) with (5), we have \( I_0 = KV_0^2 \), \( I_b = I_0(\ln(a_0) + 0.5) \), and

\[ x = \frac{a_0I_x}{2I_0} \quad (17) \]

Fig. 5 (a) logarithm circuit. (b) exponential circuit.

Similarly, in Fig. 5(b), we assume that \( I_{out} \) has the characteristic of \( \exp(y) \), that is \( I_{out} = I_u \exp(y) \), where \( I_u \) is a constant current. If \( I_9 \) is mirrored from \( I_8 \) with a scale factor \( 1 \), then \( I_{out} \) will be \( I_u + I_v \), that is

\[ I_u \exp(y) = KV_0^2 (1 + \frac{I_u}{4KV_0^2})^2 + I_v \quad (18) \]

Comparing (18) with (7), we have

\[ y = \frac{I_y}{2I_u(1-b_0)^2 \exp(b_0)} = \frac{\left| \frac{b_0}{b_0} \right| I_x}{4KV_0^2} \quad (19) \]

Fig. 6 Multiplier.

Figure 6 shows the multiplier which is modified from [11]. In the multiplier,

\[ I_{12} = K^* V_0^2 (1 - \frac{I_{in2}}{4KV_0^2})^2 \quad (20) \]

\[ I_{15} = K^* V_0^2 (1 + \frac{I_{in1}}{4KV_0^2})^2 \quad (21) \]
Figure 7 shows the proposed circuit. Due to $I_m = I_{15} - I_{12}$, $I_{in1} = I_w + I_z$, $I_{in2} = I_w - I_z$, and $I_{03} = K^{-1}V_0^2$ we have
\[ I_m = I_z + \frac{I_w I_z}{4I_{03}} \]  (22)
Due to $I_{out} = I_m - I_z + I_c$,
\[ I_{out} = \frac{I_w I_z}{4I_{03}} + I_c \]  (23)
where $I_w$ is generated by scaling the current mirrors,
\[ I_w = I_{01}(s(x - 1.5)) \]  (24)
Substituting (24) and (25) into (23), we have
\[ I_{out} = \frac{I_{01} I_w}{4I_{03}}(s(x - 1.5)((x - 1.5)^2 + 1)^n) + I_c \]  (26)
which is the S-shape correction function shown in (1).

The “Selectable n circuit” in Fig. 7 generates $I_n = n I_x \ln((x - 1.5)^2 + 1)$ by using different current-mirror ratios. Therefore, the output of the exponential circuit will be
\[ I_x = I_n ((x - 1.5)^2 + 1)^n \]  (25)

5 Error Analyses and Simulations
The proposed circuit was simulated by HSPICE using 0.35μm CMOS TSMC process parameters with 1.8V supply voltage. However, there are four error sources in the proposed circuit. The first one is called K-error. Suppose that $K_p = K_n$ at $I_x = 60 \mu A$, we have $K_p \neq K_n$ for $I_x \neq 60 \mu A$. The unequal K is against the assumption in the basic circuit. The variant K is also against the assumption of the constant K. The second one comes from the channel-length modulation for short-channel transistors, which makes the errors on (8) and (9). The third one is the mismatch of current-mirror. The last one is the truncation error of the Taylor series of $\ln(x)$ and $\exp(y)$. To decrease the errors, we tune the ratios of W/L of some transistors and current sources block by block. Table 1 shows the aspect ratios of the MOS transistors in Fig. 7. The $I_o = 380 \mu A$, $I_i = 150.9 \mu A$, $I_\sigma = 9.11 \mu A$, and $I_s = 60 \mu A$.

For input current range from 0μA to 120μA, we could watch $x$ range from 0 to 3. The output theoretical value will be the value of (26) for $I_{01} = 10 \mu A$, $I_{03} = 5 \mu A$, $I_u = 40 \mu A$, and $I_c = 25.24 \mu A$. Suppose that node X is one of nodes A, B, C, and D. As node X is switched to VDD, we denote $X = 1$. If node X is switched to GND, we denote $X = 0$. The corresponding $s$ and $n$ for the different switch combinations are show in Table 2. Figure 8 shows the S-shape correction curve for $n = 0.5$. Fig. 7 CMOS current-mode selectable S-shape correction circuit.
The -3dB bandwidths simulation at $I_{\text{out}}$ shown in Fig. 9 are 49, 49.2, 49.8, and 50.4 MHz for n being 0.3, 0.4, 0.5, and 0.6, respectively.

The maximum power dissipations are 7.8, 7.9, 8.0, and 8.4 mW for n being 0.3, 0.4, 0.5, and 0.6, respectively. Figure 10(c) simulates an LCD with an S-shape characteristic. Figure 10(b) is our correction simulation result for n = 0.4, which has similar histogram with an original picture shown in Fig. 10(a).

### Table 1
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### 6 Conclusion
The S-shape correction function with adjustable scale and shape was investigated. The shape selection using a companding technique was presented. The simulation results show the improvements in image quality. For different n selections, the proposed circuit can achieve about 50 MHz bandwidth for dissipating 8.4 mW at most.

### References:


Fig. 10 Image quality simulation for the current-mode S-shape correction circuit.