A Linear OTA with improved performance in 0.18 micron

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Abstract— The increasing demand of personal health monitoring products with long battery life has forced designers to use of those circuits which consume low power. Operational Transconductance Amplifier (OTA) operating in subthreshold (weak inversion) region introduces a versatile solution for the realization of low power VLSI building blocks. This paper is focused on design of high performance OTA through use of high output impedance low-voltage current mirror circuit and observed responses proved to be much better than that of different complex mirror architectures. The proposed OTA incorporates high linearity and better performance in low-frequency applications. The achieved open loop dc gain and unity gain bandwidth (UGB) is 68.67 dB and 70.56 KHz respectively. The OTA is operated at supply voltage of 0.9 volt and consumes power in range of nanowatts. The architecture of OTA is performed in a standard TSMC 0.18 micrometer technology on BSIM 3v3 model and simulation results were analyzed using ELDO Simulator.

Keywords— Bulk-input, Low supply voltage, Linear range, subthreshold OTA, Wilson mirror.

I. INTRODUCTION

Today the trend of scaling down channel length in CMOS technology to facilitate submicrometer high density systems on a single integrated circuit (IC) and emergence of portable devices like Ambulatory Brain Computer Interface (ABCI) systems, insulin pumps, hearing aids and mobile communications had led to development of circuits that consumes less power. The rapid increasing use of battery-operated portable equipment in application areas such as telecommunications and medical electronics imposes the use of low-power and small-sized circuits realized with VLSI (very large scale integrated) technologies. As the technology of biomedical instrumentation amplifier is moving towards portability, lower power consumption is highly desirable for devices which monitors patient whole day.

Circuits needed for processing of biological signals are a typical and good example of low-power and small-sized building blocks. The main features of biological signals are their low amplitude and low frequency range. In biomedical instruments to process low frequency signals, low-pass filter circuits with sufficient large time constant are required, typically for a capacitor value of less than 5pF which in turn require very high resistance. For example, in ECG signal detection, low-pass filter required must have cut-off frequency less than 300 Hz for which use of low-power continuous-time OTA-based filters are preferred [1]. However, major limitation of conventional OTAs is its limited linear range. As device sizes are scaling down, traditional saturation-based OTAs are facing design challenges to overcome poor linearity and limited output impedance. Various techniques for extending linear range have been proposed among which the OTA architecture used for this paper is discussed in [2]. It provides linearity of about 1.7 volt. The paper concentrates on not only to achieve high linearity but to increase the gain of amplifier with better performance. Since the OTA is a current source device, the output impedance of the device must be high.

The proposed OTA uses high output impedance low-voltage current mirror circuit as a replacement to simple current mirror (CM) which provides sufficient increase in open loop dc gain with better frequency response at extremely low voltage. Section II covers short review on bulk-driven MOS transistors, followed by basic operation of OTA and its modified architecture is discussed in section III. In section IV, simulations results are discussed and finally conclusion in section V.

II. REVIEW OF BULK DRIVEN MOS

Threshold voltage of future CMOS technologies may not decrease much below what are available today, creating difficulties for analog designers to design analog circuits with lower supply voltage. To support low threshold voltage devices proper scaling of supply voltage must be done to appropriately bias the device. A promising approach in low voltage analog circuits is “bulk-driven” MOSFET method where the gate-to-source voltage is set to a value sufficient to form inversion layer while the input signal is applied to bulk terminal.

In gate-driven MOS transistor, the gate-to-source voltage controls the drain current of the transistor while for a bulk-driven MOS transistor where threshold voltage is a function of the bulk-to-source voltage, controls the drain current. Using this technique, transistor can remain in active mode even at zero-input bias voltage. However, there are few drawbacks in bulk-driven transistors like one most important drawback is its low dc gain [3]. The current expression for well-input MOS transistor in subthreshold mode is given by

\[ I = I_0 e^{-\frac{kT}{V_{th}}} \cdot e^{-(V_{gs}-V_{th})/kT} \]  

(1)
where $V_{gs}$ and $V_{ws}$ is the gate-to-source and well-to-source voltage, $k$ is subthreshold exponential coefficient, $I_0$ is subthreshold exponential parameter, $V_T = KT/q$ is thermal voltage. From (1), it can be observed that dependence of $k$ on gate and $(1-k)$ on well creates the condition that when gate is active, well remains inactive and when well is active gate is inactive.

III. PROPOSED OTA

A. The Amplifier Core

The OTA is a transconductance type device, which means that the input voltage controls an output current by means of the device transconductance, labeled $g_m$. This makes the OTA a voltage controlled current source (VCCS). In the past few years, engineers have improved the linearity of MOS transconductor circuits. Such improvement has been primarily in the area of above-threshold, high-power, high-frequency, continuous time filters. The OTA shown in Fig. 1 which provides a linearity of 1.7 volt is detailed in [2].

It uses combination of four techniques to enhance its linearity. Firstly, the well terminals of the differential-pair transistors $M_1$ and $M_2$ is used as amplifier inputs. Secondly, feedback techniques like source degeneration via $M_1$ and $M_2$ and gate degeneration via $M_3$ and $M_4$ provide further improvement. Finally, $M_5$ and $M_6$ used as bump transistors. The bump-linearization technique is used to overcome parasitic effects which occur at low input voltage, generally less than 1 volt.

The $P$ transistor act as bias current source and the remaining transistors $M_1$, $M_2$, $M_3$ and $M_4$ are configured as simple current mirrors. Besides, there is an offset voltage adjustment which sets $V_{so}$ around 5 mV less than $V_{so}$. To improve OTA performance, simple CM used is replaced by high output impedance low-voltage CM. This technique not only compensates the offset voltage but its high impedance increases its gain compared to other CM.

Analyzing left half-circuit of OTA of Fig. 1, the overall transconductance $g$ is reduced by a feedback factor $\left(1 + 1/k_p + 1/k_n\right)$,

$$g = \frac{1-k}{1+1/k_p + 1/k_n} \quad (2)$$

where $1/k_p$ and $1/k_n$ are the loop gain of $S$ and $GM_1$ transistor respectively.

From (1)

$$I \propto e^{-(V_s-V_w)/V_T} \quad (3)$$

$$\frac{I_{OUT}}{I_B} = \frac{e^{\alpha V_s/V_T} - 1}{e^{\alpha V_s/V_T} + 1} = \tanh \left( \frac{g V_s}{2V_T} \right) \quad (4)$$

Solving

$$\frac{I_{OUT}}{I_B} = \frac{e^{\alpha V_s/V_T} - 1}{e^{\alpha V_s/V_T} + 1} = \tanh \left( \frac{g V_s}{2V_L} \right) \quad (5)$$

where $V_s = V_{a2} - V_{a1} = V^+ - V^-$

$$I_{OUT} = I_B \tanh \left( \frac{V_s}{V_L} \right) \quad (6)$$

where $I_{OUT}$ is the output current, $I_B$ is the bias current of $P$ transistor, $V_L$ is the linear range of OTA expressed by

$$V_L = 2V_T/g \quad (7)$$

where $g$ is the overall reduced transconductance of OTA.

From $\tanh$ series expansion $\tanh \left( \frac{x}{2} \right) = \frac{x}{2} - \frac{x^3}{24} + \ldots$; it can be observed that if $V_L$ is made sufficiently high then cubic order term in the $\tanh$ series expansion can be easily neglected thereby reducing distortions of non-linearity.

B. High output impedance low-voltage CM

A current mirror is characterized by the current level it produces, the small-signal ac output resistance and voltage drop across it. The simple current mirror uses the principle that if gate-to-source potentials of two identical MOS transistors are equal then their channel currents are equal. In late 1967, George Wilson proposed a modified current mirror just by adding one extra transistor which increases output impedance.
to appreciable amount and named the circuit as Wilson current mirror. The Wilson current mirror implemented using three nMOS transistors is shown in Fig. 2 (a). The architecture consists of simple current mirror and a current to voltage converter connected in the feedback loop. If there is any increase in output current due to output voltage variation, the simple current mirror transistors senses this variation and feed back the current to input node thereby reducing gate voltage of output transistor followed by reduction in original current increase. But these current mirror suffered systematic gain error along with unequal voltages across input and output transistors. To compensate systematic gain error, Barrie Gilbert; added a fourth transistor in diode connected form in the input branch and later this circuit became famous by name improved Wilson CM [4] as shown in Fig. 2 (b).

Assuming the output resistance of current source infinite, the effect of diode connected transistor $M_{s4}$ is neglected, and the output resistance $r_{out}$ (neglect 2nd order effects for simplicity) is given by [5].

$$r_{out} = r_{s3} \left(1 + \frac{g_{m3}(1 + g_{m3}r_{s4}r_{in}) + g_{m3}}{g_{m2} + g_{m2}}\right) \approx g_{m3}r_{s3}r_{in}$$  \hspace{1cm} (8)

where $g_{m}$, $r_{s}$ and $g_{o}$ are the transconductance, incremental output resistance, and output conductance of transistors. The improved Wilson circuit requires an input voltage of two diode drops and output compliance voltage incorporates a diode drop plus saturation voltage. Such diode drop made Wilson mirror unattractive for low-power design units. To overcome this, a new Wilson topology was introduced [6], which sense the output current at low input voltage of a diode drop plus a saturation voltage whereas output senses only two saturation voltage. As seen from architecture of Fig. 3 (a), the diode connected transistor on input side biased by current source $I_b$, causes the input voltage to decrease much lower than gate voltage needed as in case of simple mirrors to sink input current. This makes it a low voltage high-swing improved-Wilson current mirror circuit. The mirror achieves high output resistance by using negative feedback and is directly proportional to the magnitude of the loop-gain of the feedback action from the output current to the gate of output transistor $M_{s3}$. The transistor $M_{s1}$ and $M_{s2}$ samples the $I_{OUT}$ and compares it with $I_{in}$. In combination with current source load $I_{in}$, transistor $M_{s1}$ act as a common source amplifier used to maintain gate voltage of $M_{s3}$ to avoid mismatching of $I_{OUT}$ to $I_{in}$. The small-signal output resistance remains almost the same as (1). The transistor $M_{s4}$ forces the drain voltages of $M_{s1}$ and $M_{s2}$ to be equal and reduces unwanted offset in the output current. The transistor $M_{s4}$ exhibits low output resistance of $1/g_{m}$. In order to enhance its output resistance, the diode structure is replaced by cascode one as shown in Fig. 3 (b). The mirror provides an increase in output resistance by factor of $g_{m}r_{s4}r_{in}$, given by [7].

$$r_{out} = r_{s3} \left(1 + \frac{g_{m2}(1 + g_{m2}r_{s3}r_{in}) + g_{m3}}{g_{m2} + g_{m2}}\right) \approx g_{m3}g_{m2}r_{s3}r_{in}$$  \hspace{1cm} (9)

C. Proposed OTA using high output impedance low-voltage CM

The proposed OTA is shown in Fig. 4. The architecture works on low supply voltage thereby introducing appreciable reduction in power consumption. A bias current generator circuit is connected to OTA as a replacement to bias transistor $P$, which generates current in the range of nanoamperes.
Figure 4. Proposed OTA using high output impedance low-voltage CMOS transistors

Transistors $M_{p13} - M_{s16}$ and $M_{p11} - M_{p12}$ along with $R_s$ comprises current generator circuit. As the source-to-gate voltage of $M_{p11}$ and $M_{p12}$ are equal their corresponding currents are equal, i.e. $I_{D11} = I_{D12}$ (neglect channel length modulation). Furthermore, it can be noted that $I_{D13} = I_{D11}$ and $I_{D14} = I_{D13}$. The equation for drain current of MOS transistor is given by

$$I_D = \frac{1}{2} \mu \frac{C_{ox}}{L} W (V_{GS} - V_{Th})^2$$  \hspace{1cm} (10)

Solving for $V_{GS}$

$$V_{GS} = \sqrt{2I_D \frac{C_{ox}}{\mu}} \frac{W}{L} + V_{Th}$$  \hspace{1cm} (11)

In Fig. 3

$$V_{GS,n13} = V_{GS,n14} + I_{D,n14}R_S$$  \hspace{1cm} (12)

From (11)

$$\sqrt{2I_{D,n13}} = \sqrt{2I_{D,n14}} \frac{C_{ox}}{\mu} \left( \frac{W}{L} \right)_{M_{n13}} + I_{D,n14}R_S$$  \hspace{1cm} (13)

Rearranging above expression and solving for $I_{D,p12}$ by equating equivalent currents, the $I_{D,p12}$ is given by

$$I_{D,p12} = \frac{2}{\mu \frac{C_{ox}}{\mu} \left( \frac{W}{L} \right)_{M_{n13}}} \frac{1}{R_S} \left( 1 - \frac{W}{L} \right)_{M_{n14}}^2$$  \hspace{1cm} (14)

The output current $I_{bias}$, that is, $I_{D,p13}$ is now the function of $I_{D,p12}$. By adjusting the aspect ratio of $M_{p13}$ relative to $M_{p12}$, desired $I_{bias}$ can be obtained. The $W/L$ ratio of $M_{p13}$ is kept four times lower than $M_{p12}$, which results in output current $I_{D,p13} = I_{bias} = I_{bias}/4$.

IV. SIMULATION RESULTS

The design of low voltage, high performance OTA circuit on TSMC 0.18 micron technology provide low power consumption exhibiting performance levels that satisfy the demands of state-of-art mixed-signal circuits. The simulations were performed under normal condition (room temperature) using ELDO Simulator and BSIM 3v3 model of MOS. Current generator circuit generates $I_{bias}$ of 65nA at $R_S = 10k\Omega$. The supply voltage is kept at 0.9 volt. Fig. 5 shows the linear response of proposed OTA. In Fig. 6, the ac response of OTA under no load condition is shown. For comparison of open-loop dc gain of proposed OTA, the simulations were performed using different CM circuits and the best result can be seen in case of OTA using high impedance low-voltage CM circuit. The achieved dc gain and UGB of proposed OTA is 68.67 dB and 70.56 KHz respectively. Its low UGB supports it for use in biomedical applications. When configured as follower integrator using 1 pf of load shown in Fig. 7, it tracks the input perfectly whereas the OTA using different Wilson
CM topology faces offset at low input voltage. The dc response of follower integrator is shown in Fig. 8.

\[ V \]

**CONCLUSION**

This paper explored the approach of low-voltage OTA design using the bulk-driven technique and enhancement of output impedance using high output impedance low-voltage CM circuit. The design of such low voltage, high performance OTA circuit on TSMC 0.18 micron technology satisfies the required parameters for its implementation not only in power-saving devices but also in biomedical portable devices like biomedical implantable sensors, disk read channel integrated circuits (ICs), video filters, ADSL front-ends, and RF ICs.

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**REFERENCES**


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![Figure 5. Linear response of proposed OTA](image)

![Figure 6. Open loop dc gain of OTA under different CM circuits](image)

**Figure 7. Follower Integrator**

**Figure 8. DC response of follower integrator using different CM circuits**