Solid-state fault current limiter for voltage sag mitigation and its parameters design

B. Boribun and T. Kulworawanichpong

***Abstract*—**Due to the difficulty in electric distribution network reinforcement and the interconnection of more distributed generations, fault current level has become a serious problem in system operations. The utilization of solid-state fault current limiters (SSFCLs) in power system provides an effective way to suppress fault currents and result in considerable saving in the investment of high capacity circuit breakers. The limiter must reduce fault current to a level below the momentary capabilities of the system components and permit correct relay operation within the interrupting capabilities of circuit breakers. The additional feature of SSFCL is the improvement of power quality by reduces the voltage sag during the fault. The limiter impedance is tuned by the gating controller of thyristor. Design methods and component selection criteria are developed. The simulation results, limiting effect, and mitigation capability are discussed and summarized.

***Keywords*—**Solid-state fault current limiter, voltage sag, simulation, power quality.

I. Introduction

NOWADAYS, the growth of electric power consumption has resulted in an increase in the magnitude of the fault current. Because the 22-kV electric power distribution systems are closet with consumers, three important performance parameters of system must be evaluated. These corresponding parameters are the capability of continuous supplying electric power, power quality, and safety. Normally, the fault current of large electric power distribution systems more than 5 times of its normal operating current [1]. The fundamental problems with high fault currents were described by [2] as:

– After a fixed time of fault occurring, recloser open the faulty line for protect transformer, feeder, bus, load, and consumer. In the case of very large fault current, recloser may open the no fault line. This scenario is shown in Fig. 1. The tested scenario is the fault at bus 5. The fault current is more than pickup setting of relays R1-R4. If fault current level still exists until the last relay is operated, it is sure that all relays will operate. The corresponding effects are the removing of bus 3-5 from the electric power line. The consumers S_3-S_5 will encounter problems because of the power outage. In case of the fault current level reach the pickup setting of only relay R1, R2-R3 unable to detect the fault. Therefore, loads of buses 2-3 are still gain the electric power.

– The assessment of rated and performance of protective devices are required because of more fault current. Unfortunately, some devices are degrading and need the replacement. The extra budgets for installation and maintenance are basic needs.

– Fault state effects directly to reliability index of electric power system. It depends on number of removed loads and level voltage sag. The optimization of protection and solution for this problem is required.

– High mechanical dynamic stress due to electromagnetic force throughout feeders or any devices carrying the fault current. Adequate mechanical reinforcement must ensure that equipment can withstand these stresses.

– The physical difficulties of high current interruption lead to the need for sophisticated mechanical contact systems as circuit breakers.

The main goal of this paper is to describe voltage sag problem during the fault and mitigation method using SSFCLs. The performance assessment was evaluated using voltage of point of common coupling (PCC). The simulation results and discussion were also proposed.

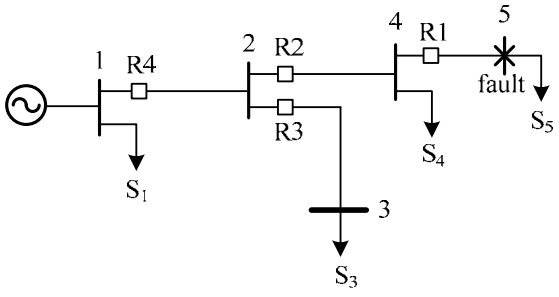

Fig. 1 relay location of 5-bus system and fault location

II. Literature Review

Voltage sags have become one of the most important power quality concerns in recent years. According to survey results

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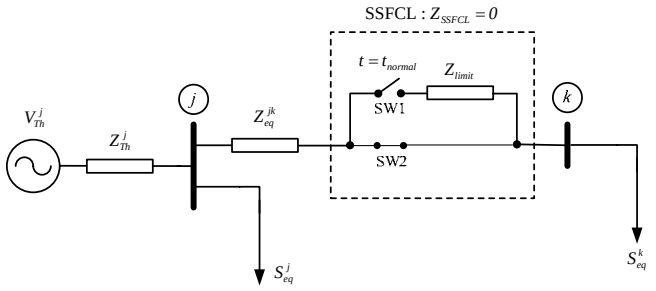
across the U.S., voltage sags and short-duration power outages account for 92% of power quality problems encountered by industrial customers [3]. In a radial power distribution system, a fault in one location of many feeders will produce voltage sag at the substation bus, thus affecting adjacent feeders. If any of these feeders supplies sensitive loads, like adjustable speed drives, PLC's, computer systems, etc., problems may arise at the customer loads where these voltage sags are seen as interruptions [4]. It is suggested that a way to reduce these voltage sags to acceptable values can be achieved by limiting the fault current in the distribution feeders. IEEE Standard 1159- 1995, Recommended Practice on Monitoring Electric Power Quality, provides a common terminology that can tie used to discuss and assess rms voltage variations [5].

The voltage sag mitigation during the fault was presented by [6] which applied thyristor controlled series capacitors (TCSCs). The study provides a means of quantifying such assessments and a common terminology for discussion. This capability of limiting fault current is an additional feature presented by TCSCs, which may improve the quality of supply of power systems, in addition to others such as power flow control, power system stability enhancement, mitigation of subsynchronous resonance, etc. The power quality improvement considered both voltage sags and the associated phase angle jumps are presented by [7]. This study focuses on the proper selection and design of suitable SSFCL configurations for application on the power systems to mitigate voltage sags in term of voltage magnitudes and phase angle jumps. Sensitivity analysis was also performed to determine the effects of varying fault current limiter (FCL) parameters on its performance in term of voltage supporting capability, phase angle jump reduction and fault current reduction.

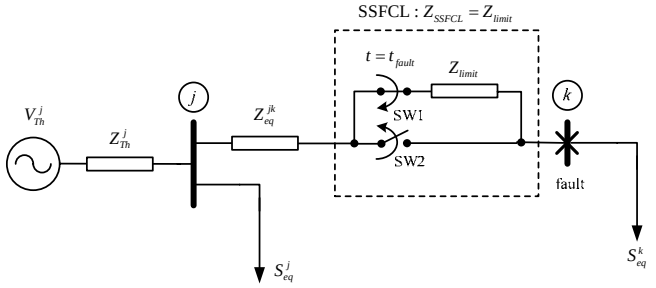
A simple series LC circuit reducing voltage sags through FCL are presented by [8] and [9]. The capacitor shunted by a metal oxide varistor (MOV) and LC were tuned at the net frequency. The short circuit current can be effective limited since the expected voltage sag amplitude during faults can be dramatically reduced. Reference [10] was presented the application two types of FCLs as a resistive type (R-type) FCL and an inductive type. It was found that the range of the limiting impedance for the L-type FCL to suppress the fault current out of the customer system and the voltage sag in the customer system is larger than that for the R-type FCL.

Reference [11] was presented waveform analysis of the bridge type SFCL during load changing and fault time. In fault conditions, the peak value of the waveforms is considered in calculating the voltage drop at load terminal during the load changing time. The analysis can be used in selecting an appropriate inductance value for designing such SFCL.

Reference [13] was detailed the installation of SSFCL on power circuit and its firing control strategy. The simulation was demonstrated in graphical diagrams using elements of the MATLAB's Power System Blockset (PSB). The simulation results showed that, with a moderate sensing technique to monitor voltage and current of the protected feeder, the SSFCL can interrupt fault effectively.



(a) open circuit



(b) current limitation

Fig. 2 two states of SSFCL operation

Regarding to all previous references, this paper propose the method of voltage sag mitigation using SSFCL and parameters optimization. The first part of paper presents the operation and design of proposed SSFCL. The second present the simulation results. The analysis and discussion was performed on the third part of paper. Finally, the conclusion of this work was presented.

III. SOLID-STATE FAULT CURRENT LIMITERS

A. Principle of Operations

The advantage characteristic of SSFCL is fault current limitation. The increase in reliability index as a result of the large current is reduced to the suitable level which corresponds to the SSFCL design specification. Under normal operation, SSFCL is controlled to be zero impedance device, power quality compensator, harmonics filter, or stabilizer. The topology of connection and switching of SSFCL when electric power system operates in normal situation is shown in Fig. 2(a). During the time which normal operation, the switch SW1 and SW2 is close. The limiter impedance is separated from feeder and equivalent impedance of SSFCL is zero. It's clear that SSFCL have no effect on system operation.

The system has normal operation until fault occur on bus k at time equal to t_{fault} as shown in Fig. 2(b). The switch SW1 is close while SW2 is open. The limiter impedance is connected

to feeder result of equivalent impedance of SSFCL is Z_{limit}. The duration of fault current limitation mode depends on the topology of SSFCL, reduction rate of fault current, and level of fault current. The limiter impedance is switched to original status when fault current level is equal to the desired value and the electric system is return again to the normal operation.

B. Design Specifications of SSFCL

The suitable SSFCL for application on the system should meet the following requirement:

– The varying of voltage magnitude, V, at the PCC should be minimized. It means that the difference of voltage magnitude at the PCC between pre-fault state, during fault state, and post fault state should equal to zero as (1),

$$V_{prefault} - V_{fault} \approx 0 \tag{1}$$

when $V_{prefault}$ and V_{fault} are the voltage magnitude of pre-fault state and post fault state respectively.

– As the varying of voltage magnitude at the PCC, the different of phase angle should be closed to zero which following to (2),

$$\phi_{prefault} - \phi_{fault} \approx 0 \tag{2}$$

when $\phi_{prefault}$ and ϕ_{fault} are the phase angle in pre-fault state and post fault state respectively.

– The most importance of performance of FCL is the capability of current limitation. When the fault occur and the FCL is inserted automatically in the optimal position of feeder, the FCL must reduce fault current to a level between relay current and breaker current. The reduced fault-current must satisfy the condition as show in (3).

$$I_{relay} < I_{fault} < I_{breaker} \tag{3}$$

when I_{fault}, I_{relay}, and $I_{breaker}$ are the fault current, current level at which protective (over-current and directional over-current) relays operate, and current level above which circuit breakers will be damaged respectively.

– The total cost of FCL components and the installation should be the consideration factors. The various type of FCL may be R, L, C, transformers, switching devices, or others. The selection of these devices and the installation after the design process must consider the cost is within the budget of the utility which recent SSFCL development faced the budget problem in the part.

C. Limiter Impedance Calculation

The most faults in electric power system are unsymmetrical fault but the balanced three-phase fault is often analyzed for CB selection. It's the same idea as impedance calculation for SSFCL. The fault current can be expressed by

$$I_k^{sc} = \frac{V_k}{Z_{kk}} I_b \tag{4}$$

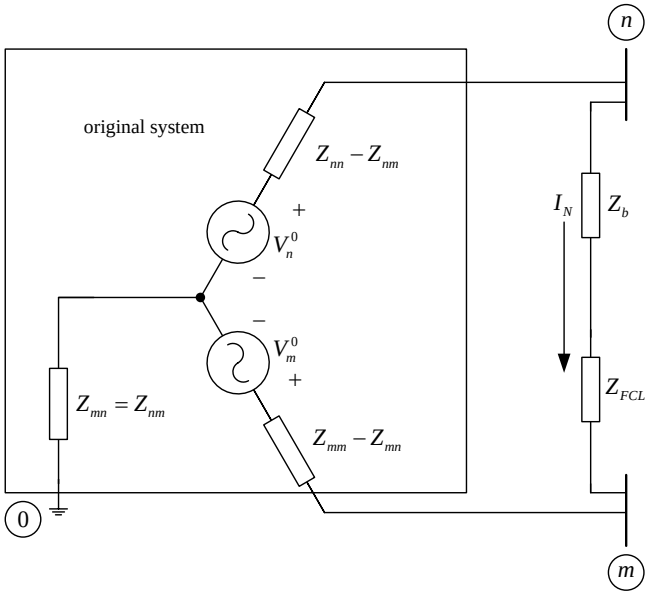


Fig. 3 Thevenin's equivalent network with SSFCL location between bus *m* and *n*.

when V_k is pre-fault voltage on bus k, I_k^{sc} is fault current on bus k, I_b is base current, and Z_{kk} is Thevenin's impedance of bus k. The impedance Z_b is added to a feeder of original network between bus *m* and *n* on feeder result of the change of bus impedance matrix elements as

$$Z_{xy}^{new} = Z_{xy} - \frac{\left(Z_{xm} - Z_{xn}\right)\left(Z_{my} - Z_{ny}\right)}{Z_{mm} + Z_{nn} - 2Z_{mn} + Z_b} \tag{5}$$

when Z_{xy} is original element of $\boldsymbol{Z}_{bus}$, and the modified value of element of $\boldsymbol{Z}_{bus}$. The appropriate time after fault occurred, SSFCL is operated. The Thevenin's equivalent network is shown in Fig. 3. The installation of SSFCL is the addition impedance on partial network results in

$$Z_P = \left(-Z_b\right) // \left(Z_b + Z_{FCL}\right) = -\frac{Z_b\left(Z_b + Z_{FCL}\right)}{Z_{FCL}} \tag{6}$$

The variation of diagonal impedance of $\boldsymbol{Z}_{bus}$ after SSFCL operated is equal to

$$\Delta Z_{ii} = -\frac{\left(Z_{im} - Z_{in}\right)^2}{Z_{mm} + Z_{nn} - 2Z_{mn} + Z_P} = \frac{C_2}{C_1 + Z_P} \tag{7}$$

The bus current reduces to

$$\Delta I_{i,F} = \frac{V_i}{Z_{ii} + \Delta Z_{ii}} - \frac{V_i}{Z_{ii}} \quad (8)$$

Substituting for ΔZ_{ii} from (7) into (8), the reduction of fault current becomes

$$\Delta I_{i,F} = -\frac{V_i}{Z_{ii}} \frac{C_2}{(C_1 + Z_P) Z_{ii} + C_2} \quad (9)$$

If the fault current is reduced from $\Delta I_{i,N}$ to $\Delta I_{i,F}$, optimum limited impedance Z_P can be calculated from (9) which the result is [12]

$$Z_P = \frac{I_{i,F}}{I_{i,N} - I_{i,F}} \frac{C_2}{Z_{ii}} - C_1 \quad (10)$$

Substituting for Z_P from (10) into (6), the desired impedance for SSFCL becomes

$$Z_{FCL} = -\frac{Z_b^2}{Z_b + Z_P} \quad (11)$$

The values of Z_P and Z_{FCL} depend on the pick-up setting of relays and the level of fault current. The desired impedance Z_{FCL} is evaluated using the firing control of thyristor as [13].

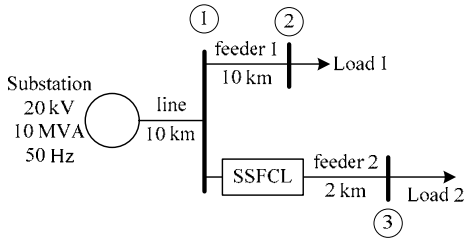


Fig. 4 the experimental system

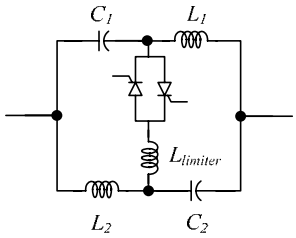


Fig. 6 the configuration of study SSFCL

D. Experimental System

To verify the performance of SSFCL, the electric distribution system is selected and simulated. The configuration and data of 3-bus system are shown as Fig. 4. The optimum limiter impedance was calculated by (11). The firing angle of thyristor is optimized to pick-up setting of relays and the level of fault current. The component specifications are calculated according to the equivalent impedance of SSFCL as show in Fig. 5.

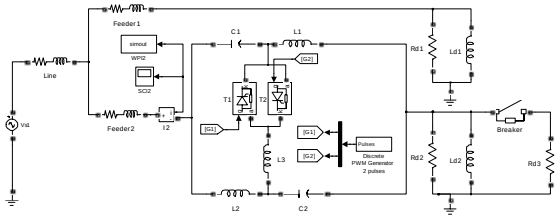


Fig. 7 simulation system on Simulink

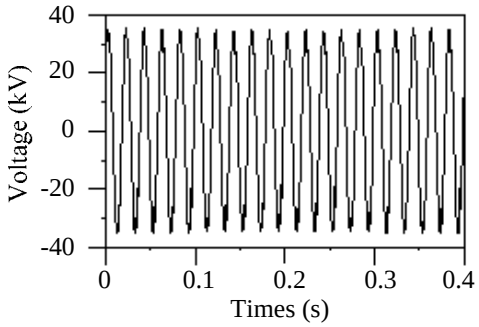


Fig. 8 voltage waveform of PCC

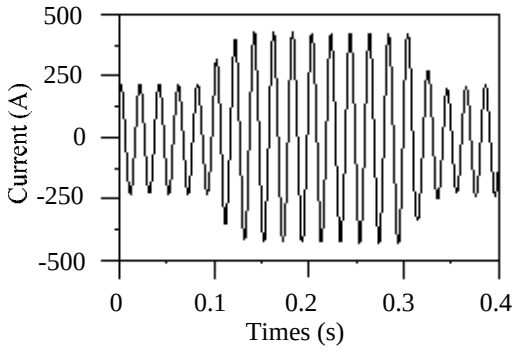


Fig. 9 current waveform of PCC

E. Simulation Results

The experimental system are simulated in Simulink is shown in Fig. 7. The fault single-phase to ground is occurred on feeder 2 and was behind the PCC. The time step is 1×10-4 s and total simulation time is 0.4 s. The resonant frequency of each branch is equal to

$$\omega = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}} \quad (12)$$

Refer to (11) and (12), the optimum current limiter was inductor equal to 0.22 H. The main goal of the assessment is

voltage regulation of substation and the varying of voltage and phase angle of PCC. The fault current limitability of SSFCL is the normal performance should be investigated. According to simulation results, the substation voltage and current waveform as show in Fig. 8 and Fig. 9. According to the simulation results, the voltage of PCC is regulated. During the time of fault (0.1–0.3 s), the voltage magnitude are approximately constant as the pre-fault state. On the other hand, the magnitude of voltage sag is nearly to zero. To consider the limitability of fault current limiter, the current is limited to the level less than 2 times of rated current. According to the simulation results, it's clear that the ability of fault current limitation and voltage sag reduction is successful.

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