Overcurrent Protection in DC/DC Converters – An Overview

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Abstract: - Fault protection is commonly available in most of power management chips to date and its accuracy highly praised, mainly in cases where driving rates reach a few Amperes, or even above. In this paper, some of most common techniques for overcurrent protection (OCP) applied to both switching and linear DC/DC supply voltages are revisited and their trade-offs analyzed. Current limitation approaches based on sense resistors and sense FETs are described, with special emphasis on circuits that present high immunity to process, voltage and temperature (PVT) variation. Simulation data are provided for distinct approaches, as well as experimental results for a fast-response current limiter with internal compensation against process and temperature (PT) spread.

keywords: Current Sensor, Current Limiter, DC/DC Converters, Power Management

1. Introduction

The need to measure the current flow in electronic systems to protect them against catastrophic failures is becoming increasingly widespread. Reasons for this include the growing mobile consumer market, such as cell phones, notebooks and digital cameras, as well as the spread of automotive electronics. Additionally, microprocessor-based boards require power supply rails of high integrity, even under extreme conditions such as hot-swapping.

State-of-art integrated power-supplies sense the load current for fast over-current protection (OCP) [1-3]. Fault protection accuracy is highly praised, mainly for stirring rates of several Amperes. The current detector/limiter embarked in the DC/DC converter should promptly flag the fault to protect the chip against overcurrent. Since the detector should not interfere with normal operation, the current detection threshold I_{TH} has to precisely fall into an interval whose boundaries are defined by the maximum current and the current beyond which thermal dissipation would endanger the power device and/or the chip integrity.

This overview discusses OCP schemes applied to linear and switching regulators. The remainder of the tutorial is organized as follows. Basic current sensing schemes for DC/DC converters are revisited in Section 2 Principle and design of current limiters of low sensitivity to process, voltage and temperature (PVT) variation are described in Section 3, alongside simulation data. Experimental data are presented in Section 4, whereas concluding remarks are summarized in Section 5.

2. Current Limiter Description

As illustrated in Fig. 1, the current limiter usually comprises a current sensor followed by an arbitration circuit (ABT), whose basic function is signalize the faulting condition, so that the control circuit can turn off the regulator power stage as long as the fault persists. Additionally, the limiter clamps to a safety value the current delivered to the load.

The arbiter performs on-time comparison between the sensor current I_{SNS} and a reference current I_{REF}, the latter a scaled-down value of the maximum load current allowed under normal operation, here denoted as I_{TH}. In case $I_{SNS} < I_{REF}$, the output FLAG remains negated and the limiter has no effect on the converter functionality. Otherwise, FLAG is asserted and an action is taken by the control circuit, such as disabling the power devices to prevent them from overheating, and likely, permanent damage. Since the sensor is a key element in the current detector, the most common techniques of current sensing for OCP are now revisited.

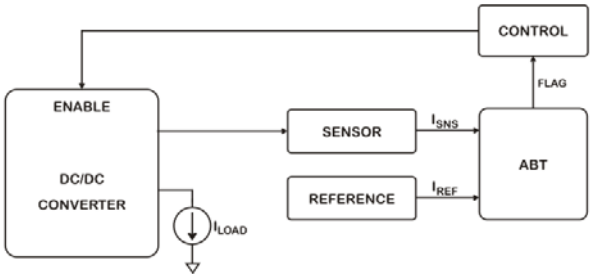

Fig. 1. Block diagram of a current limiter

2.1 Resistor-Sense Current Sensors

A sense resistor R_{SNS} is inserted along the power-device current path to develop a voltage proportional to the regulator output current [3]. Fig. 2 displays this type of sensor applied to a switcher. However, ohmic losses decrease efficiency, mainly in high-current applications, so that the use of resistors with very low values (<<1Ω) becomes mandatory [2]. Accuracy relies then on the resistor material and typically corresponds to ±10%, for a metallic resistor with zero-temperature coefficient (ZTC) [3].

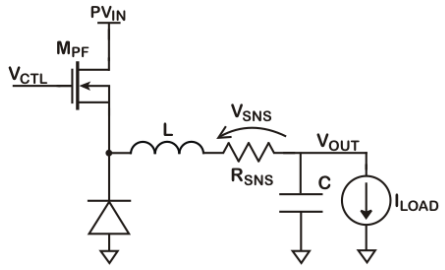

Fig. 2. Series-resistor sense

To further improve the regulator efficiency, one can use components inherently available in the power stage, such as series resistances associated with the inductor and power switches. However, these sensing techniques suffer from uncertainties on the absolute value of such parasitic elements, as they are dependent on fabrication process spread, temperature, current rate, manufacturer and cost. These inaccuracies are commonly mitigated by end-of-line factory trimming, at expense of circuit complexity and testing time.

Since the MOSFET switch in buck converters acts like a resistor when turned on, a lossless strategy of sensing current is to monitor the drain-source voltage of either the high-side (HS) or low-side (LS) transistor. As shown in Fig. 3, this voltage drop is converted into current by means of the on-resistance R_{DSon} of triode-operating power FET. Although cost-effective, this solution lacks precision, as R_{DSon} is a strong function of process parameters, gate voltage and temperature [4],

$$R_{DSon} = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}\left(V_{GS} - V_{TH}\right)} \qquad (1)$$

where (W/L) corresponds to transistor aspect-ratio, μ to carriers mobility, C_{ox} to gate-oxide capacitance per area unit and V_{TH} to threshold voltage. Tolerances as high as 50% on R_{DSon} due to process, voltage and temperature (PVT) variations should be considered when designing such current sensors.

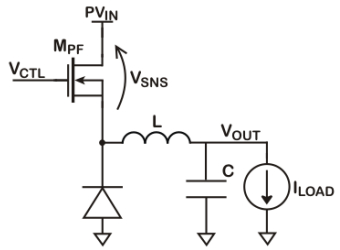

Fig. 3. Lossless R_{DSon} sensing

2.2 MOSFET-Sense Current Sensors

Sense-FET techniques are usually employed in smart-power chips. As displayed in Fig. 4, a built-in sense transistor M_{SNS} is placed in current-mirror configuration with the integrated pass-transistor M_{PF}, while exhibiting an aspect-ratio (W/L) significantly smaller than the latter. In practice, the scaling factor M varies from 1000 to 10,000.

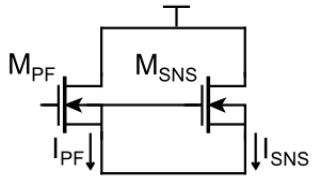

Fig. 4. Sense-FET approach

Alternatively, a sense resistor R_{SNS} can be added in series with M_{SNS}, as shown in Figure 9. The sensed current I_{SNS} is then converted into voltage V_{SNS} developed across R_{SNS} terminals. Since R_{SNS} is not along the power path, the regulator efficiency is practically unaffected. Again, the current mirroring ratio I_{SNS}/I_{PF} suffers from unbalanced drain-source voltages. Furthermore, the exactness of this conversion is limited to manufacturing tolerances affecting the absolute value of R_{SNS}, not to mention its variation with temperature.

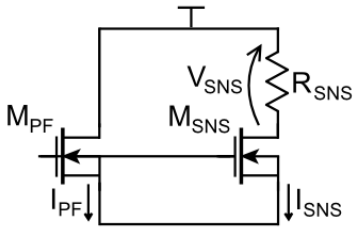

Fig. 5. Sense-FET and sense-resistor approach

To minimize sensing dependence on PVT spread, Fig. 6 displays a compact and accurate differential-mode sense-FET current sensor for linear regulators [5]. A NMOS pass transistor M_{PF} delivers a current I_{PF} to the load. The sensor comprises a couple of matched sense transistors M_{SNS}^{+} and M_{SNS}^{-}, in series with asymmetrical

sense resistors R_{SNS}-ΔR and R_{SNS}+ΔR. A differential voltage V_{SNS} across these resistors is converted into a current at the sensor output I_{OUT} by means of a transconductor with heavily-degenerated differential-pair, with $g_mR_E >> 1$ and R_E is the degeneration resistor. In this case, one has $V_{SNS} \cong 2I_{PF}\Delta R/M$, yielding

$$\frac{I_{OUT}}{I_{PF}} \cong \frac{2}{M}\frac{\Delta R}{R_E} \qquad (2)$$

Since I_{OUT}/I_{PF} relies only on a resistor-ratio and a geometrical scaling factor, its dependence on PT-variation is thus minimized.

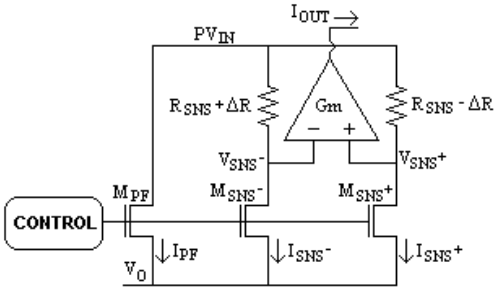

Fig. 6. Differential sense-FET, sense-resistor sensor

3. Limiter Design and Simulation Results

Accurate FLAG assertion, with low PT-spread, is mostly desirable in high-current rated converters. Large tolerances on I_{TH} demands equal safety margins in sizing power devices and bond wiring, as they must withstand the maximum current before entering limitation. Usually, the trimming of I_{TH} has been a feasible solution in industry to handle non-idealities and process variation. However, a broad change of I_{TH} with process and temperature (PT) demands a large number of trimming bits, and therefore more registers and/or fuse cells, which increases die size. In addition, production test time is stretched, further increasing overall costs.

3.1 Current Limiter with PT Compensation

A fast-response sense-FET sense-resistor current limiter with internal compensation for PT spread is illustrated in Figure 7 [6]. A relationship between I_{SO} and I_{TH} is fixed through R_{SNS}. Since both M_{PF} and M_{SNS} operate in deep triode region in low-dropout (LDO) linear regulators and high-efficiency switchers, the precision on I_{PF}/I_{SNS} ratio is impacted by the offset in drain-source voltages caused by a finite sense voltage V_{SNS}. Whenever feasible, making $R_{SNS} << R_{DSON\_SNS}$, where R_{DSON_SNS} is the on-resistance of M_{SNS}, helps mitigating the dependence of I_{TH} on dropout.

V_{SNS} is converted into a current I_{SO} by a simple transconductor G_M that corresponds to either a single depletion-mode (DM) p-MOSFET or a level-shifter followed by common-source enhancement-mode (EM) p-MOSFET. While the latter is fully compatible with standard integration processes, the former is restricted to fabrication processes featuring such a sort of device, although several design techniques relying on DM P-MOSFETs have been reported [e.g., 7-8]. For the sake of conciseness, only the transconductor based on EM devices is herein considered, as shown Fig. 8.

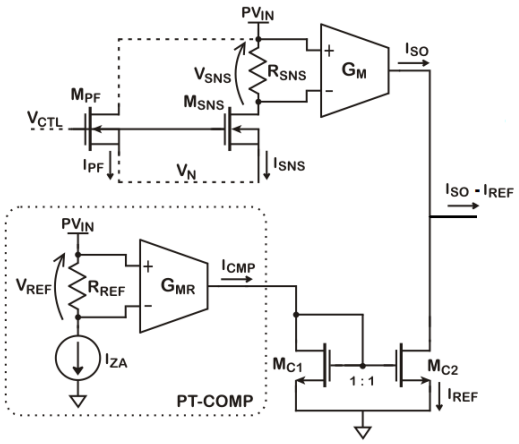

Fig.7. Current limiter with PT compensation

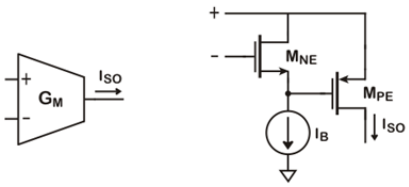

Fig.8. Transconductor with EM devices

Denoting M as the scaling factor between M_{PF} and M_{SNS}, at current limitation threshold,

$$I_{SNS} = \alpha\frac{I_{TH}}{M} \qquad (3)$$

where correction factor α in current mirroring is

$$\alpha = \frac{PV_{IN} - V_N}{PV_{IN} - V_N + \frac{I_{TH}}{M}R_{SNS}} \qquad (4)$$

PT cancellation scheme is now explained in detail. Elements in transconductor G_{MR} are denoted by subscripts *RNE* and *RPE*, respectively for M_{RNE} and M_{RPE}, while those in sensor by *NE* and *PE*, respectively for M_{NE} and M_{PE}. The variation ΔI_S superimposed to I_{SO} due to PT-spread, as well as tolerance on I_B value, is described as

$$\Delta I_{SO} = R_{SNS}\left(\frac{\partial I_{SO}}{\partial R_{SNS}}\right) + V_{TH\_NE}\left(\frac{\partial I_{SO}}{\partial V_{TH\_NE}}\right) + I_B\left(\frac{\partial I_{SO}}{\partial I_B}\right) + V_{TH\_PE}\left(\frac{\partial I_{SO}}{\partial V_{TH\_PE}}\right) \quad (5)$$

whereas the deviation ΔI_{REF} associated with I_{REF}, due to similar effect, corresponds to

$$\Delta I_{REF} = R_{REF}\left(\frac{\partial I_{REF}}{\partial R_{REF}}\right) + V_{TH\_RNE}\left(\frac{\partial I_{REF}}{\partial V_{TH\_RNE}}\right) + I_B\left(\frac{\partial I_{REF}}{\partial I_B}\right) + V_{TH\_RPE}\left(\frac{\partial I_{REF}}{\partial V_{TH\_RPE}}\right) \quad (6)$$

with

$$I_{REF} = \frac{\beta_{RPE}}{2}\left(R_{REF}I_{ZA} + \sqrt{\frac{2I_B}{\beta_{RNE}}} + V_{TH\_RNE} - \left|V_{TH\_RPE}\right|\right)^2 \quad (7)$$

At current limitation onset, one has $V_{SNS} = V_{REF}$ and $\Delta I_{SO} = \Delta I_{REF}$. Considering $[M_{NE}, M_{RNE}]$ and $[M_{PE}, M_{RPE}]$ pair-wise matched and imposing $\Delta I_{SO} = \Delta I_{REF}$, manipulation of (5) - (7) implies that first-order PT-cancellation on I_{TH} is ensured by

$$\frac{R_{REF}}{R_{SNS}} = \frac{\alpha}{M}\frac{I_{TH}}{I_{ZA}} \quad (8)$$

Supposing ideal matching, Fig. 9 displays simulated waveforms of a linear regulator as a stand-alone block using this scheme, i.e., without a disabling signal from system control after FLAG assertion. PV_{IN} = 1.5V and V_{OUT} = 1.25V were selected, compelling a low 250mV-dropout. As long as I_{LOAD} falls into its normal operation interval, the current limiter remains deactivated. Upon overcurrent, I_{LOAD} is then clamped to I_{TH} = 875mA.

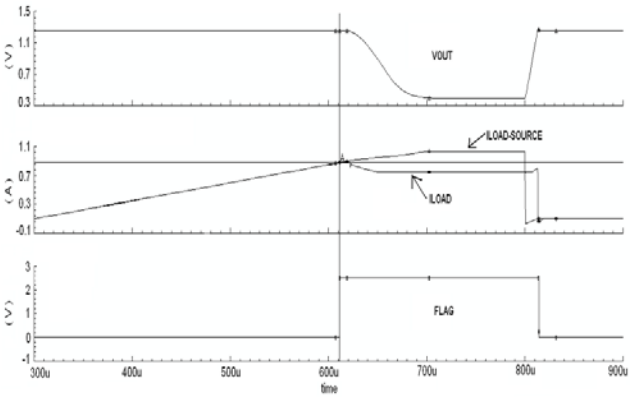

Fig. 9. Current limitation in linear regulator (low-dropout)

An alternative for robustness against PT-variation is the compact resistor-less current detector that protects linear regulators against overcurrent [6], as illustrated in Fig. 10. The circuit suits converters with either p- or n-channel pass-device, for different dropout voltages. The ratio between I_{TH} and a reference current I_{REF} depends only on transistor geometry scaling, making the current limiter robust against PT-variations.

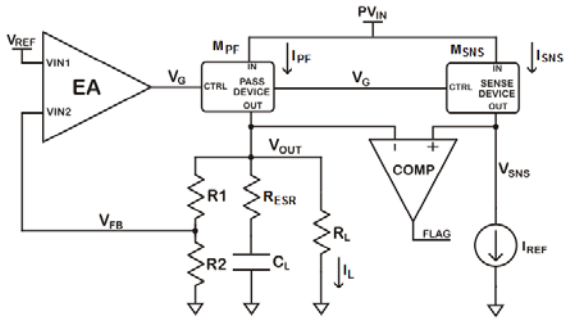

Fig. 10. Linear regulator with resistor-less OCP

The current detector consists of sense transistor M_{SNS}, ZTC current source I_{REF} and comparator COMP. Structurally identical to M_{PF}, M_{SNS} is paralleled with the latter, but has its aspect-ratio scaled down by a factor M, so that $(W/L)_{PF}/(W/L)_{SNS}$ = M. Nodes IN, CTRL and OUT, all common to M_{PF} and M_{SNS}, respectively correspond to source, gate and drain terminals for p-MOSFET regulator, whereas denoting drain, gate and source terminals for its n-type counterpart. Comparator positive and negative inputs are tied to sense voltage V_{SNS} and V_{OUT}, respectively.

During normal operation, one has $I_{PF} < I_{TH}$ and, as imposed by design, $V_{SNS} < V_{OUT}$. The current detector remains then deactivated, with output signal FLAG negated. Whenever I_{PF} exceeds I_{TH}, the condition $V_{SNS} \geq V_{OUT}$ asserts FLAG to signalize the system control for preventive action, such as turning the converter off as long as the fault persists. The operation of current limiter is now described for both PMOS and NMOS regulators.
ZTC bias circuit that generates I_{REF} is an elementary opamp-based V/I converter that drives a common-drain transistor with source connected to a resistive ladder built up with resistors of complementary temperature coefficients. Input reference voltage V_{REF} is tapped off a bandgap circuit. Current mirrors provide all necessary references to other blocks. The comparator consists of a differential-pair amplifier with diode-connected loads and a couple of digital inverters. To cope with noisy V_{OUT} and V_{SNS}, hysteresis is added to the input stage through local positive feedback [9].

Let´s assume a p-MOSFET linear regulator operating initially at low dropout, with both M_{PF} and M_{SNS} operating in triode region, it turns out

$$I_{PF} = \beta_{PF}\left(PV_{IN} - V_G - \left|V_{THP}\right| - \frac{PV_{IN} - V_{OUT}}{2}\right)(PV_{IN} - V_{OUT}) \quad (9)$$

$$I_{REF} = \beta_{SNS}\left(PV_{IN} - V_G - \left|V_{THP}\right| - \frac{PV_{IN} - V_{SNS}}{2}\right)(PV_{IN} - V_{SNS}) \quad (10)$$

where $\beta = (W/L)\mu C_{ox}$. At current detection onset, i.e. $I_{PF} = I_{TH}$, Working out (9) and (10) yields

$$I_{REF} = \beta_{SNS}\left(\frac{I_{TH}}{\beta_{PF}(PV_{IN} - V_{OUT})} - \frac{V_{OUT} - V_{SNS}}{2}\right)(PV_{IN} - V_{SNS}) \quad (11)$$

so that design condition for $V_{SNS} = V_{OUT}$ is obtained by

$$I_{REF} = I_{TH}\frac{\left(\frac{W}{L}\right)_{SNS}}{\left(\frac{W}{L}\right)_{PF}} = \frac{I_{TH}}{M} \quad (12)$$

At large dropouts, when M_{PF} and M_{SNS} are saturated, V_{SNS} can possibly be determined only by action of channel-modulation, or λ-effect. It can be demonstrated that (12) also applies to this case.

Waveforms of current detection and FLAG generation are displayed in Fig. 11, for low dropout V_{DRP} = 250mV and distinct temperatures of -40° and 150°. Imposing a load transient-rate of 100mA/ms, I_{TH} data are [79.3mA @-40°C, 81.9mA@150°C] and [84.1mA @-40°C, 85.8mA@150°C] for p- and n-type regulators, respectively. For a large-dropout scenario of V_{DRP} = 1.5V, similar analysis yields I_{TH} values of [84.1mA @-40°, 85.8mA@150°] for p-MOSFET regulator. In case of short-circuit between OUT and GND, FLAG is asserted within 28ns.

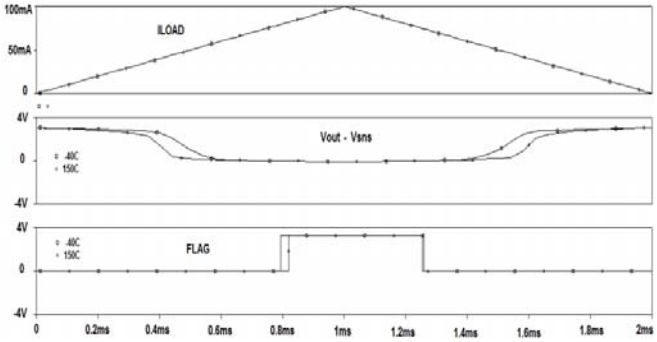

Fig. 11. Current detection for p-type linear regulator

Monte Carlo analysis reveals a maximum standard deviation (σ) of only 1.89mA for I_{TH}, which attests the low susceptibility of the current detector to PT-spread and mismatching. Such accuracy makes the resistor-less current limiter attractive for power-management chips demanding excellent control of power dissipation upon overload condition. Furthermore, trimming of I_{TH} may no longer be required, which is highly advisable for low-cost applications.

4. Experimental Results

Experimental results of the fast-response sense-FET sense-resistor current limiter with PT compensation are displayed in Fig. 12, at low dropout (PV_{IN}=1.5V, V_{OUT}=1.25V) and for distinct temperatures. Load current I_{LOAD} is mirrored from an external pulsed current source, which ramps from 0 up to 1A. The output voltage is under regulation within the normal operation from 0 to 400mA, when the limiter remains deactivated. For ambient temperatures of -40°C, 27°C and 150°C, clamping occurs at 934mA, 867mA and 776mA, respectively. Upon FLAG assertion, central control is signalized and the regulator turned off.

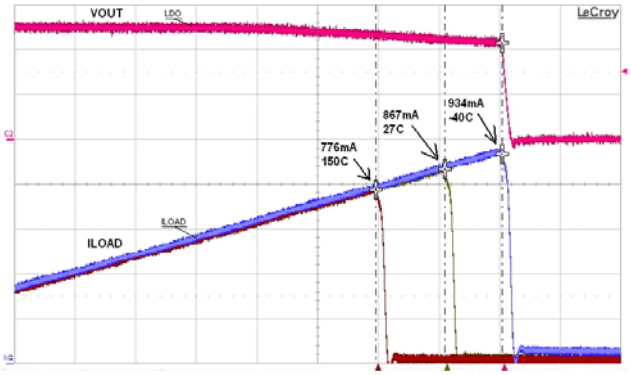

Fig. 12. Measured current limiter waveforms

Data collected from parts of different fabrication lots are statistically represented in the histogram of Fig. 13. Boundaries of I_{TH} are well inside +/- 30% of its nominal value, as predicted from process and temperature corner simulations.

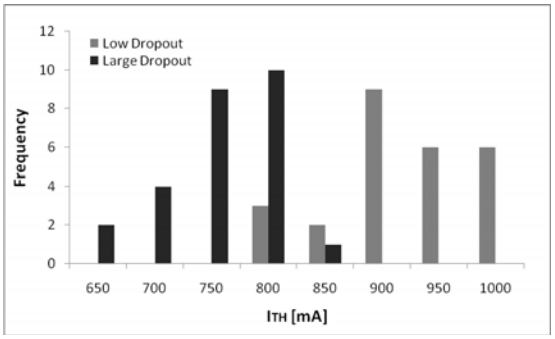

Fig. 14. Experimental I_{TH} histogram in a linear regulator

The performance of the current limiter was also validated in case of faulty short-circuit between V_{OUT} and P_{GND}. As displayed in Fig. 15, V_{OUT} starts to decrease to 0V after the fault, with I_{LOAD} growing fast. After a delay of 2.3μs, I_{LOAD} clamps to nearly 800mA and FLAG asserted. Control logic reacts after 4μs, turning the regulator off. The under-damped oscillation observed on I_{LOAD} is similar to the simulated response to short-circuit. A higher current peaking was nonetheless observed and may be attributed to inductive and resistive stray components of PCB and cables used to provoke the failure. Additionally, the current was measured from PV_{IN} pin, with decoupling capacitors removed, leading to small oscillations due to load transient.

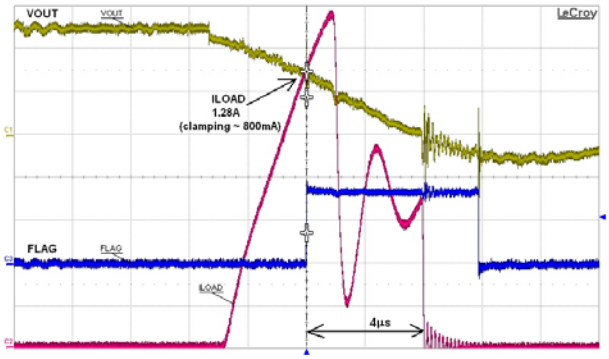

Fig. 15. Limiter response after short-circuit at output node

The limiter susceptibility to noise superimposed to PV_{IN} was also analyzed. Fig. 16 shows current clamping with a noise voltage of $42mV_{rms}$ coupled onto PV_{IN}. With respect to a noiseless PV_{IN} case of Fig. 17, a negligible deviation of only 4mA on I_{TH} was observed, attesting the robustness on I_{TH} against a noisy PV_{IN}.

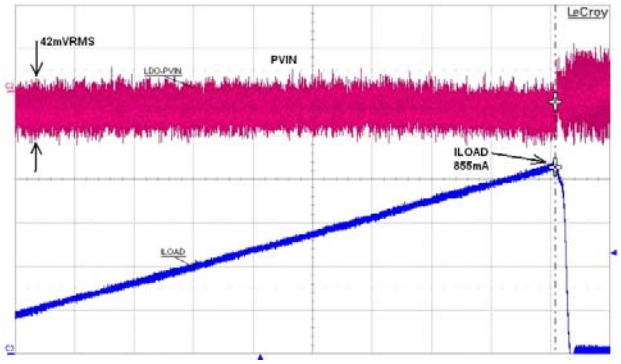

Fig. 16. Current limitation with noise coupled onto PV_{IN}

5. Conclusion

An overview of overcurrent current protection (OCP) techniques applied to both switching and linear regulators was presented and their trade-offs discussed. Basic current sensors commonly employed in DC/DC converters were also revisited.

Examples of current limiters with high immunity to manufacturing and temperature spread were presented, such as differential current sensing. A limiter with an internal reference generator that first-order compensates for PVT variation was also described. Simulation and experimental data attested the validity of the current limiters, as well as the accuracy of the current threshold I_{TH}. Therefore, the need for post-fabrication trimming is significantly reduced, even discarded, leading to smaller layout area and shorter testing time, and consequently, lower costs.

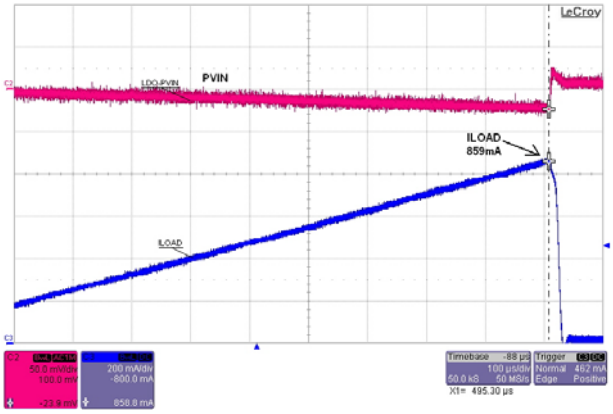

Fig. 17. Current limitation without noise coupled onto PV_{IN}

6. Acknowledgment

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7. References

[1] B. Mammano – "Current Sensing Solutions for Power Supply Designers", Unitrode SEM1200, 1999.
[2] Erickson, R. and Maksimovic, D., Fundamentals of Power Electronics, Kluwer Academic Publishers, 2001.
[3] R. Lenk - "Application bulletin AB-20 optimum current-sensing techniques in CPU converters," Fairchild Semiconductor, Application Notes, 1999.
[4] Y. Tsividis, Operation and Modeling of MOS Transistor, 2nd Edition, Oxford University Press, 1999.
[5] J. De Lima and W. Pimenta – "A Differential-Mode Current Sensor and Its Application to a LDO Regulator", IEEE Proc. of ISCAS, Taipei, May 2009.
[6] J. De Lima and W. Pimenta – "A Current Limiter for DC/DC Regulators with Internal Compensation Against Process and Temperature Variations", Analog Int. Circuits and Signal Proc., Vol. 63, Issue 2, 2010.
[7] M. Ugajin and T. Tsukahara – "A 0.6-V Reference Voltage Circuit Based on Σ-V_{TH} Architecture in CMOS/SIMOX", pp. 141-142, 2001 Symposium on VLSI Circuits Digest of Technical Papers, 2001.
[8] S. Yoo and S. Kang – "New High-Performance Sub-1V Circuit Technique With Reduced Standby Current and Robust data Holding", IEEE Proc. of ISCAS, Vol. IV, pp. 65 – 68, May 2000.
[9] R. Gregorian – "Introduction to CMOS OP-AMPS and Comparator", John Wiley and Sons, 1999.