A Virtually Isolated Transformerless Off Line Power Supply

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Abstract - This paper describes a new method of isolation between a.c. mains and d.c. voltage output without the use of a transformer. It consists of two buck converters, connected in series, each one using a pair of two MOSFET transistors. Each pair of transistors is conducting at different time intervals, thus under the assumption that the impedance of an OFF state MOSFET is practically infinite, there is transfer of energy from the a.c side to the d.c. side without actual ohmic continuation in the circuit. If the maximum limit of the drain to source voltage is not exceeded, the power supply becomes virtually isolated, making redundant the transformer used in classic power supplies. This configuration is suitable for output powers above 50Watts. The proposed circuit is analysed and simulated results are derived.

Key-Words: buck converter, power supply, transformer, voltage isolation, transformeless isolation, high efficiency power supply

1 Introduction

Traditionally, the isolation of a power supply is achieved by using a transformer. This paper describes an off line dc power supply which makes the large impedance of OFF state transistor MOSFETs equal the impedance between the A.C. and D.C side. The circuit consists of two buck converters, connected in series, each one using a pair of two MOSFET transistors, as shown in Fig.1. The necessity of using four transistors, makes this configuration attractive for output powers above 50Watts.

Fig. 1 shows the basic principle of operation for this circuit. Tr1, Tr2, L5, D8, C3 form one buck converter [1],[2], while Tr3, Tr4, L8, D13, C4, form the second one. There are four repeated modes in steady state operation.

MODE I
Tr1 and Tr2 are closed with Tr3, Tr4 opened. Capacitor C3 is charged through Tr1 and Tr2.

MODE II
Tr1 and Tr2 are opened with Tr3, Tr4 opened. Current freewheels through L5, D8, C3, keeping the voltage variation of C3 at low levels.

MODE III
Tr1 and Tr2 are opened with Tr3, Tr4 closed. Capacitor C4 is charged through the discharging of capacitor C3 and through the energy stored in L5.

MODE IV
Tr1 and Tr2 are opened with Tr3, Tr4 opened. Current freewheels through D13 and L8 keeping the load voltage variation at low levels.

2 Circuit design and operation

The purpose of this design is to demonstrate the isolating principle of operation and not the production of an optimized power supply where all factors such as efficiency, optimized control, soft starting, current limiting and suitably optimized values of components are taken into account.
The theoretical design was in the Orcad environment, the requirement being a supply fed from the mains with $230 \pm 10\%$ V RMS / 50Hz giving an output of 14V/14A/196W.

Apart from the standardized ORCAD components such as the MOSFETs used (IRFP360), diodes (MUR1560), the PWM control integrated circuit (SG1525A/25C) and the bipolar transistors (BC546A), assumed values of the resistive lossy component of the inductors and capacitors are taken into account, approaching practical values of laboratory components.

The general circuit layout is shown in Fig.1. With the actual circuit developed in ORCAD program not shown in this paper due to its complexity. Usual values of components are chosen as those used in ordinary power supplies. The use of the antiparallel diodes D5, D6, D9 was found necessary to minimize the voltage stress on the MOSFETs. Diodes D14, D15, D10, D11 were used to block reverse currents in diodes of MOSFETs though the earth loop and power supply.

2.1 PWM Control

The control method is based on the integrated circuit 1525A. The control circuit is shown in Fig.2. Here, the output B is used to produce the two pulses driving the two pairs of MOSFETs (Tr1 - Tr2 and Tr3 - Tr4). The first pulse drives directly the drive circuit of Tr3 and Tr4 and being modulated, produces the constant load voltage. The pulse driving the other pair of input MOSFETs has a constant maximum width occupying almost 50% of the period which the 1525A operates. This action ensures that the first buck converter always gives the maximum voltage irrespective of load conditions, with the second buck converter providing the control.

The antiphase nature of the pulses is achieved via the circuit shown in Fig.3. The pulse derived from output B is differentiated through $C_5$ and $R_9$. $R_{10}$ and $R_{11}$ bring the amplitude of this pulse at appropriate voltage levels, feeding the clear input of the counter 74HC193. This zeroes all outputs of the counter. The clocking of this counter is provided by the oscillator output of the 1525A circuit. The oscillator output is independent of the 1525A control circuit and always gives two pulses of short duration during one period, so that even if output B is zeroed due to current limiting or other reasons, the oscillator output will provide the inverter 74HC04 with a pulse. The inverter output is fed to the UP count of the counter, driving the output A of the counter high. Here, it must be noted that the clear input of the counter, needs only to be applied once, since odd number of pulses will drive output A of the counter high and even number of pulses will drive output low.

Fig. 4 shows waveforms in various parts of the antiphase circuit.

2.2 Transistor drive circuits

The requirement is to drive the MOSFETs through four isolated circuits, two for every MOSFET pair. The authors recommend the use of the integrated circuit HCPL316J. Two identical drive circuits were designed as the one shown in Fig. 5. Fig. 6 shows the waveforms of...
the pulses applied to the drive circuits and Gate to Source voltages of transistors Tr1 and Tr3.

![MOSFETs drive circuit](image)

**Fig. 5** MOSFETs drive circuit

![Pulse input to driver of Tr1, VGS of Tr1, Pulse input to driver of Tr3, VGS of Tr3](image)

**Fig. 6.** A: Pulse input to driver of Tr1  
B: VGS of Tr1  
C: Pulse input to driver of Tr3  
D: VGS of Tr3

### 2.3 Snubbers

The snubber used, is shown in Fig. 1 with components D8, D7, L4 and R5. Its use was necessary due to large spikes of current flowing through the MOSFETs during switch ON.

### 3 Simulation results

Repeated runs were made on the theoretical model with the most important parameters plotted in the following figures. Since the power supply must be operated with minimum mains voltage of 230-10%Volts, these figures were taken at this voltage, even though a separate waveform is taken with the mains voltage being 230+10%Volts showing the potential difference between Drain and Source of the most voltage stressed MOSFET. Fig. 7 shows the output voltage of the supply with an 1 Ohm load resistance the output power being 196 Watts.
Fig. 12 shows the voltages across point AB, CD and output voltage showing the function of each buck converter.

![Fig. 12. A: Voltage across points AB B: Voltage across points CD C: Output voltage V\textsubscript{out}(V)](image)

Fig. 13 shows the currents in Tr\textsubscript{3} and Tr\textsubscript{1}, with the currents in Tr\textsubscript{4} and Tr\textsubscript{2} being identical. The current through Tr\textsubscript{1} is somewhat higher than expected because the circuit operation has not reached the steady state. Rise times of currents show the effect of the snubber circuits.

![Fig. 13. A: Current in Tr\textsubscript{3} B: Current in Tr\textsubscript{1}](image)

Figs. 14 and 15 demonstrate the isolation principle of this power supply. Fig. 14 shows the current from the mains, to earth and output of the supply from starting to 100ms (current through R\textsubscript{E1}). Even though at steady state the current reaches peak values of ±3Amperes, if seen at higher time resolution, as in Fig.15, this current is constituted from short duration (100nsec) pulses associated with the capacitive nature between Drain and Source of MOSFETs during switching. The energy associated with these spikes is very small and easily filtered using commercial type filters associated with power electronic circuits. However, these spikes will not trip a leakage current relay even if remained unfiltered as the manufacturers of standard type leakage current relays have assured the authors.

![Fig. 14. Current through R\textsubscript{E1}](image)

![Fig. 15. Current through R\textsubscript{E1} at higher time resolution](image)

Fig. 16 shows the overall efficiency versus output power for 230-10% applied mains voltage with the output d.c. voltage being 14Volts. By making the mains voltage 230Volts, the output d.c. voltage was raised to 54Volts for possible applications of this circuit in telecommunication industry. As Fig. 17 shows, for an output power variation 50-400Watts, the efficiency is higher than 90%.

![Fig. 16. Efficiency versus load power for 14V d.c output.](image)

![Fig. 17. Efficiency versus load power for 14V d.c output.](image)
Fig. 17. Efficiency versus load power for 54V d.c output.

Fig. 18 shows the potential difference between Drain and Source of the most voltage stressed MOSFET (Tr1). The waveform was taken with the upper limit of the a.c. mains voltage being 230+10%. The voltage across it does not exceed 480 Volts. The circuit operated satisfactorily, thus fulfilling the requirement of operation in the range of mains voltage 230±10%

4 Considerations in practical applications

4.1 Protection

Personnel and equipment safety is ensured by earthing the output and connecting a classic blow fuse in the ac mains. Circuit malfunctioning due to simultaneous conduction of “primary” and “secondary” transistor or shorting of the transistor will blow this fuse. The leakage current relay of the installation provides additive security.

Transient mains overvoltages can be suppressed using voltage dependent resistors or other techniques.

4.2 Maximum output voltage

Due to the nature of buck converters, the maximum output voltage is limited to one quarter of the a.c. line rectified voltage. This is because simultaneous conduction of “primary” and “secondary” transistors is prohibited. The maximum conduction of the “primary” transistors is limited to a theoretical 50% of the PWM cycle while the “secondary” transistors conduct during the other half of the cycle. So, if we assume that the a.c. mains rectified voltage is 300V, the maximum theoretical output voltage is 75 Volts. Practically, assuming that the power supply has operating range of 230Vrms±10%, the PWM integrated circuit must have a dead time of at least one microsecond, allowing switching times of transistors, diodes and transistor drive circuits also assuming a switching operating frequency of 50kHz, the maximum output voltage is practically limited to about 55 Volts.

If higher voltages are required, for example in telecommunication applications, the authors propose the a.c. line rectification circuit shown in Fig. 19.

Fig. 19. Mains rectification circuit for higher output voltage applications

5 Conclusion

This paper describes a new method of isolation between a.c. mains and d.c. voltage output without the use of a transformer. The necessity of using four transistors, makes this configuration attractive for output powers above 50 Watts. As the power increases, the complexity of handling the magnetizing currents and leakage reactance energy of transformers used in rival half and full bridge converters makes this circuit more attractive. The proposed configuration has been presented and analysed. The results from simulation have confirmed the theoretical predictions.

References: