Double Gate Nanoscale MOSFET Modeling by a Neural Network Approach

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Abstract – The use of independently-driven nano-scale double gate (DG) MOSFETs for low-power analog circuits is emphasized and illustrated. In independent drive configuration, the top gate response of DG-MOSFETs can be altered by application of a control voltage on the bottom gate. This paper presents modeling of nanometer Double Gate (DG) MOSFET by a neural network approach. The principle of this approach is firstly introduced and its application in modeling DC and conductance characteristics of nano-DG MOSFET is demonstrated in details. It is shown that this approach does not need parameter extraction routine while its prediction of the transistor performance has a small relative error within 1% compared with measure data, thus its result is as accurate as that BSIM model.

Keywords— Double Gate MOSFET, Nanoscale CMOS, BSIM, Artificial Neural Networks,

I. INTRODUCTION

In low-power analog systems, current-mode signal processing has been usually considered an attractive strategy due to its potential for high-speed operation and low-voltage compatibility. These features can be especially rewarding in the context of mixed-signal system design in sub-100 nm CMOS era, where SOI substrates provide a viable platform for active and passive RF device integration while also hosting ultra-small CMOS devices for the digital system blocks. However, in most current mode circuits, the tuning of circuit response is achieved by use of extra transistors, leading to losses in area and performance. Following the ITRS prediction, the CMOS integrated circuit will soon approach 32nm technology generation in two or three years, and the compact model for such nanoscale DG MOSFETs is highly required for the device optimization and circuit analysis. The traditional device models such as BSIM and PICM models use the threshold voltage method to construct the compact model framework. Such a model approach, however, is generally believed to be outdated due to the regional characteristics, too many fitting parameter which lead to complex parameter extraction routine, thus requires a paradigm shift in the core model structure. In such a background, the advanced DG MOSFET model approaches such as surface potential based and charge-based become popular in compact modeling community in recent several years. These new developments will replaced the threshold voltage based model for us to be sued in the nanoscale DG MOSFET circuit simulation and analysis.

1.1 DEVICE STRUCTURE AND MODELING:

DG-MOSFETs considered in this work are chosen to facilitate the mixed-mode circuit design methodology, which seeks to integrate analog circuits on the same substrate as digital building blocks with minimal overhead to the fabrication sequence

(a)

(b)
Fig 1.1 (a,b). Structure of DG MOSFET, (c) symbol, (d) type of DG MOSFET.

Fig 1.2. Modes of operation (a) Cut off region. (b) Linear region (c) Saturation region

1.2 MODES OF OPERATION OF DG MOSFET:

There are three modes of operation. They are
1. Cut off region.
2. Linear region and
3. Saturation region.

1.2.1. CUT OFF REGION (VGS < VT):

In this region the transistor is turned off, since the applied Gate voltage is less than the Threshold voltage, and there is no conduction between drain and source.

1.2.2. LINEAR REGION (VGS > VT and VDS < (VGS - VT)):

The transistor is turned on, and a channel has been created which allows current to flow between the drain and the source. The MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages.

1.2.3. SATURATION REGION (VGS > VT AND VDS > (VGS - VT)):

The switch is turned on, and a channel has been created, which allows current to flow between the drain and source. Since the drain voltage is higher than the gate voltage, the electrons spread out, and conduction is not through a narrow channel but through a broader, two- or three-dimensional current distribution extending away from the interface and deeper in the substrate. The onset of this region is also known as pinch-off to indicate the lack of channel region near the drain. The drain current is now weakly dependent upon drain voltage and controlled primarily by the gate–source voltage.

The maximum ION/IOFF ratio optimized normally for minimum switching delay power product. It is also assumed that both gates have been optimized for symmetrical threshold VT = ±0.25 V using a dual metal process. In this paper, we forsake the traditional method and develop a neural network approach to modeling nanoscale DG MOSFET transistor. When comparing with the measured data, the accuracy of this approach is satisfactory for the compact modeling application because the relative error is within 1%. The paper is divided into four sections, the section one is a simple introduction, and in section two we give a description of the neural network principle and its algorithm—back propagation algorithm. In section three, we design a neural network to model the DC and conductance performance of different size DG MOSFET device. In section four we show the neural network method.
result compared with the measurement data and BSIM model. The final is the conclusion and acknowledgement.

2. NEURAL NETWORK PRINCIPLE

We first describe the neural network structure to better understand what neural network is and why it has the ability to model nanoscale MOS transistor performance. We start the neural network from the external input-output-point-of-view, and also from the internal neuron information processing point-of-view. The most popularly used neural network structure is the multiplayer perception (MLP) as shown in Fig.1.1. A typical neural network structure has two types of basic components, namely, the processing elements and interconnections between them. The processing elements are called neuron and the connections between the neurons are known as links or synapses.

Every link has a corresponding weight parameter associated with it. Each neuron receives stimulus from other neurons connected to it, processes the information, and produced an output. Neurons that receive stimuli from outside network are called input neurons, while neurons whose outputs are used externally are called output neurons. Neurons that receive stimuli from other neurons and whose outputs are stimuli for other neurons in the network are known as hidden neurons. Different neural network framework can be constructed by using different type and amount of neurons and by connecting them differently. The type and amount determine the network scale and the connecting algorithm determines network efficiency and accuracy.

2.1. BACK PROPAGATION ALGORITHM

we used a so-called back propagation algorithm, which may be suitable for the nanoscale device modeling. Some research results proven that MLP feed forward networks with arbitrary squashing functions can be approximated as a bore integral function from one finite dimensional space to another finite dimensional space. Fig.2 is a three-layer forward neural network, there are R neuron inputs, S1, S2, and S3 neurons in the first, second and third layer, respectively. The output of one layer becomes the input to the following layer; the equation that describes this operation is as follows:

\[ X_{K+1} = X_K - (J^T(X_K)J(X_K) + \mu K)^{-1} J^T(X_K) \]

Where the XK is the weights or bias matrix of the Kth epoch of network, J(XK) is the Jacobian matrix that contain first derivatives of the network errors with respect to the weights and biases, V(XK) is a vector of network errors. This algorithm has a very useful feature: As \( \mu K \) increases it approaches the steepest descent algorithm with small learning rate:

\[ X_{K+1} = X_K - \mu K^{-1} J^T(X_K) V(X_K) = X_K - (2X_K)^{-1} V(X_K) \]

While as \( \mu K \) decreases to zero the algorithm becomes Gauss-Newton algorithm:

\[ X_{K+1} \approx X_K - (J^T(X_K)J(X_K))^{-1} J^T(X_K) V(X_K) \]

The algorithm begins with being set to some small value. If a step does not yield a smaller value for F(X), then the step is repeated with multiplied by some factor \( \mu > 1 \), eventually F(X) should descent; otherwise \( \mu K \) is divided by \( \mu \) for the next step, so that the algorithm will approach Gauss-Newton which should provide faster convergence. The algorithm provides a good compromise between the speed of Newton’s method and the guaranteed convergence of steepest descent [1].

3. NEURAL NETWORK APPROACH TO MODELING NANOSCALE TRANSISTOR

Here, we select a three-layer forward network, the network has 6 inputs parameters: drain-source voltage (Vds), gate-source voltage (Vgs), bulk-source voltage (Vbs), length (L), width (W), and temperature (T).

The network has 16,8,1 neurons in the first, second and third layer and the corresponding transfer function f1, f2, and f3 is hyperbolic tangent sigmoid, log-sigmoid and linear function, the output is the drain-source current. This network can model the transistor DC and AC characterization of nanoscale DG MOSFETs.
Fig 2: Modeled 3D & Plane View (a) Conduction Band. (b) Device Doping Profile (c) Electron Density.

The device doping level and DC characteristics of DG MOSFETs. The 3D view and Plane view of conductance, device doping and Electron density is shown in Fig 2.

We firstly train the network with the measured data coming from 90nm CMOS production process. The training algorithm is the Levenberg-Marquardt algorithm, after epochs to 300, the output of the network compared with the measure data, has only the relative error within 1%, the corresponding result is show in Fig.3-4 and Fig.5-6.
4. RESULT COMPARISON BETWEEN THE NEURAL NETWORK METHOD AND BSIM MODEL

In order to validate the neural network method, we use the neural network method and BSIM model to fit the same measured data of the same nanoscale transistor. The results and the relative errors are shown in from Fig.7 to Fig.9. It is found that the relative error between the neural network method and the measured date is about 1% while the relative error between the BSIM model and the measured data is larger than 1% in most cases. So we can conclude that the neural network method is at least as accurate as BSIM model, and can be used to model nanoscale DG MOSFET transistor.

5. CONCLUSIONS

In this paper we present a neural network approach to modeling nanoscale DG MOSFET transistor performance. The MLP neural network application in modeling nanoscale DG MOSFETs is demonstrated in details via the training and work processing. It is shown that the neural network approach does not need extraction parameters while also having some other advantages: the characteristic curve can be differentiable from first order to infinite order in all transistor operation regions. Moreover, the used neural network method’s accuracy is tested and is further validated by compared with BSIM model.

REFERENCES:

[5] Min Fang, Jin He, Jian Zhang, Lining Zhang, Mansun Chan, and Chenyue Ma “Modeling Nanoscale DG MOSFETs By a Neural Network Approach” 978-1-4, 244-2540-2/08/$25.00 ©2008 IEEE.