S-Parameter Analysis of 0.18µm LNA for W-CDMA Application

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Abstract - This paper presents the design for Low Noise Amplifier (LNA) using Silterra 0.18µm technology and it based on W-CDMA standard application. The LNA function is to amplify extremely low noise signal without adding noise and also preserving required signal to noise ratio of the system at extremely low power level. Cadence design tool is used to optimize the simulation performance based on resistor and capacitor distributed. The used of power constrained method to provide an area-efficient architecture for effective design at Silterra 0.18µm CMOS technology. Result for S11 is 13.12dB and the frequencies are at 2.08GHz while S21 is observed to be -20dB and these values show that the resistance at the input of LNA is very close to 50Ω.

Index Term – Low Noise Amplifier (LNA), Power constrained, S-parameter.

I. INTRODUCTION

A. Low Noise Amplifier

Low Noise amplifier is normally used as amplification the signal receives at the antenna systems. The smallest possible signal can be received by the receivers defines sensitivity. The largest signals that can be received by the receiver establish an upper power level limit that can handle by the system while preserving voice or data quality. The objective of this project is to design an LNA with good noise and gain performances following the specifications set by the W-CDMA standard. It also to study a suitable topology for the LNA designs in a W-CDMA standard such as the inductively-degenerated cascode. Subsequently, detailed noise, gain and S-parameter analysis of the chosen topology will be performed from the small signal model incorporating the capacitances for high frequency analysis.

B. Scattering Parameter

S-parameters are mostly used for networks operating at radio frequency (RF) and microwave frequencies where signal power and energy considerations are more easily quantified than currents and voltages. S-parameters change with the measurement frequency so this must be included for any S-parameter measurements stated which is the characteristic impedance or system impedance [1].

This paper describes the operation and the simulation of s-parameter, gain and minimum noise figure using Silterra 0.18um CMOS technology.

II. LITERATURE REVIEW

A. Low Noise Amplifier Topology

Low Noise Amplifier (LNA) is the first block of any receiver system. Due to this fact, the LNA is considered as one of the important stage to be designed. Thus, it is very important for the LNA to be performing well in order to provide the following stage with good signals process [2]. The topology of low noise amplifier is shown in Figure 2.1.

![Figure 1: Topology of Low Noise Amplifier](image)

The detail methodology in designing LNA from the initial stage of understanding the application specification to determine the transistor size associated passives involved, on-chip matching circuitries, physical layout design, design analysis and the simulation result.
B. Noise

Nowadays, it is important to analogue designers to deal with the problem of noise because it trades with power dissipation, speed and linearity. Circuit noise is associated with the electrical components that build the subcomponents, such as resistor and transistor. The noise phenomena considered are caused by small current and voltage fluctuation that are generated within the device themselves [3].

C. Filter

A passive microwave filter is a circuit component consisting of lumped elements (inductors, capacitors and resistor) only or distributed elements or both arranged in particular configuration so that desired signal frequencies are allowed to pass with minimum possible attenuation while undesired frequencies are attenuated [4].

D. Analog Circuit Design Topology

Amplification is an important function in most analog circuit. The amplification process cause either signals from digital or analog is too small to drive load, overcome noise came from previous stage or bring logical level to digital circuit. Some aspects that must be take into account while designing amplifier and measure performance amplification process are power dissipation, supply voltage, linearity and noise [5].

III. METHODOLOGY

A. Schematic.

To design a schematic layout, the Design Architect (DA) is the software to use. It contains a standard cell library where tools been place and provide simulation after circuit been design. Meanwhile auto placing/ routing layout which is embedded with physical layout is available in the ‘ic library’. The technology to be used can be chosen here. Block of symbol should be created after the schematic design has been set up. This symbol is used to generate netlist to make sure the entire configuration in the schematic are correct. Schematic should be checked and saved first before the block of symbol is generated. Each input and output should be named in order for easy port reorganization.

B. Layout

The layout must pass a series of checks in a process known as verification. The two most common checks in the verification process are Design Rule Checking (DRC), and Layout Versus Schematic (LVS).

C. Design Rule Check (DRC), Layout vs Schematic (LVS).

Design rule are a series of parameters provided by semiconductor manufacturer that enable the designer to verify the correctness of mask set. Design rule are specific to a particular semiconductor manufacturing process where Silterra 0.18µm CMOS technology is used to perform this design. LVS is to ensure that the layout is correct realization of the intended circuit topology by comparing the layout and the Schematic.

D. Calculation of S-Parameter for Two-port Network

Figure 2: Schematic of the LNA

Figure 4: S-parameter for two-port network
Two-port network showing incident waves (a1, a2) and reflected waves (b1, b2) used in s-parameter definition.

The linear equations describing the two-port network are then:

\[ b_1 = S_{11} a_1 + S_{12} a_2 \]  \hspace{1cm} (1)

\[ b_2 = S_{21} a_1 + S_{22} a_2 \]  \hspace{1cm} (2)

The s-parameters S11, S22, S21, and S12 are:

\[ S_{11} = \frac{b_1}{a_1} |a_2 = 0 \]  \hspace{1cm} (3)

Input reflection coefficient with the output port terminated by a matched load \( Z_L = Z_0 \) sets \( a_2 = 0 \)

\[ S_{22} = \frac{b_2}{a_2} |a_1 = 0 \]  \hspace{1cm} (4)

Output reflection coefficient with the input terminated by a matched load \( Z_S = Z_0 \) sets \( V_s = 0 \)

\[ S_{21} = \frac{b_2}{a_2} |a_2 = 0 \]  \hspace{1cm} (5)

Forward transmission (insertion) gain with the output port terminated in a matched load

\[ S_{12} = \frac{b_1}{a_2} |a_1 = 0 \]  \hspace{1cm} (6)

Reverse transmission (insertion) gain with the input port terminated in a matched load.

IV. RESULT & DISCUSSION

All the schematic are simulated according to the design. The design parameters are the length and the width of MOS, the voltage \( V_{DD} \) and the architecture of the low noise amplifier. These design parameters are very important to produce the expected result. All data of the simulation results are analyzed. Discussions are made based on the results of the simulation.

The result from the simulation was quite consistent which at 4.12mA of current flowing through the LNA. The current flow the biasing is 143uA. The Fig.4.1 show the plots of the S11 and S21 obtained from the simulation analysis.

Figure 5: S-parameter simulation result of LNA

From the Fig. 5 displays the S-parameter plots obtained from the schematic analysis performed on the LNA. S11 is observed the simulated (13.12dB) and the frequencies are at 2.08GHz. Based on the comparison it can see this result can achieve for LNA design. For additional, the good reverse isolation was achieved for this design is the value of below the -25dB can be obtained throughout the W-CDMA reception band.

Based on that figure, S21 is observed to be -20dB and these values show that the resistance at the input of LNA is very close to 50Ω. However, the frequencies at which these optimum matching occur are at 2.10GHz, respectively from the targeted 2.14GHz the reason may be attributed to unaccounted parasitic capacitors.

Figure 6: Gain simulation result of LNA

From the Fig. 4.2, the gain of LNA was observed. Therefore, from the simulation available gain (GA) is drop at frequencies (2.1GHz) and the value is gain at that point is (25.67dB). It is approximate to the measurement (28dB) [3]. However, the frequencies at minimum Noise Figure (NFmin) are display at Fig. 4.3.
Refer to Fig. 4.3 above, the minimum noise figure (NF_{min}) is drop at -19.56dB and the frequencies are at 2.1GHz. For the good noise achievable for this design the value is not more than (-20dB) and also less than (2dB). The reason is the output port; one must match the input load.

VI. REFERENCES


