Design of a new intelligent CMOS controller chip for control water level in Tanks

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Abstract: In this paper, we present a new CMOS chip using fuzzy logic controller architecture to control the level of water in a tank. The flow of water (liquid) will be controlled with controllable valves. A motor controls the valve of the tank. The significant aim of this paper is to reduce both motor and input valve amortization and to increase their useful lifetime with presenting a simple and inexpensive controller for minimizing the movement of the motor valve, at the same time, setting the level of the tank at defined points. The controller is implemented by CMOS chip techniques in 0.35 um CMOS technology. The die size of the chip is 0.043 mm and power consumption is 8mw. The inference speed of the controller is about 4.05 MFLIPS.

Keywords: intelligent controller, CMOS chip, water level, FLC.

1. Introduction

The tank level is controlled by two conventional methods: on–off and PID. Simplicity and low cost are the advantages of on-off method but to keep the level at a constant point are difficult and also amortization of input valve or motor is another drawback. In the other method, exact setting of the level is an advantage of this method but it is complicated and expensive and valve amortization is high, too.

This paper proposes a new combined method to control the level of a tank. The method has almost all advantages of the other two methods. It sets the level of the tank at desired points constantly. Valve and motor amortization are minimized. Meanwhile it is simple and inexpensive. In this method, the rate of variation in output valve must be low, which is a restriction of this method.

The main parts of this controller are two fuzzy systems which implement a logarithm and an antilogarithm function. These fuzzy systems are constructed using product inference engine, triangular fuzzifier, center of gravity (COG) defuzzifier, and are implemented by current mode circuits. The controller is able to measure the level and output flow of a tank and then set the level at a desired point with only one movement of the input valve.

2. Algorithm of the proposed method

Fig. 2 block diagram of a controller used to set the level of a tank at a desired point (hset)
The level of a tank is measured by many bar sensors, inserted into its body (Fig. 1). And the water in it play the role of a switch. That is, when a sensor touches the water, a circuit containing that sensor will be closed; otherwise, it is open. The information obtained from sensors is converted into a 5-bit digital word to show the tank level (\(h\)). Another controller input is a 5-bit digital word regarding the desired set point (\(h_{\text{set}}\)). The output of the controller is a 5-bit digital word, too. This word is an input to a decoder. Each one of the 32 outputs of the decoder denotes one allowed point for positioning input valve (When output word is 00000, the valve is completely closed and when it is 11111, the valve is completely open and 30 words between 0 and 31 denote 30 positions between completely closed and completely open states).

4. Functional blocks

4.1. Time measuring block

To implement all steps need to control, a controller is needed which contains: fuzzy block, time measuring block, subtractor-adder block, some registers and multiplexers, and some control gates as shown in Fig. 2. A circuit should also be designed to change the information obtained from sensors into a digital data.

3. Extracting tank level as a 5-bit digital word

As mentioned in the previous sections, the level of liquid in the tank is measured by some bar sensors inserted into the tank. These bar sensors together with the circuit shown in Fig. 3, provide some information which can be used for extracting tank level as a digital word. The switch shown in Fig. 3 is constructed by a brass bar. If a sensor touches the water in the tank, this switch will be on, otherwise it will be off. The output of these circuits is either logical 1 or 0, depending on the water touching the corresponding bar sensor or not.

The information obtained from these circuits (Fig. 3) will enter into three 12-input and two 14-input OR gates. The output of these gates is a 5-bit digital word denoting the level of the tank.

Fig. 1 schematic of a tank and its control system

Fig. 4. Time measuring block

The different parts of time measuring block are illustrated in Fig. 4. When output valve changes from one position to another, a pulse named CV is generated and applied to the clock of flip-flop 1 (the width of this pulse must be at least 400ps and can be generated by a mono stable). Now, this block is ready to measure the output flow. As soon as the level passes from a sensor, flip-flop 2 receives a signal named Ch and counter starts to measure the time (since the clock is enabled now). When the level passes the next adjacent sensor, the counter will be disabled and measurement of the time stops. Finally, the data obtained by counting \(D_t\) is saved into a 5-bit register and FF1 is cleared by a circuit (gates in Fig. 4). The clock of the counter should be designed properly in order to measure all possible \(D_t\)'s by a 5-bit data.
4.2. Fuzzy block

Nowadays, fuzzy logic and fuzzy systems are getting increasingly popular in a wide range, such as theoretical and experimental sciences and industrial applications. In theoretical fields, many applications such as theory of possibility [12], decision analysis, image processing and pattern recognition [5,7], biological process [3], computing with words (CW), and so on, have been reported and their use has been demonstrated. (Equ. 7)

In industrial systems, fuzzy control is the most important application of fuzzy logic and fuzzy systems. In this area, many successful applications have been reported. For instance, power systems and nuclear reactor control [2,11], control of solar power plant, control of ABS braking system, elevator control [6], motor control [8], aircraft flight control [14], robot control [13], and speed control.

Fuzzy systems are based on knowledge or rules. The heart of a fuzzy system is a knowledge base that is configured by fuzzy if-then rules, and a fuzzy if-then rule is a conditional expression that is demonstrated by many, continues membership functions. The start point of designing a fuzzy system is to obtain a set of if-then rules from expert knowledge or the knowledge of the inspected field. The next step is to combine these rules to generate a unit system. Various fuzzy systems use different methods for combining the rules.

The significant motivation of selecting fuzzy technique for this project is the role of fuzzy systems as nonlinear mapping. That is, fuzzy systems are general approximators; therefore, we can approximate every nonlinear function with an arbitrary accuracy if enough fuzzy sets are defined in the domain of variables.

Since, domain of variables is rather large in this project (the input variables, \( q_i, \), \( At \), \( hset \), \( h \), can accept integer numbers between 1 and 31), and regarding the type of the function \( w = \frac{1}{x^2}y^{1/z} \), to obtain a good approximation by fuzzy systems, it is necessary to define many fuzzy sets for each input. For example, at least, 10 fuzzy sets are needed to define each one of them. Since the function is a 3-input variable function it is necessary to have at least 1000 rules to obtain complete combinations of rules. To solve this problem, a shortcut method is used to evaluate the function. That is, instead of direct evaluation of \( w \) function, the logarithm of each independent variable is calculated first and then, the logarithm of overall function (log(\( w \))) is obtained by Eq. (7). Using Eq. (8), \( w \) function can be found.

\[
w = \text{Anti log}(\log_2(\omega)) = 2\log_2(w).
\]

Thus for evaluating \( w \) function, it is sufficient to approximate a logarithm and an antilogarithm function by fuzzy sets and then use Eqs. (1) and (2) to calculate the final result. Since logarithm and antilogarithm functions are single variable functions, the fuzzy system can be simplified. For example, we only need a few rules and do not need any min–max functions to combine the rules. If fuzzy sets with 50% overlapping are used, the defuzzifier section will be considerably simple and this section can be realized with a simple sum.

The internal parts of a fuzzy block are shown in Fig. 5. Fuzzy systems that approximate logarithm and antilogarithm functions have been constructed by product inference engine, triangular fuzzifiers, and COG defuzzifier, and implemented by current mode circuits. Because of the difficulty in implementing the sum function in voltage mode, current mode approach is superior.

The block shown in Fig. 5 contains a digital-to-analog converter (D/A),
Both logarithm and antilogarithm sections are one-variable functions. Implementation of these functions with fuzzy systems is desired. At first, fuzzy sets and membership functions for input and output variables are needed. The number and shape of fuzzy sets are important to reach a desired approximation. Fuzzy toolbox in Matlab software helps us to determine fuzzy sets to obtain appropriate approximation.

Basic building cell of MFC is shown in Fig. 6. This circuit is the same as the one reported in [9,10], with a few modifications to generate two different slopes in one triangular membership function. When ascending slope is generated, M11 switch is on and M12 switch is off and the slope m, is obtained by M7-M10 transistors. For descending slope, M12 switch is on and M11 is off and the slope m’ is built by M7, M8, M13, and M14 transistors. With this structure, it is possible to generate every triangular (or with slightly change, trapezoidal) membership function, with any desired slope for m and m’. X and Y invertors are used to control M11 and M12 switches. Since, the threshold voltage (Vt) of a transistor changes with the rate of (W/L), in order to have exact rate for slopes, the output transistors of current mirrors are repeated in parallel. This structure is shown in Fig. 7.

4.2.1. Design of membership functions

In order to decrease the size of the hardware, only one fuzzy system is used to evaluate three logarithm functions. Each input variable is entered into this part and the output is saved in a current copier (it is an analog memory), then regarding Eq. (7), the currents stored in three copiers are combined and the result enters into the antilogarithm section for evaluating w function in analog format.

Afterwards, the analog data is converted into a 5-bit digital data by an A/D and exits the fuzzy block.

Fig. 6. Membership function circuit

4.2.1. Design of membership functions
defuzzifier is employed. Since these systems are one-variable functions and membership functions with 50% overlapping in input variables are applied, it is necessary to use only a sum at the output of current mirrors (Eq. (9)) for defuzzification with COG method.

In order to approximate these functions by means of fuzzy systems, 13 MFCs in logarithm and 14 in antilogarithm sections are designed. Figs. 8 and 9, show membership functions generated by MFCs for logarithm and antilogarithm sections, respectively. The range of input currents for log-part is from 1 to 31 $\mu$A and for antilog-part is from 0 to about 25 $\mu$A.

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Fig. 8. MF for logarithm

Fig. 9. MF for antilogarithm.

Fig. 10 presents the absolute error for approximating the logarithm function by fuzzy system. Since the ratio of maximum error (275 nA) to maximum range of output current (25 $\mu$A) is less than $\frac{1}{2}$, 5-bits resolution in calculating antilogarithm function (600nA/40 $\mu$A = 0.015 < 32).

4.2.2. Current copier circuit

As mentioned in previous sections in order to decrease the size of the hardware, only one fuzzy system is used to evaluate three logarithm functions. Instead, three current copier cells have been employed for saving current obtained from logarithm part of each of the three inputs. In contrast to current mirrors, the current copier technique does not require matching of transistors for its operation [4]. The circuit requires a non critical MOS transistor, non critical capacitor and switches.

In a practical current copier cell, the effect of channel length modulation, charge feed through from switches, and parasitic capacitive coupling from drain to gate of the transistor, must be addressed.

To eliminate this effect an op-amp is used as shown in Fig. 12. To copy and save a current, first, $a$ and $b$ switches are on and $c$ is off, therefore, capacitor $C$ charges by the op-amp with a gain of 24. Therefore, the current of the two branches and the voltages of nodes 3 and 6 are equal. To connect $M5$ to the load and copy current to load branch, first switch $a$ and then switch $b$ will be off and switch $c$ will be on. The Fig.

Fig. 12. Op-amp based current copier.

Fig. 13. Simulation results of current copier circuit.
does not change.

Fig. 13 shows a simulation of current copier operation. The range of input current for current copiers is from 3.5 to 25 μA. Maximum error in copying the currents is about 1.4%.

4.2.3. Data converter and timing block

A digital-to-analog converter is employed in fuzzy block to convert 5-bit digital words into an analog signal. This D/A converts a 5-bit digital word into an analog signal in range of 1–31 μA. A conventional structure is used for this purpose. An algorithmic A/D converter has also been selected to convert analog data exited from antilogarithm part into a 5-bit digital word. The current comparator proposed in Fig. 15 the simulation results of timing block [1] is used. The range of input current is from 0 to 20 μA. In this range A/D works in its linear operation.

The timing block is responsible for generating control signals to the fuzzy block (multiplexer, switches of copiers), and clock of Registers 1 and 2. Internal parts of this block are shown in Fig. 14.

It contains D flip-flops, NAND and AND gates, delay circuits, and an oscillator. The oscillator, named Ken Martin oscillator, which is enabled by a pulse signal (this pulse is generated when output valve or set point changes), generates a clock pulse with a period of about 130 ns. This clock is responsible to generate the other timing signals. The delay circuit makes a delay in descending edge of ax, ay, and az signals in order to generate bx, by, and bz signals in Fig. 14.

Fig. 15 shows the simulation results of timing block; this block is responsible for generating pulses required in fuzzy block and clock of Registers 1 and 2. Timing block starts its operation after receiving a pulse signal (this pulse is generated if output valve or set point changes). At first, oscillator generates a clock pulse with a period of about 130 ns, then this clock generates other pulses. Signals ai, bi, and ci, are control signals of each current copier and signals S0 and S1 are control signals of fuzzy block multiplexer. Thus, depending on S0 and S1 signals, three digital words enter into logarithm section and necessary calculations are saved in the corresponding current copier. After ending all necessary calculations, and obtaining a 5-bit digital word that designates the input flow, the clock of Register 1 will be generated. This clock will save the obtained input flow into Register 1. Total time, from starting the pulse to registering the evaluated input flow, is about 1 us. Then, the oscillator will be disabled and prepared to receive another initiating pulse.

The total fuzzy block is simulated with different signals and data, and its operation is tested. At first, the operation of this block was tested for making various functions.

The ratio of maximum error (800 nA) to maximum range of output current (40 μA) is less than \( \frac{1}{32} \), therefore there will be 5-bits resolution in calculating this function (800nA/40 μA = 0.02 < 32).

Fig. 18. typical output of fuzzy block for function (32/x(root 6))
This fuzzy block is tested with different digital data and digital outputs are obtained for each case. The results are completely satisfactory and show that the fuzzy block evaluates the desired function, that is, \( w = (\alpha /x)^{\beta /y}z \) in digital format accurately. Fig. 18 shows this issue for a typical input data. Output data are obtained after about 1 us. The layout of the controller using 0.35 um CMOS technology has been obtained and the die size is 0.043 mm².

5. Conclusions

In this paper, a new method is proposed to design an applicable specific fuzzy controller chip for controlling the level of a tank. For this purpose, first a relation for describing the system is obtained. This relation is completely non-linear.

Since fuzzy systems are non-linear mappings and general approximators, they are used to implement the obtained relations and design the controller. By employing this controller, if output flow or set point changes, the input valve will only move once to set the level at desired point, thus useful lifetime of motor and input valve will be optimum.

Fuzzy systems in this controller are constructed by product inference engine, triangular fuzzifiers, COG defuzzifier and implemented by current mode circuits. Simulation results are presented for 0.35 um CMOS technology. The die size of the chip is 0.043 mm², and power consumption is 8mw. The inference speed of the controller is about 4.05 MFLIPS.

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