Modeling and Performance Evaluation of Wide Bandgap Semiconductors Devices for High power Applications

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Abstract— Modeling of the drift region properties of 4H-Silicon Carbide (4H-SiC) and Gallium Nitride (GaN) based Schottky rectifiers and power Metal Oxide Semiconductor Field Effect Transistor (MOSFET) to achieve breakdown voltages ranging from 200 to 5000 V is presented. Schottky rectifiers rated at 1000 V and 3000 V are simulated and the characteristics of the 4H-SiC and GaN devices are compared with those of Si devices. The specific on-resistance $R_{on,s}$ of 4H-SiC and GaN MOSFET is at least two and three orders of magnitude smaller than the corresponding on-resistance for a Si device, respectively. 4H-SiC and GaN Schottky rectifiers rated for 5000V can deliver on-state current density of 100 A/cm$^2$ at room temperature with a forward drop of 1.72V and 1.29V, respectively because of very low drift region resistance. A thermal analysis, based on a junction temperature limit, as determined by packaging considerations, showed that 5000V GaN MOSFET and Schottky rectifier dies would be approximately 17 and 85 times smaller than corresponding Si devices. 4H-SiC MOSFET and Schottky rectifier rated for 5000V dies would be approximately 12 and 83 times smaller than the corresponding Si devices. This thermal analysis indicates that 4H-SiC and GaN devices would show correct operation at higher temperatures and higher breakdown voltages than the conventional Si devices.

Keywords: Gallium Nitride, power MOSFET, Schottky rectifiers, 4H-Silicon Carbide, specific on-resistance.

1 Introduction
Power electronic devices with high-temperature and high-power performance are becoming increasingly
important as the applications for which they are needed expand. Silicon, the conventional material for these devices, has begun to reach its physical limits for some applications such as pulse power for ships and aircraft, electronic circuits for power transmission and control in the electric utility systems, automotive electronics, and solid-state drivers for large electric motors. Table 1 compares some of the electrical and material properties of Si, 4H-SiC and GaN that are relevant in this regard. Gallium Nitride is a promising material for high-power, high frequency and high temperature applications due to its superior characteristics such as large saturated electron drift velocity, large breakdown electric field strength, small dielectric constant, and reasonably high electron mobility.

Recent developments in the growth of thin films of GaN by chemical vapor deposition have stimulated a renewed interest in GaN devices for a wide range of high temperature and high power device applications. Improvement in the quality of GaN epilayers on sapphire, Si and GaN substrates [1-4] have made fabrication of high-voltage GaN power devices a realistic possibility in near future. The doping of p- and n-type dopants [5] and the discovery of ohmic and Schottky contact materials [6, 7] have been reported. Study of the electrical properties, doped films, and their dependence on the temperature [8] and advancements in the characterization techniques of the CVD-grown GaN films [9] have made fabrication of high-voltage GaN power devices a realistic possibility. JFETs and MOSFETs built using GaN have been reported [10,11]. GaN Schottky rectifiers with reverse breakdown voltage in the range 450 -2500V have been reported [12, 13]. 4H-SiC Schottky barrier diodes with breakdown voltages up to 1000 V have been reported [14]. 4H-SiC MOSFETs with breakdown of 1.1KV have been reported [15, 16].

This paper provides an empirical formulation for the calculation of some of the electrical and thermal parameters for 4H-SiC and GaN devices. A theoretical analysis is carried out to compare the performance of power rectifiers and power MOSFETs made from 4H-SiC and GaN with those made from silicon. This provides a reasonable appraisal of the expected enhancement in the power handling capability of 4H-SiC and GaN devices over present day silicon devices.

Table 1
A comparison of some of the electrical and material properties of Si, 4H-SiC and GaN for power device applications at room temperature

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Si</th>
<th>4H-SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band gap $E_g$ (eV)</td>
<td>1.12</td>
<td>3.25</td>
<td>3.39</td>
</tr>
<tr>
<td>Critical electric field $E_c$ (MV/cm)</td>
<td>0.3</td>
<td>3.0</td>
<td>3.3</td>
</tr>
<tr>
<td>Electron mobility $\mu_e$ (cm²/V s)</td>
<td>1350</td>
<td>100 0</td>
<td>1000</td>
</tr>
<tr>
<td>Saturated electron drift velocity $V_d$ (10⁶ cm/s)</td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Relative dielectric constant $\varepsilon_r$</td>
<td>11.8</td>
<td>9.7</td>
<td>9.5</td>
</tr>
<tr>
<td>Thermal conductivity $\lambda$ (W/cm K)</td>
<td>1.3</td>
<td>4.9</td>
<td>2.3</td>
</tr>
<tr>
<td>BFOM$^*$ = $\varepsilon_\mu_nE_c^2$ (relative to Si)</td>
<td>1</td>
<td>608</td>
<td>794</td>
</tr>
<tr>
<td>JFOM$^*$ = $E_cV_d^2/4\pi$ (relative to Si)</td>
<td>1</td>
<td>400</td>
<td>1089</td>
</tr>
<tr>
<td>CFOM = $\lambda\varepsilon_\mu_nV_dE_c^2/\varepsilon_\mu_nV_dE_c^2$</td>
<td>1</td>
<td>397</td>
<td>383</td>
</tr>
</tbody>
</table>

$^*$BFOM: Baliga’s figure of merit, a measure indicating minimum conduction losses in power FET’s.

$^*$JFOM: Johnson’s figure of merit, a measure of the ultimate high frequency capability of the material.

$^*$ CFOM: Combined figure of merit for high temperature/high power/high frequency applications.

2 Power MOSFET

Power MOSFETs have several advantages over power bipolar transistors for high-frequency applications where switching power losses are dominant. MOSFETs have high input impedance, which makes the gate drive circuitry very simple. They exhibit excellent safe operating area and better output characteristics for paralleling. These characteristics of MOSFETs make them important candidates for many applications such as inverters and in switch-mode power supplies. However, these advantages are offset by the high on-resistance $R_{\text{on,sp}}$ associated with Si power MOSFETs for high breakdown voltages. Consequently, the use of Si power MOSFETs has been limited to breakdown voltages below 1000V.

The $R_{\text{on,sp}}$ of a Si double-diffused d MOSFET (DMOSFET) is determined as

$$R_{\text{on,sp}} = R_N + R_C + R_f + R_i + R_D + R_s \quad (1)$$

Where $R_N$ is the resistance from the N⁺-sources diffusion, $R_C$ is the channel resistance, $R_A$ is the accumulation layer resistance, $R_f$ is the resistance from the drift region between the P-base regions due to the
JFET pinchoff action, $R_D$ is the drift region resistance, and $R_S$ the substrate resistance. In a power MOSFET, the drift region supports the blocking voltage and thus, drift-region resistance is the minimum possible limit for $R_{on,sp}$. For an ideal DMOSFET, the resistances associated with the N’-source, the N-channel, the JFET, the accumulation region, and the N’-substrate are negligible, and only the drift region determines the specific on-resistance of the power MOSFET. This assumption is not accurate at low breakdown voltages where the drift-region resistance $R_D$ is comparable to the other resistive components. However, at higher breakdown voltages, $R_D$ is significantly higher than other resistances and $R_{on,sp}$ could be approximated by $R_D$.

We performed the drift region analysis for an ideal DMOS structure by approximating the depletion layer in the drift region as an abrupt one-dimensional junction fabricated in a uniformly doped semiconductor. The expressions for doping level $N_B$ (cm$^{-3}$) required to support a given breakdown voltage $V_B$ and depletion layer width $W$ (cm) at the breakdown for indirect bandgap semiconductor 4H-SiC and direct bandgap semiconductor GaN are as follows [17]:

\[
N_B = \frac{\varepsilon \varepsilon_C \varepsilon}{(2qV_B)} \quad (2)
\]

\[
W = 2V_B / \varepsilon_C \quad (3)
\]

The specific on-resistance ($\Omega \text{cm}^2$) associated with the drift layer to support $V_B$ for 4H-SiC and GaN is [18]:

\[
R_{on,sp} = \frac{8.725 \times 10^5 V_B^2 \varepsilon_C^{1.75}}{\mu_n \varepsilon} \quad (4)
\]

In general, both the mobility $\mu_n$ and the breakdown electric field $E_B$ are dependent on $N_B$. The dependence of $\mu_n$ for 4H-SiC and GaN on $N_B$ as used in this analysis is as follows [19]:

\[
\mu_n = \mu_n (T/300)\varepsilon + \mu_n (T/300)\varepsilon + \mu_n (T/300)\varepsilon N_C \quad (5)
\]

Table 2 lists the values of $\alpha_n$, $\beta_n$, $\gamma_n$, $\mu_{2n}$, $\mu_1n$, and $N_C$ for 4H-SiC and GaN.

In case of Si, the exact dependency of the electron mobility on $N_B$ is determined as [20]:

\[
\mu_n = (5.10 \times 10^{18} + 92N_B^{0.91}) / (3.75 \times 10^{18} + N_B^{0.91}) \quad (6)
\]

The doping concentration ($N_B$) and width ($W$) of the drift region scaled with the breakdown voltage are [17]:

\[
N_B = 2.01 \times 10^{18} V_B^{-4/5} \quad (7)
\]

### Table 2: Mobility parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>4H-SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\alpha_n$</td>
<td>-0.57</td>
<td>-0.7737</td>
</tr>
<tr>
<td>$\beta_n$</td>
<td>-2.7</td>
<td>-5.844</td>
</tr>
<tr>
<td>$\gamma_n$</td>
<td>2.55</td>
<td>6.109</td>
</tr>
<tr>
<td>Minimum electron mobility $\mu_{1n}$</td>
<td>88</td>
<td>55</td>
</tr>
</tbody>
</table>

\[
W = 2.58 \times 10^{5} V_B^{7/6} \quad (8)
\]

The specific on-resistance $R_{on,sp}$ of the drift region for Si is as follows [18]:

\[
R_{on,sp} = 3.35 \times 10^{-5} V_B^{2} \varepsilon C \mu_n \varepsilon \quad (9)
\]

Table 3 provides values of $N_{B}$, $W$, $\mu_{2n}$, and $R_{on,sp}$ of an ideal DMOS as a function of breakdown voltage for Si, 4H-SiC and GaN power MOSFETs. This analysis suggests that inspite of lower electron mobility, 4H-SiC and GaN MOSFETs have lower $R_{on,sp}$ due to their higher $E_C$. For a given breakdown voltage, $R_{on,sp}$ for the 4H-SiC and GaN MOSFET is at least two and three orders of magnitude smaller than for Si MOSFET, respectively. The ratio of $R_{on,sp}$ of the Si MOSFET to that of 4H-SiC MOSFET and the ratio of $R_{on,sp}$ of the Si MOSFET to that of GaN MOSFET increases with increasing breakdown voltage. However, this difference in the ideal specific on-resistances of these two devices is of greater importance at higher breakdown voltages because at lower voltages the component of the total resistance from the regions other than the drift region must also be included since they would be comparable at lower breakdown voltages.

### 3 Power Rectifiers

Power rectifiers are of interest in power electronic circuits at high frequencies because of their fast switching times. The high-frequency operation allows reduction in the size of passive components (capacitors and inductors) leading to a more compact and efficient system design. The Schottky rectifier is a unipolar device providing high-frequency rectification. The P-i-N rectifier is a bipolar device and exhibits large reverse recovery current and slow switching speed whereas the Schottky rectifier is a majority-carrier device not exhibiting any significant reverse recovery current. Here rectification occurs by means of nonlinear current transport across a metal-semiconductor interface. In the case of the Schottky rectifier fabricated on a semiconductor region with low doping levels, negligible current components are due to field emission, tunneling, and recombination. The only significant component of current is the thermionic emission current by means of electron transport over the potential barrier into the metal. For this case, thermionic emission theory describes the current flow across the Schottky barrier interface [21] as:

\[
W = 2.58 \times 10^{5} V_B^{7/6} \quad (8)
\]

The specific on-resistance $R_{on,sp}$ of the drift region for Si is as follows [18]:

\[
R_{on,sp} = 3.35 \times 10^{-5} V_B^{2} \varepsilon C \mu_n \varepsilon \quad (9)
\]
\[ J = J_s \left( e^{qV/kT} - 1 \right) \]  
\[ J_s = A^* T^2 \exp(-q \phi_{bhn} / kT) \]

Where \( T \) is the temperature, \( q \) is the electron charge, \( k \) is the Boltzmann’s constant, \( V \) is the applied voltage, and \( J_s \) is the saturation current of the Schottky rectifier.

After including the voltage drop associated with various resistive components, the total forward voltage drop \( V_F \) is [22]:

\[ V_F = (nkT/q) \ln(J / A^* T^2) + n\phi_{bhn} + R_{on,sp} J \]  

Where \( n \) is the diode ideality factor. The values of \( n \) for Si, 4H-SiC and GaN are 1, 1.2 and 1.13 respectively [21, 14, 23]. \( R_{on,sp} \) is the specific on-resistance of the rectifier and it includes contributions from the drift region, the substrate, and any contact resistances. At higher breakdown voltages, the resistance associated with contacts, and the substrate are relatively negligible, and \( R_{on,sp} \) may be approximated as the drift region resistance \( R_D \) only.

The value of \( \phi_{bhn} \) for Si, 4H-SiC and GaN were taken as 0.8, 1.15 and 1.19 eV, respectively [21, 14, 24]. In Figures 1 and 2, we compare the theoretical forward conduction characteristics of ideal Si, 4H-SiC and GaN Schottky rectifiers at room temperature for breakdown voltages of 1000 and 3000V, respectively. For these calculations, Richardson constant \( A^* \) chosen for Si, 4H-SiC and GaN are 110 A/cm²K² [25], 146 A/cm²K² [14] and 26.4 A/cm²K² [24], respectively, and the voltage drop contributions from the substrate and contacts were neglected. These figures clearly show the advantages of 4H-SiC and GaN rectifiers over the Si rectifier in terms of reduced voltage drop, increased current density, and reverse blocking capability.

Table 3 lists the calculated forward voltage drop \( V_F \) for a current density \( J \) of 100 A/cm² at room temperature for Si, 4H-SiC and GaN rectifiers as a function of \( V_B \). As is the case for MOSFETs, for a desired breakdown voltage, 4H-SiC and GaN Schottky rectifiers require higher drift region doping and smaller drift region thickness than for the silicon devices. This results in a decrease in its series resistance. Based on this analysis, it is expected that 4H-SiC and GaN Schottky rectifiers with breakdown voltage as high as 5000V can deliver 100A/cm² at room temperature with a forward voltage.
High power semiconductor devices, invariably, witness high junction temperature. Some of the desirable characteristics for power semiconductor devices are low on-state resistance, high input impedance, high switching speed, and large avalanche breakdown voltage. Additionally, for high-temperature operation of these devices, their thermal stability in terms of high-temperature performance and possibility of thermal runaway are very important considerations. The calculated results from the previous sections reveal that 4H-SiC and GaN have superior materials properties leading to high-performance 4H-SiC and GaN devices at room temperature for high-power, high-frequency electronic applications. To exploit the potential of 4H-SiC and GaN as materials of choice for power electronic applications, it is important to estimate the high-temperature performance capability of the 4H-SiC and GaN devices as compared to the Si devices. The Si-based power devices are limited in their operating capability to 200°C whereas 4H-SiC and GaN devices are capable of operating at temperatures as high as 600°C. 4H-SiC and GaN device has considerably higher on-state conductance and smaller off-state leakage current than a Si device at high operating temperatures. Consequently, the power dissipated in the active device area is less and thus, the GaN devices show desirable performance even at very-high junction temperature.

However, none of the research reported to date considered the performance of 4H-SiC and GaN devices under the conditions when the maximum allowable junction temperature T<sub>j</sub> is limited by criteria based on the existing packaging technology and does not exclusively depend on the semiconducting material properties. This approach to evaluate the high-temperature performance of 4H-SiC and GaN devices by considering the same T<sub>j</sub> for Si, 4H-SiC and GaN devices is of practical significance since the device packaging technology to accommodate high temperatures that are sustainable by 4H-SiC and GaN devices, is not currently available. Since Si devices are limited in their operation to temperatures below 200°C, it is worth making a comparison of the on-state current density J and the chip size of 4H-SiC and GaN MOSFETs with Si MOSFETs at the same maximum junction temperature T<sub>j</sub> of ~200°C.

Considering the heat transfer as solely due to conduction, the temperature rise in the active area of the device ∆T is [17]

$$\Delta T = \theta_{th} P_D$$

(13)

Where θ<sub>th</sub> (K/W) is the thermal resistance associated with the device and P<sub>D</sub> (W) is the total ohmic power generated. P<sub>D</sub> consists of ohmic power dissipated during the on-state P<sub>on</sub> and power dissipated during the off-state P<sub>off</sub>. For a 50% duty cycle, P<sub>0</sub> expressed for a MOSFET is

$$P_D = (J^2 R_{on,sp} + J_L A V_B) / 2$$

(14)

Where A is the area of the active device (cm<sup>2</sup>), J is the on-state current density (A/cm<sup>2</sup>), R<sub>on,sp</sub> is the specific on-resistance of the drift region (Ω cm<sup>2</sup>), J<sub>L</sub> is the leakage current density when the device is in its reverse blocking mode (A/cm<sup>2</sup>), and V<sub>B</sub> is the reverse blocking voltage (V). Si, 4H-SiC and GaN power devices with equal area A and equal junction temperature T<sub>j</sub> are compared in terms of J and the chip area. In general, the thermal resistance θ<sub>th</sub> between the active region and the ambient thermal reservoir consists of two components- θ<sub>jc</sub> that is the junction-to-case thermal resistance and θ<sub>ca</sub> that is the case-to-ambient thermal resistance. θ<sub>jc</sub> is relatively insensitive to the ambient environment and is mainly a function of chip material and geometry and is given by

$$\theta_{jc} = d / A$$

(15)

Table 4
Value of forward voltage drop at 100 A/cm<sup>2</sup> for ideal Si, 4H-SiC and GaN Schottky rectifiers at room temperatures as function of breakdown voltage

![Fig. 2 Forward conduction characteristics of an ideal Si, 4H-SiC and GaN Schottky rectifiers at room temperature with 3000 V breakdown voltage](image-url)
Where $d$ (cm) is the substrate thickness, $A$ (cm$^2$) is the junction area, and $\lambda$ (W/cm-K) is the thermal conductivity of the substrate which for Si, 4H-SiC and GaN decreases with temperature. However, an upper bound for $\theta_c$ at 200°C may be obtained by using the lowest value for $\lambda$ at 200°C. For Si, 4H-SiC and GaN, $\lambda$ at 200°C is 0.8, 2.2 and 1.37 W/cmK, respectively [25, 26, 27]. Assuming a chip area of 1 cm$^2$ and a 500µm thick substrate, maximum value of $\theta_c$ for Si, 4H-SiC and GaN substrates is ~0.06, 0.02 and 0.04 K/W, respectively. Thus for Si, 4H-SiC and GaN temperature coefficients of $\theta_{jc}$ are 1K/W, and the overall thermal resistance for Si is 1K/W. Thus, the overall thermal resistance for Si, 4H-SiC and GaN devices is about the same. The reverse leakage current density $J_l$ in power devices, which are based on the principles of p-n junctions, is given by (17) and has components due to the diffusion current $J_D$, the generation current $J_G$, and due to the space-charge generation current $J_G$ [21]

$$J_D = \frac{(q n_i W / \tau_e) + q (D_h / \tau_h) \sqrt{n_i^2} N_d}{N_d}$$ (17)

Where $n_i$ is the intrinsic carrier concentration (cm$^{-3}$), $W$ is the width of the space-charge region (cm), $\tau_e$ the lifetime of electrons in the space-charge region (s), $N_d$ is the concentration of donor atoms (cm$^{-3}$), $D_h$ is the diffusion constant of holes in the N-type region (cm$^2$/s), and $\tau_h$ is the lifetime of holes (s). The space–charge generation current is the first term; the second term corresponds to the diffusion current. Based on (17), it is obvious that due to the large bandgap of 4H-SiC and GaN, the intrinsic carrier concentration $n_i$ in 4H-SiC and GaN is very small and consequently, even at high operating temperatures, 4H-SiC and GaN has much smaller reverse-leakage current than Si. However, at 500K, $J_l$ even for a Si MOSFET device is very small and the amount of power dissipated in the off-state $P_{off}$ is negligible compared to the on-state power dissipation $P_{on}$. To make an objective comparison between the chip size and $J$ for Si, 4H-SiC and GaN MOSFETs, we have considered the expression for on-state current density is

$$J = \sqrt{400 \times \frac{P_{on}}{R_{on,sp}}}$$ (18)

Table 5 provides $R_{on,sp}$ and $J$ for Si, 4H-SiC and GaN MOSFETs based on this analysis for different values of breakdown voltage for a junction temperature of 500K. These $J$ values are the maximum allowable on-state
current densities for given junction temperature and rate of power conduction away from the active device area. Table 5 shows that for all the breakdown voltages, GaN MOSFET have higher J than Si and 4H-SiC devices and this difference become more significant as the breakdown voltage is increased. Figure 3 compares the forward conduction characteristics of a 1000V 4H-SiC and GaN Schottky rectifier with that of a Si Schottky rectifier at 500K. $J_{\text{GaN}}$ and $J_{\text{4H-SiC}}$ is seventeen fold and twelve fold the $J_{\text{Si}}$ MOSFET operating under the same conditions for a $V_B$ of 5000V. This improvement in the J of 4H-SiC and GaN over Si at higher breakdown voltages is due to lower $R_{\text{on,sp}}$ associated with the 4H-SiC and GaN devices as compared to Si devices. The improvement in the current-handling capability of 4H-SiC and GaN devices is especially significant for higher breakdown voltages. 

Table 5

<table>
<thead>
<tr>
<th>Breakdown Voltage $V_B$ (V)</th>
<th>$R_{\text{on,sp}}$ (10$^3$)</th>
<th>$R_{\text{on,sp}}$ (10$^3$)</th>
<th>$R_{\text{on,sp}}$ (10$^3$)</th>
<th>$J_{\text{GaN}}$</th>
<th>$J_{\text{4H-SiC}}$</th>
<th>$J_{\text{Si}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>0.07</td>
<td>0.13</td>
<td>0.01</td>
<td>11.95</td>
<td>8.77</td>
<td></td>
</tr>
<tr>
<td>1000</td>
<td>1.21</td>
<td>2.46</td>
<td>0.32</td>
<td>16.23</td>
<td>11.37</td>
<td></td>
</tr>
<tr>
<td>3000</td>
<td>10</td>
<td>20.64</td>
<td>2.85</td>
<td>16.94</td>
<td>11.78</td>
<td></td>
</tr>
<tr>
<td>5000</td>
<td>27.5</td>
<td>56.64</td>
<td>7.92</td>
<td>16.90</td>
<td>11.83</td>
<td></td>
</tr>
</tbody>
</table>

breakdown voltages. $R_{\text{on,sp}}$ has negligible contributions from the other resistive components of Figure 1 and its approximation by the drift region resistance $R_D$ in our analysis is valid.

Fig. 3 Forward conduction characteristics of an ideal Si, 4H-SiC and GaN Schottky rectifiers at 500K with 1000 V breakdown voltage

Unlike MOSFET, where the reverse-leakage current $J_L$ at 500K was negligible even for the Si devices, Schottky-barrier diodes can have an appreciably large value of $J_L$ at this temperature. For an ideal Schottky rectifier, $J_L$ is equal to the saturation current density $J_S$ and is given by (11). For the case of Schottky barrier diodes the maximum temperature generated in the device is given as

$$\Delta T = (J_F + J_L) A \theta_s / 2$$  \hspace{1cm} (19)

Where $V_F$ is the forward voltage drop (V) and $V_B$ is the reverse blocking voltage (V). Similar to the analysis for MOSFET, thermal analysis to calculate J and the relative chip size for Schottky rectifiers is based on the criteria of maximum allowable junction temperature $T_j$ as determined by the packaging. If we assume $T_j^{\text{max}}$ is 500K, $\theta_s$ is 1K/W, and a chip area of 1 cm$^2$, the maximum allowable J is obtained by solving the following equation:

$$J_F + J_L V_B = 400$$  \hspace{1cm} (20)

In equation (20) $V_F$ and J are nonlinerly coupled by (12). Table 6 includes the values of $P_{\text{off}}$, J and $V_F$ for
breakdown voltage can operate at a current density as large as 1.15eV and 1.19eV, respectively. Based on this value, Si, 4H-SiC and GaN Schottky rectifiers at 500K.

<table>
<thead>
<tr>
<th>Breakdown Voltage (V)</th>
<th>GaN</th>
<th>4H-SiC</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$P_{off}^{GaN}$ (W)</td>
<td>$J$ (A/cm$^2$)</td>
<td>$V_F$ (V)</td>
</tr>
<tr>
<td>200</td>
<td>0.001</td>
<td>494</td>
<td>0.81</td>
</tr>
<tr>
<td>1000</td>
<td>0.006</td>
<td>434</td>
<td>0.92</td>
</tr>
<tr>
<td>3000</td>
<td>0.021</td>
<td>222</td>
<td>1.8</td>
</tr>
<tr>
<td>5000</td>
<td>0.034</td>
<td>112</td>
<td>3.55</td>
</tr>
</tbody>
</table>

Si, 4H-SiC and GaN Schottky rectifiers at the junction temperature of 500K for different breakdown voltages. For low values of barrier height $\Phi_{Hb}$, $J_L$ and $P_{off}$ could be considerably larger than that for Si MOSFET. For high breakdown voltages, the GaN MOSFET has lower on-resistance, which is ~1000 times smaller than the on-resistance of corresponding Si MOSFET. This reduction in $R_{on,sp}$ of GaN power MOSFET coupled with high switching speed makes GaN MOSFET an attractive alternative for existing Si power devices, including GTO’s and thyristors. The doping levels and small thicknesses of the drift region for the GaN devices as predicted by our analysis indicate that achieving very high voltage operation is not beyond technology capability. The development of GaN Schottky rectifiers and power MOSFETs will provide devices that can deliver larger currents at very fast switching speeds in power circuits requiring high breakdown voltages. Based on thermal analysis it is possible to conclude that due to the much smaller value of off-state power loss for GaN devices as compared with Si devices, much higher on-state currents are possible in GaN devices for given junction temperatures and packaging. This would allow nearly 100x reduction in the chip size that should offset higher present day processing costs associated with the fabrication of GaN devices.

5 Conclusions
We have shown the on resistance of 4H-SiC and GaN MOSFET is at least two and three orders of magnitude smaller than that for Si MOSFET, respectively. Especially for high breakdown voltages, the GaN MOSFET has low specific on-resistance, which is ~1000 times smaller than the on-resistance of corresponding Si MOSFET. This reduction in $R_{on,sp}$ of GaN power MOSFET coupled with high switching speed makes GaN MOSFET an attractive alternative for existing Si power devices, including GTO’s and thyristors. The doping levels and small thicknesses of the drift region for the GaN devices as predicted by our analysis indicate that achieving very high voltage operation is not beyond technology capability. The development of GaN Schottky rectifiers and power MOSFETs will provide devices that can deliver larger currents at very fast switching speeds in power circuits requiring high breakdown voltages. Based on thermal analysis it is possible to conclude that due to the much smaller value of off-state power loss for GaN devices as compared with Si devices, much higher on-state currents are possible in GaN devices for given junction temperatures and packaging. This would allow nearly 100x reduction in the chip size that should offset higher present day processing costs associated with the fabrication of GaN devices.

This analysis suggests that GaN power rectifiers and MOSFETs could be superior alternatives for all Si power devices with breakdown voltage as high as 5000V. However, this would require further improvements in GaN device processing technology.

References:
[1] Hou-Guang Chen et al., Investigation on


