A SURVEY OF LOW POWER HIGH SPEED ONE BIT FULL ADDER

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Abstract: In this paper, a structured approach for analyzing the adder design is introduced. Analysis is based on some simulation parameter like No. of transistors, power, delay, power delay product, different technologies, aspect ratio. Each reference used different tool for the simulation purpose. The different circuit design are studied and evaluated extensively. Several designs give a different designing approach and give a new information which can relate with different application. Each of these circuits cell exhibits different power consumption, delay and area in different VLSI technology. This paper can be said as a library of different full adder circuits that will be beneficial for the circuit designers to pick the full adder cell that satisfied their specific application.

Key-Words: Addition, Arithmetic circuits, Delay, Full adder, Low Power, Novel XOR.

1 Introduction
The Explosive growth in laptop, portable system, and cellular networks has intensified the research efforts in low power microelectronics. Today we find number of portable applications requiring low power and high throughput circuits. Addition is one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such as application-specific DSP architectures and microprocessors. In addition to its main task, which is adding two binary numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, division, address calculation, etc. In most of these systems the adder is part of the critical path that determines the overall performance of the system. That is why enhancing the performance of the 1-bit full-adder cell (the building block of the binary adder) is a significant goal.

Recently, building low-power VLSI systems has emerged as highly in demand because of the fast growing technologies in mobile communication and computation. The battery technology doesn’t advance at the same rate as the microelectronics technology. There is a limited amount of power available for the mobile systems. So designers are faced with more constraints: high speed, high throughput, small silicon area, and at the same time, low-power consumption [1]. So building low-power, high-performance adder cells is of great interest. Designing systems aiming for low power is not a straightforward task, as it is involved in all the IC design stages beginning with the system behavioral description and ending with the fabrication and packaging processes. In some of these stages there are guidelines that are clear and there are steps to follow that reduce power consumption, such as decreasing the power-supply voltage. While in other stages there are no clear steps to follow, so statistical or probabilistic heuristic methods are used to estimate the power consumption of a given design [2], [3].

2 Classification Of Adder

2.1 Two CMOS Full Adder Based On Transmission Function
The full adder in this paper are two CMOS full adders (with and without the driving outputs) are designed by using the transmission function theory [5], as shown in fig.1a and 1b. Since these new operations can describe the physical action process.
of the CMOS transistor and the transmission function theory can guide the design of CMOS circuits at the switching level of MOS transistors, the algebraic difficulty that the high-impedance state cannot be expressed in Boolean algebra is overcome and the CMOS full adder with or without driving outputs needs only 22 CMOS transistors or 16 CMOS transistors, saving 4 CMOS transistors respectively in comparison with the two CMOS full adders designed in the conventional method.

2.2 Low Activity Factor Adder
The adder cell is a combination of XOR gate and TG [6]. It offers both low power and high speed performance. It compares three adder design CMOS Full adder (FA_c), Transmission gate adder (FA_t) and New adder (FA_New) (Fig.2).

FA_New is about 30% and 20% less area as compared with FA_c and FA_t, we can see that proposed cell FA_New has a minimal power dissipation compared to the other two cells because the signals entering the cell have a limited path to the ground. Same speed of FA_c But faster than FA_t, FA_New is superior in terms of delay and power dissipation, this is due to it's low A.F. activity factor and passing a strong signal in less number of pass logic.

2.3 Novel High Performance CMOS Full Adder
The novel adder cell (NEW) has 16 transistors, as shown in fig.3. It is based on the 4-transistor implementations of the XOR and XNOR functions presented in, pass transistor, and transmission gates [7]. NEW simultaneously generates H and H’, This new style has several advantages; first, it removes the inverter from the critical path of the cell, which decreases the cell delay. Second, it balances the delays of generating H and H’, which leads to fewer glitches at the outputs.

Third, it decreases the capacitance at node H, since it is no longer loading an inverter, while at the same time decreasing the capacitance at node H’. Also, it is noticed that NEW does not use any inverters or standard CMOS style. This eliminates the short-circuit power component within the cell. NEW consumes 4.5% less power than 14T and 9% less than TFA. Regarding speed, NEW is superior; it is faster than 14T by 28% and TFA by 8%. The overall savings show that from the power-delay product (energy), it saves 26% over 14T and 16% over TFA. Energy savings of 30% and 15% are achieved over 14T and TFA.

2.4 Full Adder For Embedded Architecture
New design full adder is characterized by consuming low power [8], as shown in fig. 4. This objective is achieved by eliminating any direct paths between the supply voltage and the ground and by reducing the number of internal node capacitances. It also has the advantage of low transistor count and hence occupies small area on silicon and operates at high speed. The designed circuit has the advantage of low power consumption because of the following reasons. First, the reduced number of transistors decreased the number and magnitudes of the internal node capacitances. The extracted netlist file generated from the layout shows that the new circuit contains only 5 capacitors while the 16-transistor circuit contains 8 capacitors and the Transmission Gate circuit contains 11 capacitors. Second, the reduced number of nodes results in a more flexible wiring requirement and hence reduces the value of the wiring capacitances. This reduction has a great effect on reducing the dynamic component of power consumed in charging and discharging these capacitances during the circuit operation. Third, for
any possible input pattern there will never be a direct path between Vdd and GND. Removing this path eliminates the short circuit power.

The circuit consumes 0.752*10^-4 Watt at a frequency of 500 MHz. The result shows that using the new cell saves 47% and 69% of the power consumed by using the 16-transistor and the transmission gate cells respective.

2.5 Static Energy recovery full adder cell

The Static Energy recovery full adder cell uses only 10 transistors and it does not need inverted inputs [9], as shown in fig. 5. The design was inspired by the XNOR gate full adder design. In non-energy recovery design the charge applied to the load capacitance during logic level high is drained to ground during the logic level low. It should be noted that the new SERF adder has no direct path to the ground. The elimination of a path to the ground reduces power consumption, removing the Psc variable (product of Isc and voltage) from the total power equation.

The charge stored at the load capacitance is reapplied to the control gates. The combination of not having a direct path to ground and the reapplication of the load charge to the control gate makes the energy-recovering full adder an energy efficient design. The performance of the SERF full adder cell is compared for power consumption, delay and silicon area against the transmission function adder (TFA), dual value logic (DVL) adder, and the fourteen transistor (14T) adder. The results shows that the proposed SERF adder design takes approximately 26% to 55% less energy than the other three designs chosen from the literature.

2.6 New Improved 14T Adder Cell

New improved 14T adder cell requires only 14 transistors shown in fig. 6. It produces the better result in threshold loss, speed and power by sacrificing four extra transistors per adder cell [10].

Even though the transistor count increases by four per adder cell, it reduces the threshold loss problem, which exists in the SERF by inserting the inverter between XOR Gate outputs to form XNOR gate. Newly proposed adders implement the Sum using XNOR-XNOR and Carry using PMOS - NMOS. We can also Build to produce Carry using NMOS-NMOS and PMOSPMOS. But the delay and power dissipation of PMOS-NMOS is better than other two kinds of producing Carry. The proposed XNOR gate is designed by putting inverter at the output of the XOR gate in order to improve the threshold loss problem, which exists in the SERF adder. Out of the three methods, PMOS-NMOS based Carry gives the better result in power, speed and threshold loss problem. The new improved 14T adder improves the threshold loss by 50% as compared to the SERF adder as per paper. It consume less power and delay as compare to SERF.

2.7 P-XOR and G-XOR Based Full Adder

It resembles the inverter-based XOR but the difference is that the VDD connection in the inverter-based XOR is connected to the input A. Because the new XOR gate has no power supply, it is called Powerless XOR, or P-XOR. Similarly, He propose a new XNOR gate which is named Groundless XNOR, or G-XNOR, because there is no direct connection to the ground[11].

The addition of 2 bits A and B with CIN yields a SUM and a COUT bit. The integer equivalent of this relation is shown by the (2) and (3) or (4)–(6)

\[
A + B + C_{IN} = 2 \times C_{OUT} + SUM \quad (1)
\]
\[
C_{OUT} = (A \land B) \lor ((A \lor B) \land C_{IN}) \quad (2)
\]
\[
SUM = (A \land B \land C_{IN}) \lor ((A \lor B \lor C_{IN}) \land \overline{C_{OUT}}) \quad (3)
\]
\[
SUM = A \oplus B \oplus C_{IN} \quad (4)
\]
\[
SUM = A \overline{B} \overline{C_{IN}} \quad (5)
\]
\[
C_{OUT} = (A \land (A \oplus B)) \lor (C_{IN} \land (A \oplus B)) \quad (6)
\]
Module-1 and module-2 can be XOR or XNOR gates and module-COUT can be a multiplexer, double PMOS or double NMOS transistors (shown in fig.7). The sum is generated by cascading module-1 and module-2. This implements (4) or (5). The COUT function is implemented by module-1 and module- according to (6).

The COUT function is implemented by module-1 and module- according to (6).

The simulation are conducted for different adder sizes, ranging from 2-bit to 16-bit. The rise time and fall time is set to be 0.01ns.

2.9 Adder Using Bridge Method

Bridge circuits are circuits that created a conventional conjunction between two circuits nodes[13]-[14]. Using this kind of circuits the classical circuits can be implemented faster and smaller than the conventional. Since one of the important parameter in circuit design is the chip area, the proposed style might reduce area or increase density of transistor in unit of area. If a function has $2^n-1$ logical ‘0’ and $2^n-1$ logical ‘1’ the function could be implemented by a fully symmetric style and other wise it called as semi symmetric style. The bridge design style focused its attention to meshes and connects each two adjacent mesh by a transistor, named “Bridge transistor”. Bridge transistor provides the possibility of sharing transistor of different path to create a new path from supply lines to an output. Sum function using bridge and carry function using bridge as shown in fig 10 and 11. Adder shows 13.8% (@ Vdd=0.65V) to 31.5% (@Vdd=1.5V) degradation in term of power consumption than conventional CMOS design. The delay improvement of 41.5% (@Vdd=0.65V) to 0.37% (@Vdd=1.5V). These adders have resulted better than the conventional CMOS.
The novel design of a 3T XOR gate combining complementary CMOS with pass transistor logic are proposed [15], as shown in fig. 12. The design has been compared with earlier proposed 4T and 6T XOR gates and a significant improvement in silicon area and power-delay product has been obtained. An eight transistor full adder has been designed using the proposed three-transistor XOR gate as shown in fig. 13 and its performance has been investigated using 0.15μm and 0.35μm technologies. Compared to the earlier designed 10 transistor full adder, the proposed adder shows a significant improvement in silicon area and power delay product.

The results of the comparative study show that the performance of the 8T full adder is somewhat poorer than the 10T full adder proposed in [12], in regard to its average power dissipation. However, the delay of the proposed adder is much less compared to any other adder. The net effect is that our proposed 8T full adder shows a much better power-delay product (PDP) compared to any other adders mentioned in literature.

### Table I

<table>
<thead>
<tr>
<th>CELLS</th>
<th>Tech @ SupplyVoltage @ Frequency</th>
<th>Avg. POWER (μm)</th>
<th>DELAY</th>
<th>PDP</th>
<th>No. TRAN.</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS [15]</td>
<td>0.35μm @ 3.3V</td>
<td>1.281</td>
<td>180.183</td>
<td>230.814</td>
<td>28</td>
</tr>
<tr>
<td>TGCMOS [15]</td>
<td>0.35μm @ 3.3V</td>
<td>1.140</td>
<td>111.242</td>
<td>126.816</td>
<td>20</td>
</tr>
<tr>
<td>TFA [7]</td>
<td>0.35 μm @ 3.3V @</td>
<td>0.697</td>
<td>3.140</td>
<td>2.189</td>
<td>16</td>
</tr>
<tr>
<td>14 T [7]</td>
<td>0.35μm @ 3.3V @</td>
<td>0.667</td>
<td>3.736</td>
<td>2.492</td>
<td>14</td>
</tr>
<tr>
<td>16 T XOR [7]</td>
<td>0.35μm @ 3.3V @</td>
<td>0.638</td>
<td>2.887</td>
<td>1.842</td>
<td>16</td>
</tr>
<tr>
<td>EA_10T [8]</td>
<td>0.35μm @ 3.3V @</td>
<td>0.752</td>
<td>2.455</td>
<td>1.8386</td>
<td>10</td>
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<tr>
<td>SERF [10]</td>
<td>0.12μm @ 1.2 V @</td>
<td>303000</td>
<td>0.823</td>
<td></td>
<td>14</td>
</tr>
<tr>
<td>HS_14T [10]</td>
<td>0.12μm @ 1.2 V @</td>
<td>10</td>
<td>0.403</td>
<td>4.03</td>
<td>10</td>
</tr>
<tr>
<td>9A [11]</td>
<td>0.35μm @</td>
<td>20% less</td>
<td>------</td>
<td>--------</td>
<td>10</td>
</tr>
<tr>
<td>9B [11]</td>
<td>0.35μm @ 3.3V @ 200MHz</td>
<td>13% less SERF</td>
<td>93% less SERF</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>13A [11]</td>
<td>0.35μm @</td>
<td>10% less</td>
<td>93% less</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>CLRCL [15]</td>
<td>0.35μm @ 3.3V</td>
<td>0.403</td>
<td>122.438</td>
<td>49.342</td>
<td>10</td>
</tr>
<tr>
<td>BRIDGEMETHOD [13]</td>
<td>0.65V</td>
<td>41.5%</td>
<td>60% CMOS</td>
<td></td>
<td>32</td>
</tr>
<tr>
<td>BRIDGEMETHOD [13]</td>
<td>1.5V</td>
<td>0.37%</td>
<td>10.2%</td>
<td></td>
<td>32</td>
</tr>
<tr>
<td>BRIDGEMETHOD [14]</td>
<td>3V</td>
<td>0.04%</td>
<td>4.4%</td>
<td></td>
<td>32</td>
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<tr>
<td>BRIDGEMETHOD [14]</td>
<td>1V</td>
<td>17% CMOS</td>
<td>34.1%</td>
<td></td>
<td>32</td>
</tr>
<tr>
<td>8T [15]</td>
<td>0.35μm m,3.3V @25MHz</td>
<td>0.409</td>
<td>1.651</td>
<td>0.675</td>
<td>8</td>
</tr>
</tbody>
</table>
3 Conclusion
In this paper, various one bit full adder cells design has been reviewed from the most recent published research work. The comparison of full adder cells with each other in term of power, delay, operating frequency and transistor count is done. Based on survey, it is concluded that the new 8T (8 Transistor circuit) have good signal level, consume less power and have high speed compare to all other designs at low supply voltage. This circuit is suitable for arithmetic circuits and other VLSI applications with very low power consumption and very high speed performance.

References:
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