Energy Efficient Interface Circuits between Adiabatic and Standard CMOS logic at 90 nm Technology

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Abstract - Adiabatic circuits and standard CMOS logic are widely employed in Low power VLSI chips to achieve high system performance. The power saving of adiabatic circuit can reach more than 90% compared to conventional static CMOS logic. The clocking schemes and signal waveforms of adiabatic circuits are different from those of standard CMOS circuits. This paper investigates the design approaches of low-power interface circuits in terms of energy dissipation. Several low-power interface circuits that convert signals between adiabatic logic and standard CMOS circuits are presented. With BSIM 3v3 90 nm CMOS technology, the energy consumption of proposed interface circuits has relatively large power saving over the wide range of frequencies. This paper also investigates the different power delay product over the wide range of supply voltages. Simulation has been done on tanner EDA tool at BSIM 3v3 90nm technology.

Key Words – Standard CMOS logic, adiabatic circuit, Interfaces, Low power, Power delay Product, Energy dissipation.

1 Introduction
With the development of VLSI technology power dissipation is increasing dramatically. Low power has become one of the crucial design constraint, especially for portable and battery operated systems. In standard CMOS logic circuits, each switching event causes an energy transfer from the power supply to the output node or from the output node to ground. Compared with the conventional low power approaches, power dissipation can be significantly reduced by using the adiabatic computation. By properly mixing the ideas derived for adiabatic and static CMOS circuits one can achieve very low power dissipation in the circuit. Adiabatic logic circuits utilize AC voltage supplies (power-clocks) to recycle the energy of circuit nodes. During recovery phase, the energy of the circuit nodes is recovered to the power source instead of being dissipated as heat. In the adiabatic circuits, circuit nodes are charged and discharged by AC voltage supplies, thus their output signals are clocked AC signals (adiabatic signals). Since, the AC supplies controls the working rhythm of the circuits, they are also called power-clocks. As is well known, a DC power supply and rectangle-wave clocks are used in the standard CMOS circuits, thus the outputs of the standard CMOS circuits are typical rectangle-wave signals (CMOS signals). In order to utilize the strengths of various low power approaches, we consider that both adiabatic logic and standard CMOS circuits co-exist on a single chip.

2 Adiabatic CMOS Interface Circuits
The Adiabatic CMOS Interfaces can be implemented using two approaches. One is based on peak sampling techniques and the other is based on comparators. At 90nm technology the peak sampling technique is inferior because it shows high energy dissipation compared with other techniques. This paper investigates the comparison between interfaces at 90 nm technology.

2.1 Peak Sampling based Technique
The logic value of the adiabatic signal can be sampled and then held using a master-slave flip-flop to attain a standard CMOS output. Fig.1 shows an adiabatic-CMOS interface based on the peak sampling. A positive edge triggered CMOS flip-flop with a master-slave configuration is used to sample the peak voltage of the adiabatic signal. The pc signal is the rectangle-wave clock that comes from the synchronous Power-clock generator. The sampling operation should be switched in the proper phase, i.e. only when the adiabatic signal inclk is at the hold state. Fig. 2 shows the values of power delay product at different values of Vdd. As it is prominent from the graph as we are increasing the value of Vdd the PDP is also increasing. Delay remains constant for all the values of Vdd. This interface does not show appreciable power saving over a range of frequencies at 90nm technology and provides static CMOS output.
2.2 Comparator Based Techniques

The adiabatic-CMOS interface can also be realized by using comparators. A Schmitt inverter has been used for the adiabatic-CMOS interface. The schematic is shown in Fig. 3. The Schmitt circuit responds to a slowly changing input waveform with a fast transition at the output terminal. Thus, the short-circuit loss of the next-stage circuit can be reduced, while itself has larger short-circuit current because of its positive-feedback configuration. The circuit is simulated using 90nm CMOS technology. At 90nm technology this circuit shows more power dissipation compared to peak sampling based technique. Fig. 4 is depicting the power delay product at various values of Vdd. For all the values of Vdd delay remains constant and power dissipation is increasing as Vdd increases.

The above two circuits have large short-circuit current, because of the gradually rising and falling adiabatic signal. For eliminating the short circuit current a power clocked CMOS (PC2MOS) inverter is shown in Fig. 9. The second-stage inverter is used for shaping of the output signal. The structure of
PC²MOS is similar to clocked CMOS circuits, but
the gate of the P-type and N-type transistors is
controlled by the power-clock instead of the
rectangle-wave clock used in CMOS circuits. The
PC²MOS has only charging current for the output
node A when the input signals (in) falls. The
introduction of the power-clock clk doesn’t add large
energy loss because it operates in a fully adiabatic
manner for the gate of the transistors. It is verified
that the interface based on the PC²MOS comparator
has low energy loss because the short-circuit
dissipation has been completely eliminated. This
circuit provides dynamic CMOS output. Fig 10
shows the power delay product at different values of
Vdd. For all the values of Vdd delay remains
constant. Power dissipation gradually increases with
the increase in Vdd. Fig 11 shows the energy loss per cycle over a wide range of frequencies. Energy loss per cycle is decreasing as the Operational frequency is increasing. This circuit provides dynamic CMOS output.

Fig. 9 Power clocked CMOS Comparator based
interface circuit.

Fig. 10 Power delay product at different supply voltages

In order to convert the adiabatic signal into a static
CMOS one, an improved power-clocked CMOS
(IPC²MOS) inverter is shown in Fig. 12. The
second-stage inverter is used for shaping of the
output signal. The power-clocks clk0, clk3, and clk2
drive the gates of the transistors, and they are used to
avoid the short-circuit current and control the
comparison time of the IPC²MOS inverter. The
IPC²MOS inverter doesn’t have short-circuit current.
A standard static CMOS signal can be obtained,
because the comparison is only carried during the
peak of the adiabatic signal.

Fig.12 Improved power-clocked CMOS (IPC²MOS)
Comparator

Although this circuit provides very good results at
180 nm TSMC technology but this circuit provides
the worst results at 90nm technology. As it is
prominent in Fig. 13 and 14 it shows very high
power dissipation and energy loss per cycle. So,
some modifications to this circuit have been done to
achieve lower power dissipation.

Fig.13 Power delay product of IPC2MOS
inverter based interface at different values of Vdd

Fig.14 Energy loss per cycle at different operational
frequencies

In the proposed circuit some different clocking
schemes are applied to the improved power clocked
CMOS inverter reported in literature. This circuit
does not show any short circuit current dissipation.
The proposed design shows the best results at 90nm
technology. A proposed IPC²MOS interface is
shown in Fig.15. Fig.16 shows the power delay
product at different values of Vdd. As it is depicting
in the figure this proposed circuit shows the least
power dissipation. Fig. 17 shows the energy loss per cycle over a wide range of frequencies. This circuit shows the least energy loss per cycle.

Fig 15 Proposed circuit for adiabatic-CMOS interface

Fig.16 Power delay product of proposed interface at different values of Vdd

Fig.17 Energy loss per cycle vs. operational frequency

3 CMOS -Adiabatic Interface Circuits
Numbers of CMOS-adiabatic interface circuits are in Figs. 18, 19 and 20. It consists of a signal converter, a CMOS edge-triggered flip-flop, and the two CMOS inverters. The signal converter converts the signals (inclk0 and inbclk0) to the adiabatic signals (out and outb). In order to avoid the deformation of the adiabatic signals, the input signals (inclk0 and inbclk0) of the converter should been only switched during wait states, thus a flip-flop is used to synchronize. The rectangle-wave clock (pc0) is generated by using the CMOS inverter comparing clk0 with VDD/2. Thus, the outputs of the flip-flop are only switched during wait states to make the inputs of the converter to have the proper phase. This circuit has been simulated at 90 nm technology. Power delay product at various values of Vdd is shown in Fig. 19. Energy loss per cycle over a wide range of frequencies is shown in Fig.20. Comparatively more energy loss is depicted by this circuit as compared to other interfaces.

One source of energy loss occurs from the comparator’s large short-circuiting dissipation. The interface based on Power clocked CMOS inverter is shown in fig.21. The rectangle-wave clock is generated using the PC2MOS is to reduce short-circuit current. The signal converter uses the buffer to reduce the input capacitances of the signal converter.

Fig. 18 CMOS-adiabatic interface based on static flip-flop and comparator using two CMOS inverters.

Fig. 19 Power delay product of CMOS-Adiabatic interface at different values of Vdd

Fig.20 Energy loss per cycle vs. operational frequency

Fig. 21 CMOS-adiabatic interface based on static flip-flop and comparator using power-clocked CMOS (PC2MOS).

The simulations reveals that this circuit also shows a large power saving over a wide range of frequencies at 90nm technology as shown in Fig.23.
The CMOS flip-flop used in the CMOS-adiabatic interfaces has large energy loss compared with adiabatic circuits, because it doesn’t operate in an adiabatic manner.

A power-clocked flip-flop (PCFF) to reduce its energy loss is shown in Fig 24. The interface consists of a FPAL buffer that converts CMOS signal to adiabatic one, and a PCFF that is used to synchronize. The structure and operation of PCFF are similar to CMOS transmission-gate flip-flops with a master-slave configuration except that it uses 4-transistor transmission gates that are driven by power-clocks instead of rectangle wave clocks. Energy loss per cycle over a wide range of frequencies for the above interface is shown in Fig.26.

Because the above interface doesn’t need the comparator and the energy of its clock input capacitances can be well recovered, lower energy dissipation can be expected and this circuit shows large power saving at 90 nm technology.

4 Comparisons of Energy Dissipations

In terms of types of converted output signals, the adiabatic-CMOS interfaces can be classified into two types. A type of interfaces can obtain a standard static CMOS output (Fig. 1, Fig.12, and Fig. 15), while another type of interfaces only obtains a clocked CMOS output (Fig. 3, Fig. 6, Fig. 9). For the interfaces with static CMOS outputs, the proposed IPC2MOS adiabatic-CMOS interface attains energy savings from 50 to 300MHz, as compared to implementation using a C2MOS flip-flop. For the interfaces with a clocked CMOS output, the PC2MOS adiabatic-CMOS interface attains energy savings as compared to the other two implementations over a range of frequencies, respectively. Among the three CMOS adiabatic interfaces, the circuit of Fig. 24 has low energy dissipation. The interface based on the power-clocked flip-flop attains energy savings clock rates ranging from 50 to 300MHZ.
Series 1- CMOS-adiabatic interface based on static flip-flop and comparator using two CMOS inverters. Series 2- CMOS-adiabatic interface based on static flip-flop and comparator using power-clocked CMOS (PC2MOS).
Series 3- CMOS-adiabatic interface based on power-clocked flip-flop.

### 5 Power delay Product Comparisons

Adiabatic-CMOS Interfaces Comparisons
It is evident from Fig. 29 that the power delay product of proposed circuit is yields the best results.

![Power Delay Product Comparisons](image)

Fig. 29 Power Delay Product comparisons of adiabatic-CMOS interfaces
Series1-Peak sampling based interface
Series2-Schmitt inverter based interface
Series3-CMOS inverter based interface
Series4-Power clocked CMOS inverter based interface
Series5-Proposed interface at 90nm technology

CMOS-Adiabatic interfaces:
It is evident from Fig. 30 that the power delay product of interface circuit based on power clocked flip flop produces the best results.

![Power Delay Products Comparisons](image)

Fig. 30 Power Delay Product comparisons of adiabatic-CMOS interfaces

### 6 Conclusion

Integrated circuits can be designed with both adiabatic and conventional CMOS logic on the same chip. There were different types of interface circuits available in the literature. Power-clocked CMOS (PC2MOS) comparator shows relatively large power savings over a wide range of frequencies, for clocked CMOS output. Proposed Improved Power-clocked CMOS (IPC2MOS) comparator with different clocking schemes shows relatively large power savings over a wide range of frequencies, for static CMOS output. CMOS-adiabatic interface based on power-clocked flip-flop and CMOS-adiabatic interface based on static flip-flop and comparator using power-clocked CMOS (PC2MOS) shows the best performance among the all other reported circuits in terms of energy dissipation over a wide range of frequencies.

### References