

# High Speed, Low Power 8T Full Adder Cell with 45% Improvement in Threshold Loss Problem

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**Abstract:** Full adder is an essential component for designing all types of processors viz. digital signal processors (DSP), microprocessors etc. Demands for the low power VLSI have been pushing the development of design methodologies aggressively to reduce the power consumption drastically. In most of the digital systems adder lies in the critical path that affects the overall speed of the system. So enhancing the performance of the 1-bit full adder cell is the main design aspect. The present study proposes a low power full adder cell with least MOS transistor count that reduces the serious problem of threshold loss. It considerably increases the speed. Result shows 45% improvement in threshold loss problem and considerable reduction in power consumption over the other types of adders with comparable performance. The simulation has been carried out on Tanner EDA tool on BSIM3v3 90nm and 130nm technologies.

**Key words:** Full adder, high speed, low power, PDP, XOR gate, VLSI.

## 1 Introduction

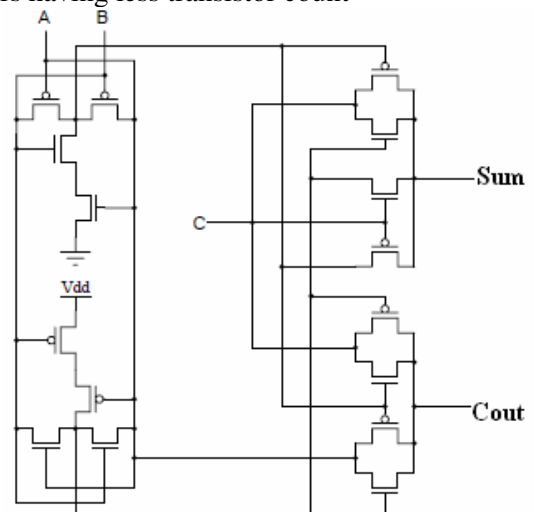
The full adders form the basic building blocks of all digital VLSI circuits. The considerable improvement have undergone at very high pace. The main motto behind such blinding pace are being motivated by three basic design goals, viz. minimizing the transistor count and the power consumption and increasing the speed of operation. The full adder performance affects the system as a whole. A variety of full adders using static or dynamic logic styles have been reported in the literature [1]-[8]. To meet the growing demand, we propose the new high speed and energy efficient full adder cell using 8 transistors (least number of transistors) that yielded very encouraging results, so to say, the best in speed, power and threshold loss in comparison to other adders using transistor count of 10, 14 and 16 [1],[3],[4],[5].

The adder has been designed using 90nm and 130nm technologies to establish the technology independence. Simulation results indicate that the proposed 8T full adder cell operates at high speed and has low power dissipation than its peer designs.

The rest of the paper is organized as follows: In Section II, we briefly describe the previous work reported in the literature. In Section III, we propose the new 8T full adder cell. In

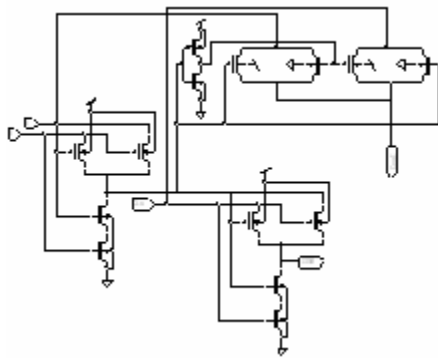
## 2 Previous Work

The literature survey reveals very wide spectrum availability of adder designs over the past few decades. Several designs of low power and high speed adder cells are available in the literature. The full adder cell realization of the circuit using 16 transistors [1] is shown in Fig.1. This circuit can operate with full output voltage swing but consumes significant amount of power and have more delay compared to other adders having less transistor count



(W/L)<sub>n</sub>=1/1 and (W/L)<sub>p</sub>=2.5/1

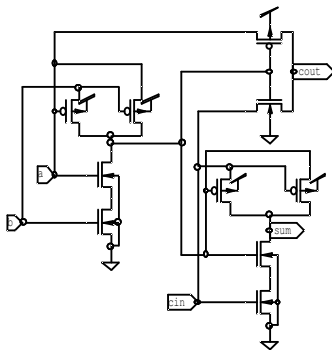
Fig.1 16T full adder



(W/L)<sub>n</sub>=1/1 and (W/L)<sub>p</sub>=2.5/1  
Fig.2 14T full adder

With the aim of further minimizing the number of transistors, pass transistor logic based XOR and XNOR circuits [2] were used and as a result the 14T full adder circuit of Fig.2 was designed. This circuit among all 14T full adder circuits [3],[4] shows the better results for delay and power as compared to 16T full adder but it suffers from the threshold loss problem of approximately 0.4v. It works well in high performance multipliers with low power consumption.

The further designed 10T full adder [5] of Fig.3 uses inverter-based 4T XOR gates in their design and shows remarkable improvements in power and delay. It also reduces the silicon area. This reveals better performance than the SERF 10T adder cell [5]. The drawback of this circuit is that it also suffers from threshold loss problem of 0.35v approximately equal to 14T adder circuit.



(W/L)<sub>n</sub>=1/1 and (W/L)<sub>p</sub>=2.5/1  
Fig.3 10T Full adder

### 3 Proposed 8T Full Adder

This design of proposed full adder is based on three transistor XOR gates. It acquires least silicon area. The design of 3T XOR gate is shown in Fig.4. The heart of the design is based on a modified version of a CMOS inverter and a PMOS pass transistor.

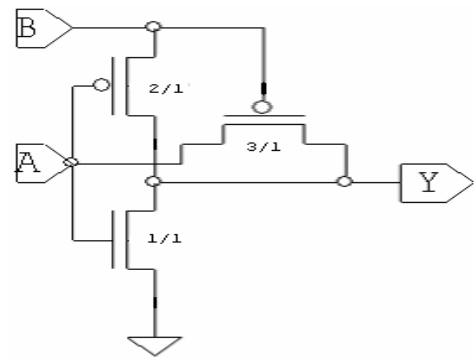


Fig.4 Design of 3T XOR gate

The design of 8T full adder cell having the least number of transistors using 3T XOR gates is shown in Fig.5. The Boolean equations for the design of the 8T full adder are as follows:

$$Sum = A \oplus B \oplus Cin$$

$$Cout = Cin (A \oplus B) + AB$$

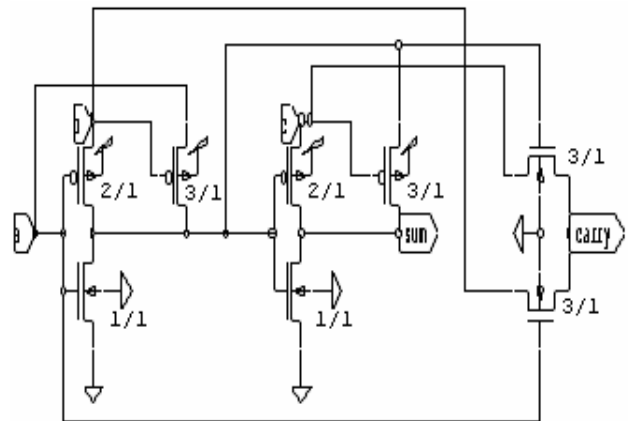


Fig.5 Proposed 8T full adder

This circuit shows approximately 45% improvement in threshold loss (0.2v) as compared to other adders stated above. It is the fastest and consumes least power. Therefore we report it to be the best on account of power consumption, delay and threshold loss.

### 4 Simulation and Performance Analysis

We have performed simulations using Tanner EDA tool in 90nm and 130nm technologies; with supply voltage ranging from 1v to 2.6v in steps of 0.2v. To establish an impartial testing environment each circuit have been tested on the same input patterns.

Comparative studies on the different adders found in literature have been done using 90nm and 130nm technologies. Studies have been done with 16T, 14T, 10T and the proposed 8T full adder cells.

In our proposed adder circuit we have shown that reducing the aspect ratio of the PMOS transistors results in better performance while keeping the threshold loss constant.

The result of the comparative study shows that the performance of the proposed 8T full adder cell is the best among all. The 8T full adder cell also occupies the minimum silicon area on chip amongst all the full adders reported so far in the literature. The small silicon area of the proposed full adder cell makes it potentially useful for building compact VLSI circuits on a small area of chips. The threshold loss, delay and power dissipation of the proposed full adder cell is much less compared to any other adder. The net effect is that our proposed 8T full adder cell shows a much better performance compared to any other adders available in the literature. Fig.6-17 shows the comparative analysis of the circuits stated above at 90nm and 130nm technology. The simulation results reveal that the proposed 8T full adder is proven to be the best if the main design aspects of area covered on chip, threshold loss, delay and power consumption are the ultimate goals.

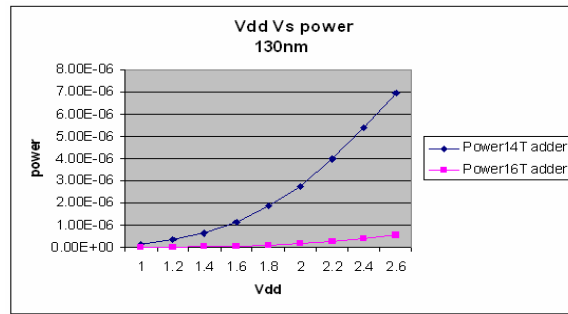


Fig.9

The above results show that the delay is more in the case of 16T adder as compared to 14T adder but the power dissipation of 16T adder is far superior to 14T adder having advantage of full output swing over 14T adder also. We have also compared the 16T full adder with 10T full adder to show the superiority of one over the other.

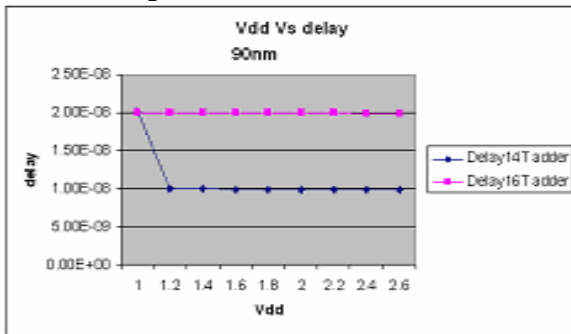


Fig.6

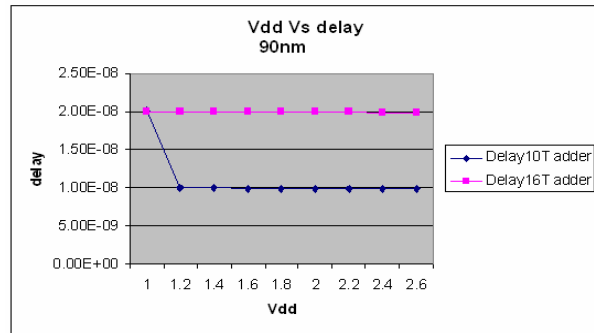


Fig.10

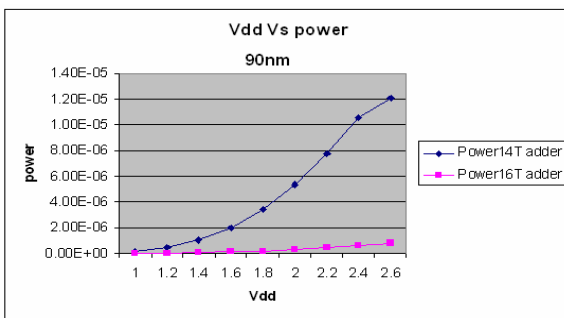


Fig.7

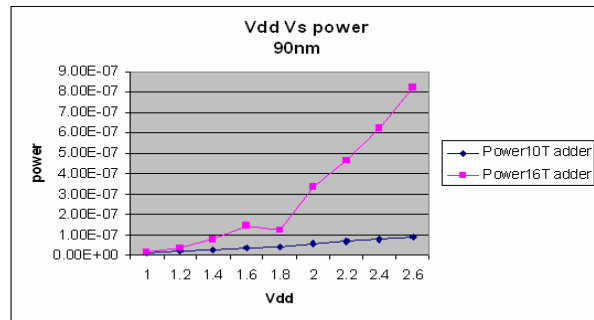


Fig.11

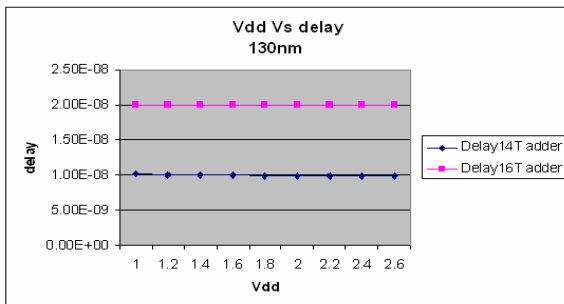


Fig.8

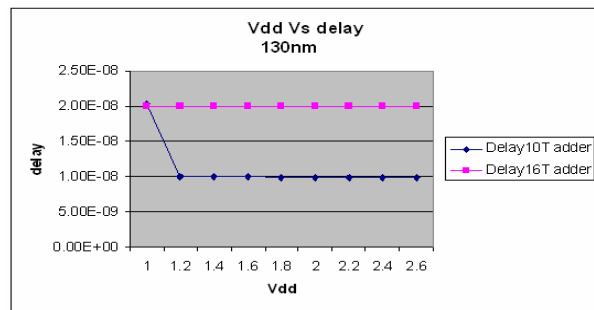


Fig.12

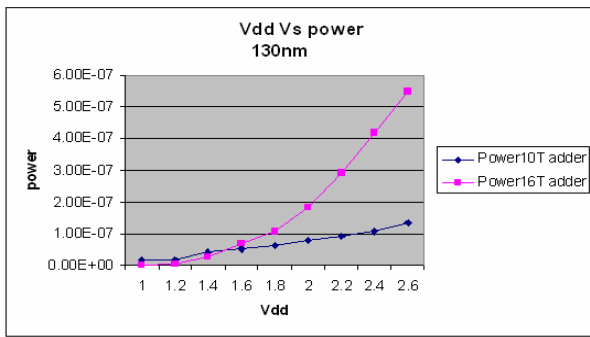


Fig.13

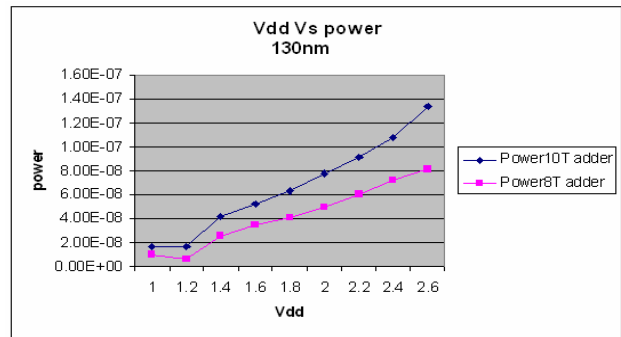


Fig.17

The above simulation results shows that the 10T full adder is giving better performance than 16T full adder in all perspectives such as area covered, delay and power dissipation and hence it proves its superiority. Now we have also compared with the best available in the literature (10T full adder) with the proposed 8T full adder.

The proposed 8T full adder circuit has threshold loss of approximately 0.2v which is nearly 45% less compared to the circuits available in the literature. Other full adder circuits explained in this paper have the threshold loss of nearly 0.35v except 16T full adder resulting into the full output swing.

### 5 Conclusion

The current work proposes the design of the improved full adder cell using 8T which acquires least area and has least power dissipation along with the lowest transistor count. It also shows nearly 45% improvement in threshold loss problem compared to other circuits [1]-[8]. With the help of this adder cell, we can design an efficient and high performance multiplier unit. The proposed 8T adder has been designed and studied using 90nm and 130nm technologies, which establish the technology independence of the circuit. The designed full adder is found to give better performance than the adders mentioned in literature so far as the low power and threshold loss is concerned. As the result reveals that the proposed 8T full adder cell yields high speed and low power consumption which signifies that its power-delay product would be the best among all full adder cells reported in the literature.

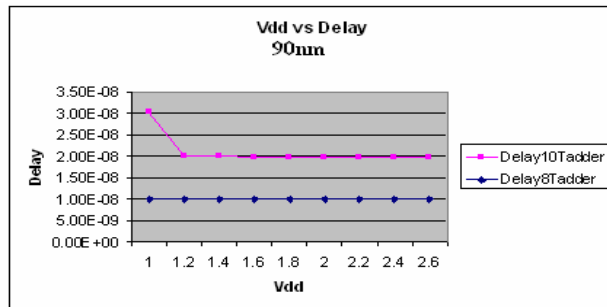


Fig.14

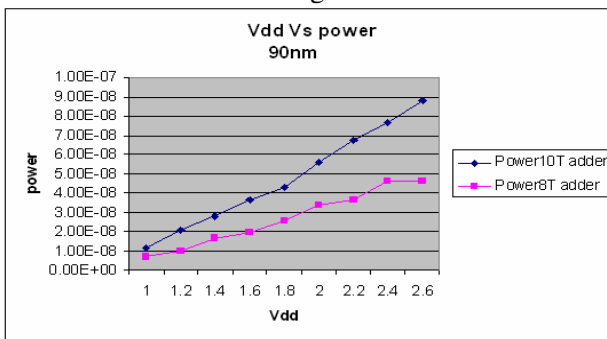


Fig.15

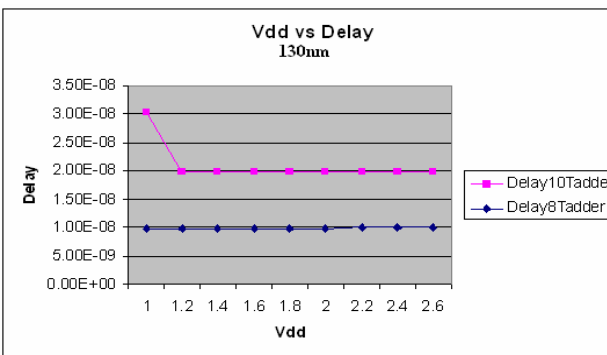


Fig.16

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