Reordering of Test Vector Using Artificial Intelligence Approach for Power Reduction during VLSI Testing

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Abstract: - Optimization of testing power is a major significant task to be carried out in digital circuit design. Low power VLSI circuits dissipate more power during testing when compared with that of normal operation. As the feature size is scaled down with process technology advancement, power minimization has become a serious problem for the designers as well as the test engineers. Test vector reordering for dynamic power minimization during combinational circuit testing is a sub-problem of the general goal of low power testing. The reordering is the process in which the sequence of applying test vectors is altered to reduce power dissipation. Power dissipation in CMOS circuits has two components: static, due to leakage current; and dynamic, due to switching activity. In this project, Artificial Intelligent (AI) based approach is presented to reorder the test vectors such that the minimum switching activity and hence the power dissipation during testing. In this method the hamming distance between successive test vectors is used to reorder the sequence. AI based reordering algorithm is implemented in Matlab and experimented with ISCAS85 benchmark circuits. Results show that the reordered test set minimized the testing power considerably when compared with unordered test set. Experimental results show that the proposed method reduces 30.15% of average power and 34.56% of the peak power when the reordered test vectors are used for testing.

Key-Words: - Combinational Circuit, Testing, Test Power, Artificial Intelligent, Reordering, Power dissipation.

1 Introduction

Very Large Scale Integration (VLSI) design plays a significant role in the fabrication of modern Integrated Circuits (ICs) with smaller in size and with more features for any electronics systems. Power consumption has become one of the biggest challenges in high-performance VLSI design. Designers are thus continuously challenged to come up with innovative ways to reduce power while trying to meet all the other constraints imposed on the design. As a consequence, a lot of low power design techniques have been proposed at all levels of the design hierarchy. However, all these techniques focus on low power dissipation. Advancements in semiconductor fabrication technology has helped the design engineers to accommodate more number of transistors in a VLSI chip. With the proliferation of mobile battery-powered devices, reduction of power in the embedded VLSI chips has become an active area of research. During the last decade, power reduction techniques have been proposed at all levels of the design hierarchy from system to device levels. For the development of complex, high performance, low power devices implemented in deep submicron technology, power management is a critical parameter and it cannot be ignored even during testing. With the increase in the density of the chips, the problem of testing has also increased manifold. A related problem is to achieve power reduction during the actual testing of a chip. Power consumption in test mode is considerably higher than the normal functional mode of a chip. The reason is that test patterns cause as many nodes switching as possible, while a power saving system mode only activates a few modules at a time. Thus, during testing switching activity in all the internal lines of a chip is often several times higher than during normal operation. Sometimes parallel testing is used in SoCs to reduce test application time, which results in excessive power dissipation. Again, successive functional input vectors applied to a given circuit during system mode have a significant correlation, while the correlation between consecutive test patterns can be very low. Usually, there is no definite correlation between the successive test patterns generated by an ATPG (for external testing) or by an LFSR (for BIST) for testing of a circuit. This can cause significantly

larger switching activity in the circuit during testing than that during its normal operation. Low power dissipation during test application is becoming an equally important figure of merit in today's VLSI circuits design with BIST and is expected to become one of the major objectives in the near future. In this paper we have proposed an AI-based approach to reorder the test vectors such that the switching activity and hence the power dissipation during testing is reduced.

2 Power Dissipation in CMOS Technology

The VLSI low power design problems can be broadly classified into two analysis and optimization. Analysis problems are concerned about the accurate estimation of the power or energy dissipation at different phases of the design process. The analysis techniques differ in their accuracy and efficiency. Analysis technique also serves as the foundation for design optimization. Optimization is the process of generating the best design, given on optimization goal, with out violating design specifications. Dabholkar et al. [2] have proposed several heuristics both for combinational circuits and scan-based sequential circuits. They show that computing an optimal order of the test vectors such that the switching activity of a combinational circuit is minimized is an NP-hard problem. There are two types of power dissipation in CMOS circuits.

1. Dynamic power dissipation
2. Static power dissipation

Dynamic power dissipation is caused by switching activities of the circuit. A higher operating frequency leads to more frequent switching activities in the circuit and results in increased power dissipation [7]. Static power dissipation is related to the logical states of the circuits rather than switching activities, in CMOS logic, leakage current is the only source of static power dissipation. However, occasional deviations from the strict CMOS style logic can cause static current to be drawn.

3 Existing Methods

In the domain of circuit testing, low-power dissipation test methods have been investigated thoroughly for combinational and sequential circuits. Dabholkar et al. [2] have proposed several heuristics both for combinational circuits and scan-based sequential circuits. They show that computing an optimal order of the test vectors such that the switching activity of a combinational circuit is minimized is an NP-hard problem. They categorize their heuristics for combinational circuits as with or without repetition of test vectors. Christofides's heuristic and a greedy heuristic are used for the case of test vector reordering without repetition. Christofides's heuristic uses a minimum spanning tree based method to find a Hamiltonian path of the transition graph composed from the test set; the algorithm has $O(n^3)$ complexity. A greedy heuristic is also proposed which exhibits better running time for all the benchmark circuits.

Kruskal's minimum spanning tree algorithm is used for the second case where repetition of test vectors is allowed. However, in the context of dynamic power minimization during testing, a test set without repetition of test vectors is always better than a test set with repetition in the sense that repeated vectors do not contribute to the increment of fault coverage but increase the total switching activity. A scheme is proposed by Chattopadhyay and Choudhary [1] that uses a genetic algorithm based approach for reducing the hamming distance between consecutive patterns in the test set. As the hamming distance reduces, the switching activity in the circuit is also expected to reduce. Improved version of genetic algorithm-based approach for combinational circuit testing was proposed by Chattopadhyay and Choudhary [1]. While the actual vector reordering was done using $O(n^2)$ Prim's Algorithm, the chromosomes of Chattopadhyay's genetic algorithm were used to represent subsets of the original test set. Using a number of operators, they were able to find a remarkably low value for switching activity at the cost of reduced fault coverage.

Flores [2] have proposed a scheme to reorder the initial test pattern set and exploiting don't cares present in the initial set. This technique uses a recursive Travelling Salesman Problem (TSP) formulation and tries to decrease the switching activity in the circuit at each recursive call. In the work by Chakravarty and Dabholkar [2], the authors construct a complete directed graph in which each edge represents the number of transitions activated in circuit after application of the vector pair. The authors use a greedy algorithm to find a Hamiltonian path of minimum cost in the graph. Girard [3] propose using the Hamming distance between test vectors rather than the number of transitions in the circuit to evaluate the switching activity produced in the CUT by a given input test pair. Using the Hamming distance makes it possible to apply test vector reordering to large VLSI designs. A survey on low power testing of VLSI circuits has been given in [11].

There are several techniques for low power testing of VLSI circuits such as, test vector reordering, scan chain ordering, power-constrained test scheduling, use of multiple scan chains, low power test pattern generation, vector compaction, etc. Test vector reordering is a very well-known technique to reduce dynamic power dissipation during combinational circuit testing through switching activity minimization in the circuit. In [4], an evaluation of different heuristic approaches has been done in terms of execution time and quality. Here, it has been shown that the Multi-Fragment heuristic performs better than Christofides and Lin-Kernighan heuristics in terms of time. It also outperforms the Christofides heuristic in terms of quality and achieves performance very close to Lin-Kernighan. In [6,10], the problem of test vector reordering has been mapped into finding the Hamiltonian path in a fully connected weighted graph which is similar to the travelling salesman problem.

4 Proposed Method

Most popular techniques for test power minimization orders the deterministic test patterns and several approaches have been followed for test vector reordering such as, finding minimum cost Hamiltonian path [9] after mapping the problem into TSP instance, finding optimal solution by applying GA or SA. Although the dynamic power minimization problem by test vector reordering during VLSI testing is an old problem, here we have proposed a new approach for solving it using Artificial Intelligence (AI). This problem can again be viewed as finding optimal path from start to goal node in a search space by applying informed search methods of AI, where start node is the node when no test vector is selected and the goal node is the node when only one test vector is remaining for selection. A* search algorithm is a very well-known informed search method used in AI. It takes advantages of both efficiency of greedy search and optimality of uniform-cost search by simply summing the two evaluation functions. Thus, it is optimally efficient algorithm for finding optimal solution in an informed search space. This has motivated us to apply A* search technique for test vector reordering problem for dynamic power reduction during testing.

4.1 Problem Formulation

Consider a test set for a combinational circuit is given by $V = \{ v1, v2,...vk \}$ with a predefined fault coverage, where $| V | = k$. Each test vector is formed by a fixed ordered set of bits bj i.e., $vi =< b1, b2, ...bl >$, where l =length of the test vectors or the number of primary inputs (PIs) of the circuit. Assume Π be the initial ordering of test vectors V. The problem of dynamic power minimization by test vector reordering is to compute an optimal vector ordering Π 'of V such that total dynamic power dissipation in the circuit during testing is minimized. The problem of reducing the peak power dissipation is not considered here. Only the average power reduction has been considered. Since, the power dissipation is directly proportional to switching activity, the problem can be restated as to find out an optimal path or optimal ordering of vertices Π' from the search space of having all possible orderings of vectors V such that total switching activity in the circuit is minimized**.**

4.2 An A*-based Method for Dynamic Power Minimization by Test Vector Reordering

The A* algorithm [5] combines features of uniform-cost search and pure heuristic search to efficiently compute optimal solutions. A* is a best-first search in which the cost associated with a node is given by the evaluation function $f(n)$.

$$f(n) = g(n) + h(n) \rightarrow (1)$$

Where $g(n)$ is the cost of the path from the initial state to node n, and $h(n)$ is the heuristic estimate of the cost of a path from node n to a goal node. Thus, $f(n)$ estimates the lowest total cost of any solution path going through node n. At each point, a node with lowest f-value is chosen for expansion. Ties among nodes of equal f-value is broken in favour of nodes with lower h-values. The algorithm terminates when a goal node is chosen for expansion. For a given node, the sum [current cost + heuristic value] is an estimation of the cost of reaching the ending node from the starting node, passing by the current one. This value is used to continuously choose the most promising path. In practice, the algorithm maintains two lists of nodes that are filled and modified during the search: an open list and a closed list. Open list is a priority queue, contains the tracks leading to nodes that can be explored in increasing order of the evaluation function $f(n)$. Initially, there is only the starting node and at each step, the best node of open list is taken out. Then, the best successor of this node (according to the heuristic) is added to the list as a new track. The Closed list stores the tracks leading to nodes that have already been explored.

4.3 Reordering Algorithm

Step 1: The algorithm maintains two sets. Open list: The open list keeps track of those nodes that need to be examined. Closed list: The closed list keeps track of those nodes that have already been examined.

Step 2: Initially, the open list contains just the initial node and the closed list is empty. Each node *n* maintains the following: g(*n*) = the cost of getting from the initial node to *n* h(*n*) = the estimate, according to the heuristic function, of the cost of getting from *n* to the goal node. f(*n*) = g(*n*) + h(*n*)

Step 3: Each node also maintains a pointer to its parent, so that later the best solution if found can be retrieved A-star has a main loop that repeatedly gets the node, call it *n*, with the lowest f(*n*) value from the open list. If *n* is the goal node then the solution is given by back tracking from *n*. Otherwise *n* is removed from the open list and added to the closed list next all the possible successor nodes of *n* are generated

Step 4: For the each successor node *n* if it is already in the closed list and copy, there has an equal or lower *f* estimate, then safely discard the newly generated *n* and move on. Similarly, if *n* is already in the open list and copy there an equal or lower *f* estimate, then safely discard the newly generated *n* and move on.

5 Results and Discussions

The above algorithm is experimented with ISCAS85 benchmark circuit C17. It consists of 6 inputs and 2 outputs. It has 6 gates. As discussed earlier, the test vectors for the CUT C17 are generated from ATPG MINTEST and tabulated in Table 1. It consists of 6 Test vectors (n=6).

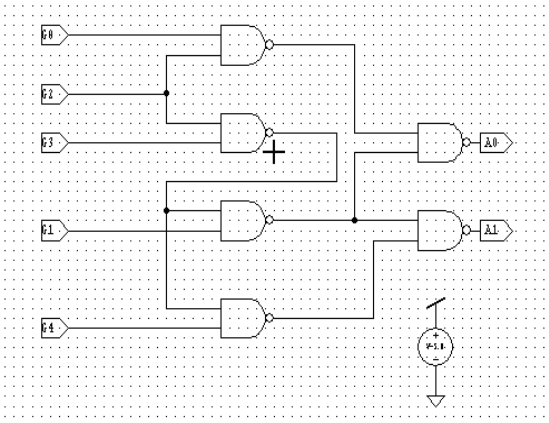

Fig. 1 C17 Benchmark Circuits

Table 1 Details of Benchmark Circuit C17

Circuit	No. of Gates	Inputs	Outputs	No. of test vectors	Fault coverage
C17	6	5	2	6	100%

Table 2 Test vector for C17 circuit

S.NO	Test vector
1.	11100
2.	11111
3.	00000
4.	01110
5.	01011
6.	10001

Table 3 Reordered Test vector

Reordered sequence	Test vector
1	11100
4	01110
5	01011
2	11111
6	10001
3	00000

The Test set contains of 6 vectors is serially numbered for C17 circuit. The C17 circuit is modeled in CMOS ML_0.25 (Technology) using T spice simulator of Tanner EDA tool and average power, peak power is calculated for reordered test vectors**.** The results are tabulated in Table 1 and Table 4 for details of benchmark circuits and average power, peak power of C17 circuit.

Table 4 Experimental Results for C17 circuit

Seed	Test Vector Order	Average Power (mW)	Peak Power (W)
Unorder	T1-T2-T3-T4-T5-T6	6.17	29.8
Reordered Test Vector			
1	T1-T4-T5-T2-T6-T3	6.89	19.5
2	T2-T5-T4-T1-T3-T6	4.49	19.8
3	T3-T6-T5-T2-T4-T1	4.31	45.8
4	T4-T5-T2-T1-T3-T6	5.77	20.8
5	T5-T4-T1-T2-T6-T3	6.71	24
6	T6-T3-T1-T2-T4-T5	4.61	21.5
% Improvement		(For Seed 3) 30.15%	(For Seed 1) 34.56%

6 Conclusion

The Reordering approach is implemented in matlab and experimented with ISCAS85 benchmark circuits. Results show that the reordered test set minimized the testing power considerably when compared with unordered test set. Experimental results show that the proposed method reduces 30.15% of average power and 34.56% of the peak power when the reordered test vectors are used for testing. Hence the proposed method can be used for reducing the power dissipation during testing of combinational circuit.

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