

Minimization of Crosstalk in High Speed PCB

D.ANISH, G.KRANTHI KUMAR, ROHITA JAGDALE

Department of Microelectronics and VLSI Design

International Institute of Information Technology

P-14, Rajiv Gandhi Infotech Park, Hinjewadi, Pune-411057

INDIA

datlab4u@gmail.com, kranthi59@gmail.com, rohita_jagdale@yahoo.com

Abstract: - Crosstalk is an important problem in high-speed printed circuit board design which is one of the signal integrity issues. A widely used theoretical model based on microstrip theory is presented in this paper. On this basis, the origin and the factors affecting crosstalk are introduced. Cadence Allegro is used to analyze these factors.

Key-words: - Signal integrity, crosstalk, aggressor line, victim line, micro strip, Cadence Allegro.

1. Introduction

Signal integrity is a measure of the quality of an electrical signal. In digital electronics, a stream of binary values is represented by a voltage or current waveform. Over short distances and at low bit rates, a simple conductor can transmit this with sufficient fidelity. However, at high bit rates and over longer distances, various effects can degrade the electrical signal to the point where errors occur, and the system or device fails. Signal integrity engineering is the task of analyzing and mitigating these impairments. Signal integrity engineering is an important activity at all levels of electronics packaging, from internal connections of an integrated circuit (IC) through the package, the printed circuit board (PCB), the backplane, and inter-system connections[1]. While there are some common themes at these various levels, there are also practical considerations, in particular the interconnect flight time versus the bit period, that cause substantial differences in the approach to signal integrity for on-chip connections versus chip-to-chip connections. Some of the main issues of concern for signal integrity are reflection, crosstalk, and power/Ground noise and EMI issues. Reflection noise occurs due to impedance mismatch, stubs, vias and other interconnect discontinuities.

Power and ground noise occurs because of parasitic effects in ground and power plane and ground bounce effect. Due to those effects the EMI/EMC issues occurred into systems [9]. The paper consists of crosstalk issues in high speed printed circuit board, different simulation results of crosstalk using Allegro SPB 16.01 and final conclusion from the results.

2. Crosstalk in High Speed PCBs

Crosstalk is an unintended electro-magnetic coupling between traces, wires, trace to wire, cable assemblies, components subject to electro-magnetic field disturbance. This undesirable effect is associated with clock, periodic signals, system critical nets like data, address, control lines and I/Os. Clock and periodic signals create majority of problems and can cause serious functionality concerns to other section of the assembly [4]. Crosstalk involves both capacitive and inductive coupling. Capacitive coupling usually results when one trace lies on top of another trace. This coupling is a direct function of the distance spacing between the trace and an overlap area. Coupled signals may exceed design limits with a very short trace route [4]. This coupling may be so severe that overlapping parallelism should be avoided at all times. Inductive coupling involves traces that are physically located in close proximity to each other. With two traces adjacent to each other, Current flows down one of the trace are aggressor or driven line,

Where as current will couple into the adjacent trace is victim line.

2.1 Forward and Reverse Crosstalk

Consider the case where the two traces are adjacent to each other as shown in Fig.1. Current flows down one of the trace: called as the aggressor or driven line. That current will couple into the adjacent trace: called the victim line and create two different noise signals. One of those noise signals will flow in the victim trace in the same direction as the aggressor current is called as forward crosstalk [2]. The other noise signal will flow in the victim trace in the opposite direction as aggressor trace is called as backward. These two currents have different characteristics and degrees of importance in our circuits [9].

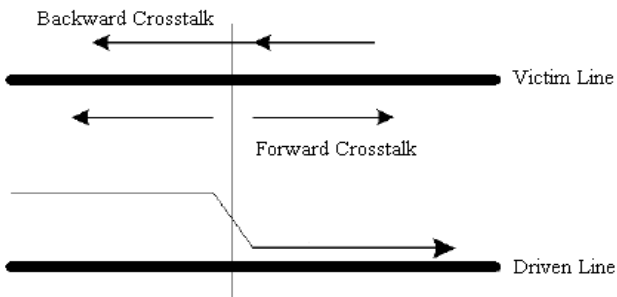


Fig.1 Forward Vs Reverse Crosstalk

2.2 Design Techniques to Prevent Crosstalk

To prevent crosstalk within a PCB, design and layout techniques listed here are useful within a PCB. *Crosstalk* will sometimes increase with a wider trace width. This is not true if the separation distance is held constant as a result of the ratio of self and mutual capacitance being held at a fixed ratio value. If the ratio is not fixed, mutual capacitance, C_m , will increase [1]. With the parallel traces, the longer the trace, the greater the mutual inductance, L_m . An increase in impedance, along with mutual capacitance, will increase with faster rise times of a signal transition, thus exacerbating crosstalk. The design and layout techniques are as follows [4].

1. Minimize physical distance between the components during placement.
2. Minimize parallel routed traces length.
3. Group logic families according to functionality.
4. Locate components away from I/O interconnects and other areas susceptible to data corruption and coupling.

5. Avoid routing of traces parallel to each other.
6. Route adjacent layers orthogonal.
7. Reduced trace impedance and signal drive level.
8. Reduce signal to ground reference distance separation.
9. Partition or isolate high noise emitters onto different layers within stack up assignments.
10. Provide termination on impedance-controlled traces, or traces rich in RF harmonic energy.

2.3 Crosstalk Estimation

Theoretical formula for calculating crosstalk based on some simplifying assumptions, but practically it is very difficult to calculate crosstalk. There are many ways for quantifying what the level of crosstalk might in design [4].

There are three things that affect the magnitude of the crosstalk noise signal:

1. The degree of coupling that exist between aggressor and victim traces.
2. The distance over which that coupling occurs.
3. The effectiveness of any traces terminations that might exist.

Formula for calculating crosstalk is

$$\text{Crosstalk} = K (H)^2 / (H^2 + D^2) \dots (1)$$

Here, constant K is always less than 1 and it depends on the circuit rise time and the length of the interfering traces, H^2 is product of the two heights of parallel traces and D is direct distance between the centerline of the traces. This equation clearly shows that to minimize crosstalk, by minimize H and maximize D .

If coupled region is very short, crosstalk does not have time to develop and crosstalk amplitude will be small for short coupling regions.

If two traces are coupled, backward crosstalk will develop. But, if the victim trace is transmission line that is terminated in its characteristic impedance at the near end, then the backward crosstalk pulse will be completely absorbed by the terminating resistor and will not reflect forward.

2.4 Problem Statement

Fig. 2 shows the layout of JTAG programmer. To study about crosstalk consider TCK trace as aggressor and TDI as victim trace. To solve the crosstalk issue consider separation methodology [2].

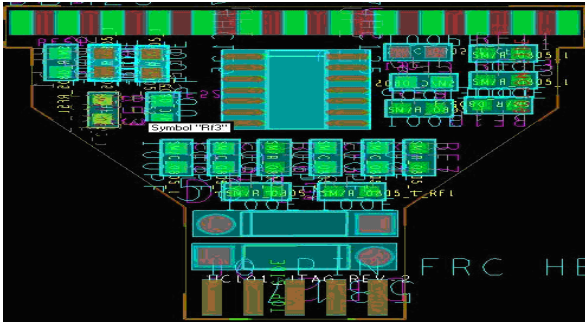


Fig.2. Layout representation of JTAG

3. Crosstalk Simulation

3.1 Basic Model

Fig. 3 shows basic coupled model [2][3]. First consists of TCK line driver J6 connected through transmission line TL1 of impedance 60Ω and microstrip to RF7. The second net consists of TDI with driver J6 connected through common microstrip (MS1) to RF6 with impedance of 127Ω [6] [7].

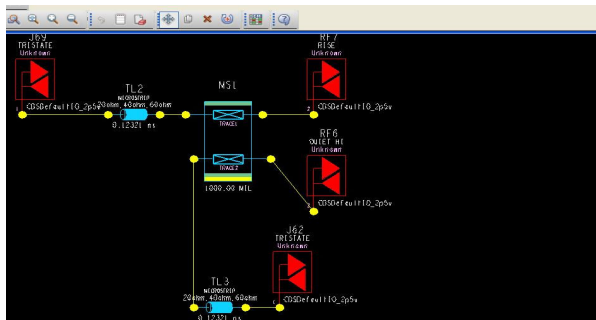


Fig.3 Basic Allegro model for crosstalk

3.2 Effect of length and Effect of separation

In order to minimize crosstalk consider trace length and trace separation methods. Fig. 4 shows simulation result of initial crosstalk in which both traces are separated by 5mils spacing and as a result the net crosstalk is 316.84mV.

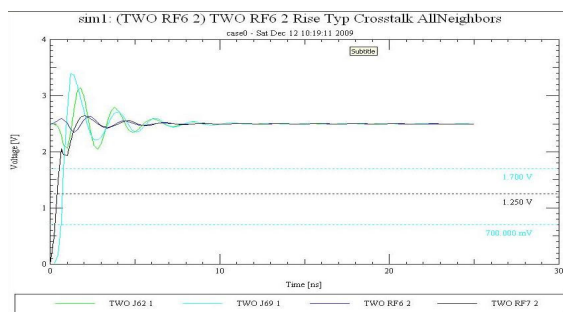


Fig. 4 Crosstalk simulation (F=50MHz, W= 5mil Spacing = 1000mil)

Fig.5 shows the simulation result of minimized crosstalk of model as shown in Fig.3. In which the spacing between the two traces is 2500 mils. As a result the net crosstalk is 0.01mV.

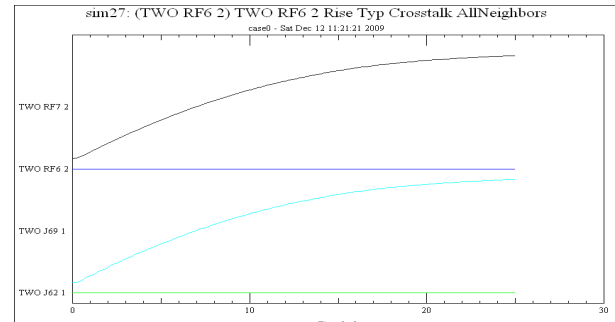


Fig 5: minimized crosstalk

Table 1 shows the various simulation results by varying the trace separation between aggressor and victim traces simultaneously. From above one, by reducing the trace impedance crosstalk also reduced but not up to desirable.

Table 1
Crosstalk Results for Varying Impedance method

Driver	Re cei ve r	MS1 Trace Width 2 [MIL]	TL2 Imped ance [ohm]	TL3 Imped ance [ohm]	Crosstal k [mv]
RF 6	J6	5	27	20	341.44
RF 6	J6	5	27	40	429.27
RF 6	J6	5	27	60	465.72
RF 6	J6	5	30	20	329.36
RF 6	J6	5	30	40	414.07
RF 6	J6	5	30	60	453.41
RF6	J6	5	33	20	318.6
RF 6	J6	5	33	40	401.22

Therefore even though impedance of traces is reduced at various levels there is slight variation in crosstalk which is not effective. Therefore next alternate method is maximizing the space between traces and its results are shown in Table 2. At 2500 mils spacing and the impedances of aggressor and victim traces are 60Ω and 60Ω respectively, then minimized cross talk is 0.01mv.

Table2
Crosstalk results for trace separation method

Driver	Receiver	MS1 . Trace Width1 [MIL]	MS1 . spacin g [MIL]	Crosstalk [mv]
RF 6.2	J6 2.1	5	5	316.84
RF 6.2	J6 2.1	5	300	0.91
RF 6.2	J6 2.1	5	600	0.23
RF 6.2	J6 2.1	5	900	0.1
RF 6.2	J6 2.1	5	1500	0.04
RF 6.2	J6 2.1	5	2000	0.02
RF 6.2	J6 2.1	5	2500	0.01

Another alternative method of reducing crosstalk in victim line is by connecting the shunt resistance of characteristic impedance at the near end. The following Fig. 6 shows the termination with shunt resistance at near end.

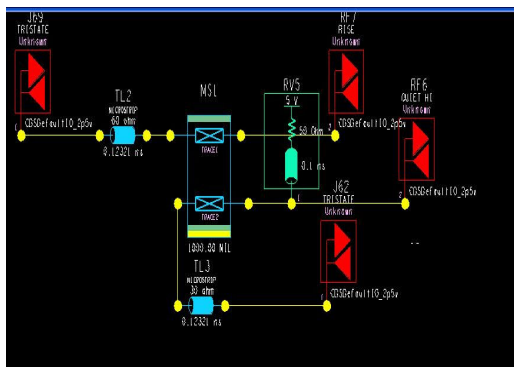


Fig. 6 Model with shunt termination at near end

Table 3
Results with Shunt Termination

Driver	Receiver	MS1 . Trace Width1 [MIL]	MS1 . spacin g [MIL]	Crosstalk [mv]
RF 6.2	J6 2.1	5	5	283.21
RF 6.2	J6 2.1	5	300	0.59
RF 6.2	J6 2.1	5	600	0.14
RF 6.2	J6 2.1	5	900	0.06
RF 6.2	J6 2.1	5	1500	0.02
RF 6.2	J6 2.1	5	1600	0.01

4. Conclusion:

Signal Integrity issues play an important role in determining the performance of a high-speed PCB design, out of them crosstalk has a major influence which is due to unintended electro-magnetic coupling between traces, wires, trace to wire, cable assemblies, components and other electrical components subject to electromagnetic field disturbance. As a result the signal at the receiver end may distort. So it is important to minimize the effect of crosstalk in a high-speed PCB design.

References:

- [1] <http://pcbdesignultimatetechasia.blogspot.com>.
- cross talk issues in high speed printed circuit board and various methods in order to reduce it.
8TH NOVEMBER 2009.
- [2] www.edacafe.com.
- For problem statements and their methodology to solve them. 12th October 2009.
- [3] www.cadence.com/help
- Usage of Allegro's signal integrity tool 15th October 2009
- [4] Douglas Brooks,
"Forward Vs. Backward", 21st October 2009.
- [5] Mark Imontose," PCB design technique
- for EMC compliance", 2nd edition- 28th September 2009.
- [6] Allegro® SI, Simulation and Analysis Reference, Product Version 16.01, June 2008 Cadence Design Systems, Inc.
- [7] Allegro® Constraint Manager Reference, Series 200 and 600, Product Version 16.01, June 2008 Cadence Design Systems, Inc.
- [8] Hall, Stephen, et.al. *High-Speed Digital System Design*, Wiley Inter science, New York, NY, ISBN: 0-471-36090-2, 2000.
- [9] Jinan Lou, *Cross Talk Driven Placement*- Synopsys Inc.