Mixed style of Low Power Multiplexer Design for Arithmetic Architectures using 90nm Technology

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Abstract: - As many researches are concentrating more on arithmetic circuits particularly with Multiplexer (MUX) design as heart of them, this paper also deals with MUX to optimize the power and hence the overall architecture of any greater module may have the considerable reduction in power. The combination of pass transistor (transmission gate) + static method gives a mixed style of MUX which is proposed in this paper and ensures full swing over pass transistor (alone) type of implementation. The circuit swing is an important factor because the use of 2-1 MUXes in a de-composed multiplexer must propagate the data to the output without signal degradation. TSPICE is the circuit simulator tool used and 90nm library is included for simulation. The power analysis and comparison between Complementary Static CMOS, Pass Transistor and the proposed styles will conclude this work is a better approach.

Key-words: - Mixed MUX, Pass transistor – static, low power MUX.

1 Introduction

Multiplexer abbreviated as MUX is the heart of any arithmetic circuit. It is the important part of computing devices start from portable devices to supercomputers and more than them. Particularly its role in miniature devices is an important one. The battery need for long battery back-up time for the miniature devices is a key issue which always increases the expectations of the users for more and more backup time. Hence the power consumed by multiplexers is a key factor to control. The multiplexer in a data path with more bits is replaced by 2-1 MUX as a tree is called *decomposition* [1]. There are different approaches followed for power optimization in a decomposed MUX tree [1]-[3]. They commonly aimed to reduce power consumption and increase speed. These papers have also investigated different approaches realizing MUX using CMOS pass transistor; each has its own pros and cons. There is the trade off exist between supply voltage, current, power, area and delay. Hence only some performance criteria are be able to meet at the same time.

Different approaches have been proposed to reduce power consumption of MUX trees. Some of the papers deal it at the algorithm level [1-3] and some at the circuit level [4-5]. An n-to-one MUX is transformed into an equivalent tree of two-to-one MUXes. There are various arrangements possible to build. But for power optimization it is required to use the proper MUX structure to do so. Even when power is available in non-portable applications, the issue of low-power design is becoming critical. This causes everyone to think about the careful design which ensures all the factors to be sacrificed rather than satisfied because of the trade off discussed a short while. It means that we need low power as well as speed for our design. In this paper the proposed style is compared with Static CMOS and Pass transistor (transmission gate) type of MUX structures.

The various technology considerations for the circuit design are discussed in Section 2 which gives an idea and leads to the choice of MUX structure. The available logic styles are to be discussed in at section 3. Section 4 describes about the power dissipation and its estimation in general. The implementation of the proposed pass transistor-static MUX structure is presented in section 5. The simulation setup is explained in section 6 which is used for all the three discussed styles of MUX structures. Section 7 covers the simulation results using 90nm CMOS technology library. Finally the work is concluded in section 8.

2 Technology Considerations

Various logic styles are available to use with their own advantages than the rest of the other styles but they are having different points of view. Evidently, they tend to favor one performance aspect at the expense of others. It is because of the tradeoff between the electrical parameters which are unable to satisfy at the same time. Hence a selected style appropriate for a specific function may not be suitable for another one. Choices between Static versus dynamic implementations, pass-gate versus Conventional CMOS logic styles and synchronous versus asynchronous timing are some of the options available to us. At another level, there are also various architectural/structural choices for implementing a given structure; In this section, the trade-offs with respect to low-power design between a selected set of circuit approaches will be introduced, followed by a discussion of some general issues and factors affecting the choice of logic family.

2.1 Circuit Design Parameters

In this subsection, the factors important to be considered for low-power design are described which lead to different kinds of circuit approaches. They give a clear idea about the low power MUX structure. They are basically from any of the three major logic styles which are static, dynamic and pass transistor designs. They are discussed in the following Sub-subsections.

2.1.1 Switching Activity

The power consumed by switching activity is considerably more and it varies among logic to logic. This is due to the variation in switching probability or on probability (whenever there is a state change from logic '0' to logic '1'). For example, if we take a NOR logic gate, the dynamic probability factor is 0.75, that is; $P_{NOR}= 0.75\ C_L V_{dd}^2 f_{clk}$. On the other hand, the activity factor for the static NOR gate will be only 3/16. These all are reported in [6].

2.1.2 Short Circuit Current

Considerable rise and fall time of the input resulting in a direct path exists between V_{dd} and GND. This happens whenever the input voltage falls between $V_{Tn} < V_{in} < V_{dd} - |V_{Tp}|$ and causes a conductive path between V_{dd} and GND. In such situations, both NMOS and PMOS devices are on. This is the case for static design and impossible in a Dynamic approach because the Pre-charge and Evaluation are not occurring at the same time [6]. The NMOS device current is given by the below expression

$$I = \beta/2(V_{in}- V_t)^2 \qquad for\ 0 < I < I_{max} \qquad (1)$$

Where, β is the gain factor, V_{in} is the input voltage, V_t is the threshold voltage and I_{max} is the maximum device current.

2.1.3 Parasitic Effects

It is related to the physical wiring of the circuit components of a chip or a module. Based on the length, width and height of the interconnect wire, the parasitic capacitance, resistance and inductance of the interconnections have a variation which affect the electrical property of any module [7]. Hence logic circuit with fewer transistors will have lower parasitic capacitance than the circuits with more CMOS devices.

2.1.4 Spurious Transitions

Spurious transitions are due to finite propagation delay from one logic block to the next logic in static designs. A node can have multiple transitions in a single clock cycle before settling to the correct logic level. The number of these extra transitions is a function of input patterns, internal state assignment in the logic design, delay skew, and logic depth. But Dynamic logic does not have this problem, since any node can undergo at most one power consuming transition per clock cycle.

2.1.5 Clock Gating

This is the common method to reduce power of a digital system in idle mode. Whenever a particular block or whole system is idle, the clock connection to that module is turned off which is also called gating technique. But this method does not reduce the sub-threshold leakage (the leakage current exists in the sub-threshold region during the device is off).

3 Available Logic Styles

The two major logic styles namely static logic and pass transistor MUX structures are to be discussed in this section. The Pros and Cons of each method are also described to get the clear picture of the importance of their own individuality.

3.1 Static MUX Structure

In this subsection the complementary CMOS style is presented as a kind of MUX structure with its own properties. It is the static style which has the combination of PMOS transistors as Pull Up Network (PUN) and NMOS transistors as Pull Down Network (PDN). The PUN connects the V_{dd} to output and the PDN makes the connection between V_{ss} and output. The two networks function in a mutually exclusive fashion [7]. Only one network is conducting in steady state. Hence the output is connected to V_{dd} or V_{ss} depends on the input pattern. Using this idea, the Static MUX is presented as illustrated in Figure 1.

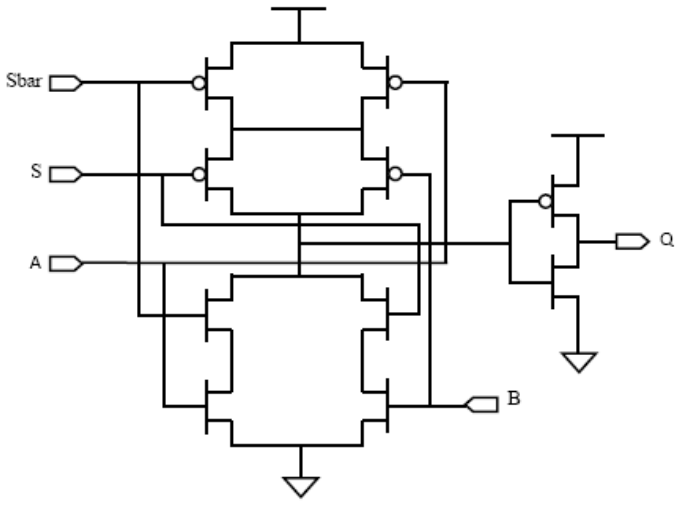

Fig.1. Complementary Static CMOS MUX

Compare to the other methods, this style is a robust design with full swing at its output. It is also a reliable design because of the static approach. It exhibits a rail-to-rail swing with $V_{OH} = V_{DD}$ and $V_{OL} = GND$. There is no static power consumption due to the mutually exclusive PDN and PUN.

The logic equation of any MUX structure in general is expressed in (2).

$$Q = Sbar.A + S.B \quad (2)$$

Where, Q is the output of the MUX, S is the selection input and A & B are data input signals.

To analyze the circuit efficiently, it is important to apply the input patterns such that they will cover all possible combinations and their output. It is discussed in section 6. Generally the static style has more current flow than that of pass transistor logic (CPL). Hence it has lower gate delay and the circuit propagates faster than that of the CPL. The gate delay as mentioned in [8] can be calculated as

$$t_{pd} \propto C_L V_{dd} / I_{DS} \quad (3)$$

Where, t_{pd} is the propagation delay, C_L is the load Capacitance, V_{dd} is the supply voltage and I_{DS} is the drain saturation current.

The other advantages of this method are no charge sharing problem and glitch free. Whereas the dynamic style and pass transistor methods are affected by these factors. Hence from (3) we can understand that the drawback of the static MUX structure when compared to Pass transistor style is the higher power usage.

3.2 Pass Transistor MUX Style

This is the Transmission Gate type of MUX structure implemented with very minimum transistors (4 MOS transistors) compare to the Complementary Static method which has 10 CMOS devices. The back to back connected PMOS & NMOS arrangement acts as a switch is so called Transmission Gate. NMOS devices pass a strong 0, but a weak 1, while PMOS pass a strong 1, but a weak 0. The Complementary Static CMOS use NMOS as pull down and PMOS as pull up. Whereas in the transmission gate, combines the best of both the properties by placing NMOS in parallel with the PMOS device. Two transmission gates are connected as in Figure 2 to form a MUX structure [7].

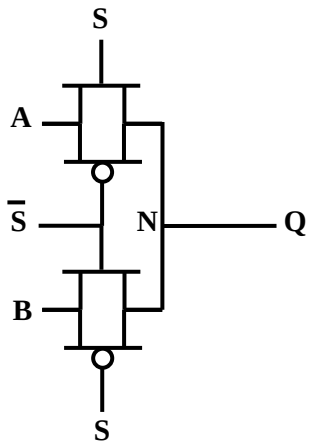

Fig.2. Transmission Gate MUX

Each the Transmission Gate acts as an AND switch to replace the AND logic gate which is used in a conventional gate design of MUX. Hence the device count is reduced to 4. One more change when compared to static method is that there is no supply voltage applied to the circuit. It results in less operating power. But the delay is more than the static style which is clear from (3).

4 Power Consumption

Any Digital CMOS circuit may have three major sources of power dissipation namely Dynamic, Short circuit and Leakage power. Hence the total power consumed by every MUX style can be estimated using the following equation:

$$P_{tot} = P_{dyn} + P_{sc} + P_{leak} = C_L V_{dd} V f_{Clk} + I_{SC} V_{dd} + I_{leak} V_{dd} \quad (4)$$

The first term P_{dyn} represents the switching component of power, the next component P_{sc} is the short circuit power and P_{leak} is the leakage power. Where, C_L is the loading capacitance, f_{Clk} is the clock frequency which is actually the probability of logic 0 to 1 transition occurs (the activity factor). V_{dd} is the supply voltage, V is the output voltage swing which is equal to V_{dd}; but, in some logic circuits, such as pass-transistor implementations, the voltage swing on some internal nodes may be slightly less [7].

The current I_{SC} in the second term is due to the direct-path short circuit current which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground [9]. Finally, leakage current I_{leak}, which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations. This current is very much negligible and hence in most of the estimations it is practically not accounted. The dominant terms in a "well-designed" circuit are the switching component, Supply voltage and short circuit current. Thus for low-power design the important task is to minimize C_L, V_{dd}, f_{Clk} while retaining the required functionality.

5 Proposed Pass transistor-Static MUX

Before address the proposed style, it is better to reveal the problem of the transmission gate MUX presented in Subsection 3.2 of this paper. The output section in a conventional gate MUX is an OR gate which is replaced by wired logic at the node named as 'N' in the transmission gate shown in Fig.2. This leads to the signal degradation and the functionality is not clear which is shown in Fig.3. The issue is distinct, when integrated in a tree like the structure reported in [10]. The circuit also causes more delay which is clearly understood from (3) which is because of the lower current flow.

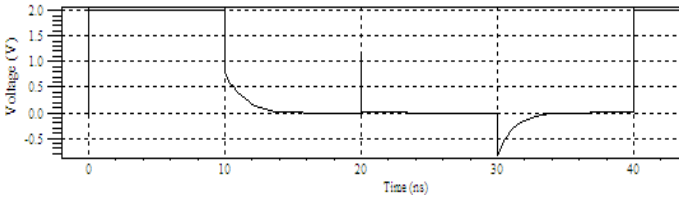

Fig.3. Output of the Transmission Gate MUX

For the circuits with more number of data bits, the tree requires more mux stages which results in more glitches. To avoid this, our proposed style gives the solution.

The idea is to eliminate the signal degradation problem caused by wired logic at node 'N' of Fig.2 and to improve the speed of the MUX along with low operating power. This is achieved by adding the best properties of Pass Transistor style and static method to form Hybrid kind of structure which has the transmission gates for the AND logic of the MUX and Static OR gate at the node 'N'. This new method is illustrated in Fig.4.

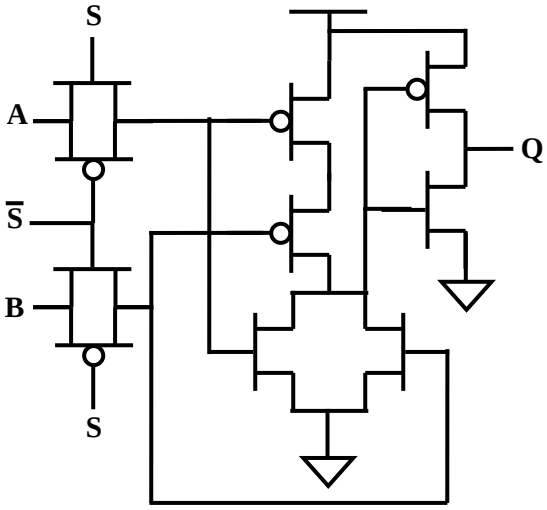

Fig.4. Pass transistor – Static MUX structure

The circuit seems to have the same amount of device count as the Complementary CMOS Static MUX with 10 transistors to build. Though the count is 2.5 times more than the transmission gate style, the power is saved to first half portion of the circuit and the delay is more for it. For the output section, the circuit is faster but the power is a bit more than the input section. This combination leads to compensate the power and speed at the same time which results in a better MUX style with a new property. For this style also the same simulation setup presented in Section 6 is used to test its efficiency.

6 Simulation Setup

We have performed the simulations using TSPICE in a 90nm technology. The simulation setup is shown in Fig.5 which is added with buffers at the inputs and output. This setup is used to measure the power and delay efficiently.

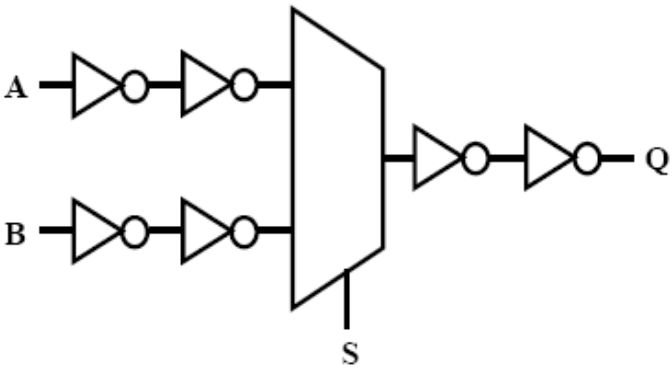

Fig.5. Simulation setup

The importance of including the effects and power consumption of the buffers connected at the inputs and outputs of the MUX cell come from the fact that the module is always going to be used in combination with other modules to build a larger system. So, the static inverters are a good generalization for any other modules to be considered.

Sizing methodology for the circuits incorporated the following steps:

a) Set all the N transistors to the minimum size. If there were *n* transistors connected in series, then the size for each transistor within the chain was modified to *n* times the original size.

b) Set all the P transistors to double the minimum size (to compensate for the mobility difference between N and P transistors). If there were *p* transistors connected in series, then the size for each transistor within the chain was modified to *p* times the original size.

c) Simulate the circuit with an input pattern to cover all input combinations.

d) Figure out the transition with the highest propagation delay, and resize the transistors involved in this critical path.

e) Repeat steps c) and d) until no longer improvement is attained for the propagation delay.

7 Simulation Results

Any circuit with the low voltage has the value of 0 volt and the high voltage possesses the value of V_{dd} at the output is terminologically called "full swing" circuit. The problem of signal degradation stated in Fig.3 is eliminated with the help of the proposed architecture. The input sets for simulation and their simulated output wave patterns are shown in fig.6. The table 1 lists the average power and delay of all the three type of MUXes.

Table 1
Simulation Results (power in nW and delay in nS)

($@V_{dd}$ = 2v)	Average Power	Delay
Complementary CMOS	25.98	153.96
Transmission Gate	17.02	235.29
Pass Transistor-Static	22.32	179.21

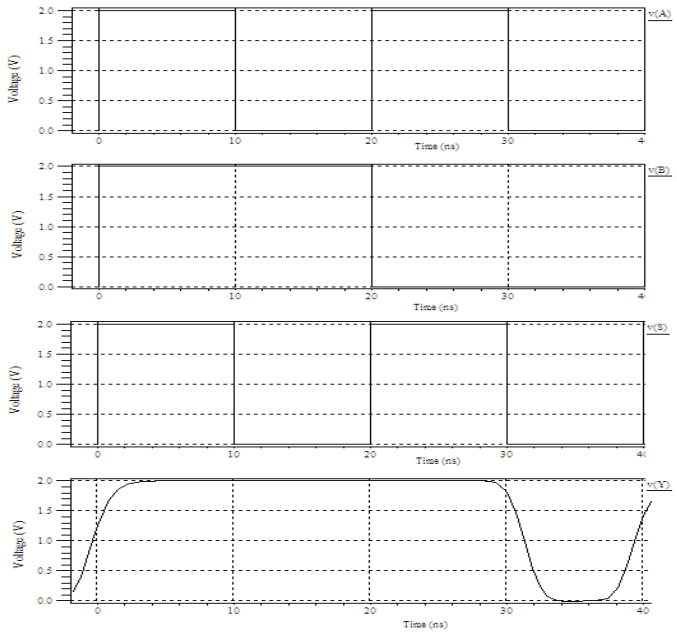

Fig.6.Simulation input patterns and output

From the waveforms of Fig.6 it is visible that the output sweeps to the full swing as discussed in this section. That is, the output swings between *GND* to V_{dd}.

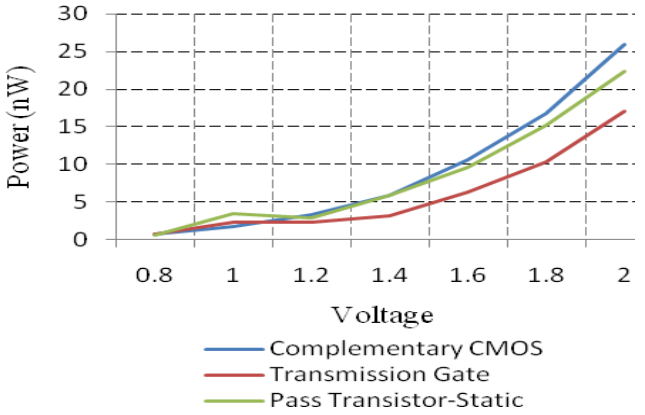

Fig.7. Average power Consumption Curves

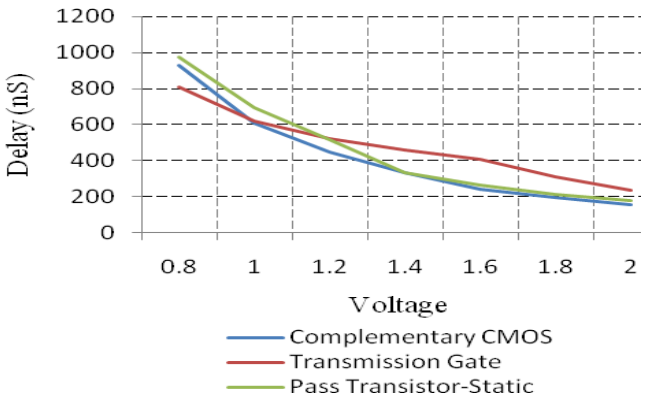

Fig.8. Delay curves

The average powers consumed by the discussed methods are shown in Fig.7 while the delay curves are illustrated in Fig.8. From them it is inferred that the proposed structure consumes moderate power with moderate delay. It means that instead of achieving high speed at the expense of power (or vice-versa) it is balanced to get the taste of better power and better speed than that of best and worst cases.

8 Conclusion

The complementary CMOS MUX, Transmission Gate MUX and Pass transistor-Static MUX styles have taken for comparison with the help of 90nm technology. From the first two types; either the power or delay is low and vice-versa to each other. But even the two properties are unable to be met at the same time, this new method proposes to get the properties of moderate power and delay at the same time. The signal degradation found in transmission gate MUX is also eliminated to ensure the full swing at the output. The new style can be implemented in a decomposed MUX tree as extension.

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