Novel Temperature Independent Ring Oscillator

MOHAMMAD HASSAN MONTASERI, HOSEI MIAR NAIMI
ECE Department
Babol University of Technology
Shariaty St, Babol, Mazandaran
IRAN
mh.montaseri@gmail.com

Abstract: - A novel temperature effect cancellation circuit is presented for ring oscillators. In the proposed circuit, the stages are the same, but the role of the devices is reversed. Experiments show that compared to the last competitive architectures, the proposed circuit is of important concern. The proposed architecture was simulated in 0.35µm CMOS technology where the temperature varied from 0 to 50 degrees Celsius, resulting in only 1% of frequency deviations.

Key-Words: - Voltage Controlled Oscillators, Ring Oscillators, Temperature Variations, Frequency Stability.

1 Introduction

High integration capability of ring oscillators has made them an integral part of many digital and analog systems [1]. These building blocks are used as beating heart of applications such as disk drive read channels [2], clock recovery circuits for serial data communications [3]. Stable frequency is imperative in order to minimize interference in adjacent frequency bands, as far as many communications applications are concerned [4].

The deviation of simple CMOS inverter's oscillation frequency is directly proportional to temperature and supply voltage variations [5, 6]. Lin and Huang [7] proposed a circuit that has very low sensitivity to variations of temperature. Lee and Kim [8] used high speed inverters to alleviate the undesired effects of temperature. Bandgap references were used to bias delay cells independent of both, temperature and supply voltage deviations [9-11]. In this research we have focused on a modified ring oscillator structure which has a more stable oscillation frequency with respect to temperature variations. Some simple evaluations showed that in some oscillators the oscillation frequency has a positive quadratic profile in terms of temperature variations with a minimum, shown in Fig. 9. This Fig. shows a reverse behaviour for oscillators with NMOS differential inverters. So the main idea is to combine these two, hopping to gain a temperature independent oscillator.

2 CMOS Ring VCO and Temperature Independent Architectures; A Brief Review

A ring oscillator is composed of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. Each delay stage must provide a phase shift of π/N, where N is the number of delay stages. The remaining π phase shift is provided by a dc inversion [5]. This means that for an oscillator with single-ended delay stages, an odd number of stages are necessary for the dc inversion. If differential delay stages are used, the ring can have an even number of stages if the feedback lines are swapped. Examples of these two circuits are shown in fig. 1.

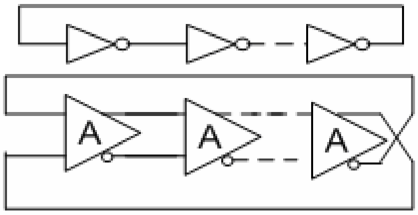


Fig. 1: Single-ended and differential-ended ring oscillators

There are several types of inverter stages by which a ring oscillator can be realized [10]. Among a variety of ROs, CMOS inverter, Maneatis cell, and Modified Lee-Kim structures are of great importance. For the rest of this section, the foregoing cells are reviewed.

2.1 Simple CMOS Inverter

The very first practical topology used as RO is CMOS inverter. Its schematic is drawn in fig.2 and its coordinate of frequency vs. temperature is shown in fig.3. This structure uses no precision mechanism against temperature variation. Therefore, temperature variation affects the behaviour of the circuit in a direct manner [6, 7].

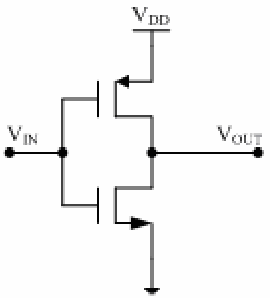


fig.2 simple CMOS inverter

In fig (3) it is shown that sensitivity of oscillation frequency with respect to power supply variations is approximately 0.008. In this structure if temperature varies by 10 percent, oscillation frequency deviates by 8 percent, which is intolerable.

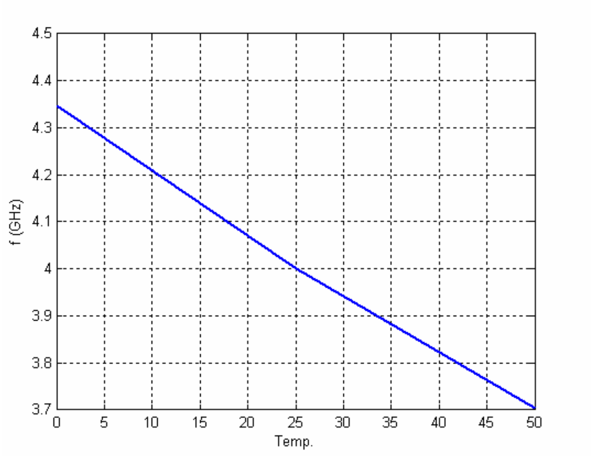


Fig.3 the effect of temperature variations on oscillation frequency

Simulations showed that in case of device scaling, sensitivity may change slightly. But variations were small enough to be ignored.

2.2 Maneatis Cell

Maneatis proposed to use differential Ring with symmetrical load like the one shown in fig.4. Apart from being completely symmetric, Maneatis used self-biasing concept. This way temperature, process, and any other deviations from desired frequency make the circuit back to the quiescent frequency.

This is achieved through a combination of three bias circuits; a voltage reference, a current reference, and the replica bias. These circuits are shown in figures 5, 6, 7 respectively. These building blocks are described in more detail in references [109], [111] and [113].

The voltage reference develops a ΔV_{be} mismatch across a fixed resistance to generate a PTAT current. This current is then drawn through another resistor attached to the supply to give a reference voltage of

$$V_{ref} = V_{DD} - \frac{KT}{q}.\ln(X).\frac{R_2}{R_1} \qquad (1)$$

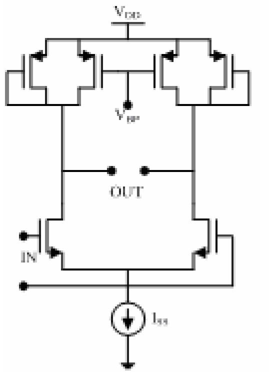


fig.4 Maneatis delay cell

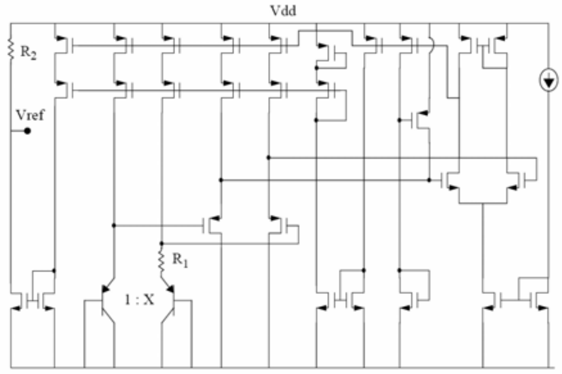


fig.5 Voltage reference generator

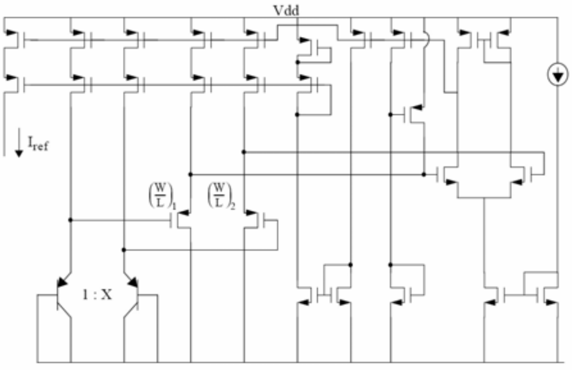


fig.6 Current reference generator

where X is the ratio of the PNP device sizes. This reference voltage is used in the replica bias circuit to set the nominal DC output swing. The swing is therefore proportional to absolute temperature and is insensitive to the power supply variations. It depends on a ratio of resistances, which match reasonably well over process variations, and to a ratio of device areas.

$$V_{SW} = \frac{KT}{q}.\ln(X).\frac{R_2}{R_1} \qquad (2)$$

The current reference uses a feedback loop match ΔV_{be} a mismatch in pair of bipolar devices to a $\Delta(V_{GS} - V_{th})$ mismatch in a pair of MOS devices.

The end result is a current that depends on the thermal voltage kT/q, device sizes, and device mobility.

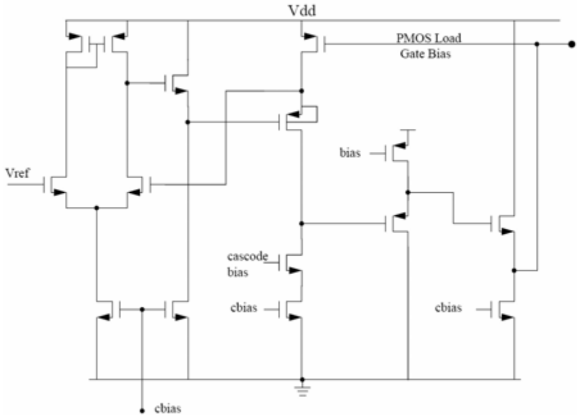


fig.7 Replica bias circuit

Including the effects of temperature on device mobility, this current has a net temperature dependence of somewhere between $T^{1/2}$ and T^1. Therefore, the time delay per stage has a net temperature dependence that is between $T^{1/2}$ and constant.

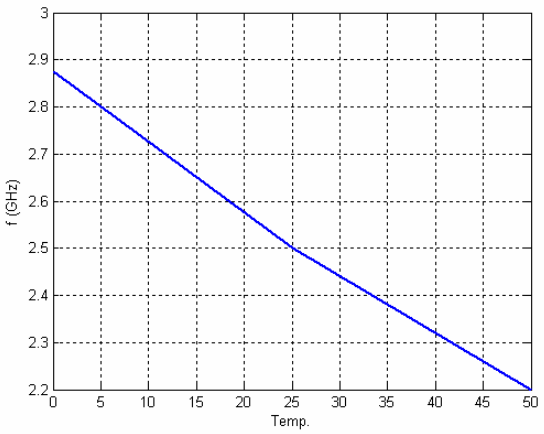


fig.8 effect of temperature variations on oscillation frequency of Maneatis cell

2.3 Modified Lee-Kim Cell

Using the method proposed by Lee-Kim and a little bit modification of the circuit results in the following structure which has been proved to be drastically independent of temperature variations.

The proposed delay cell, illustrated in figure 9, is based on a differential NMOS input pair with an active load. This load consists of a cross-coupled PMOS pair, connected to the control transistor, in parallel with two resistors directly connected to the supply voltage. The PMOS pair is equivalent to a negative resistance. While the gate voltage of the control MOS increases, the injected current decreases so the negative resistance becomes less negative. Then the total load resistance of the input pair increases, thereby lowering the frequency of the oscillation.

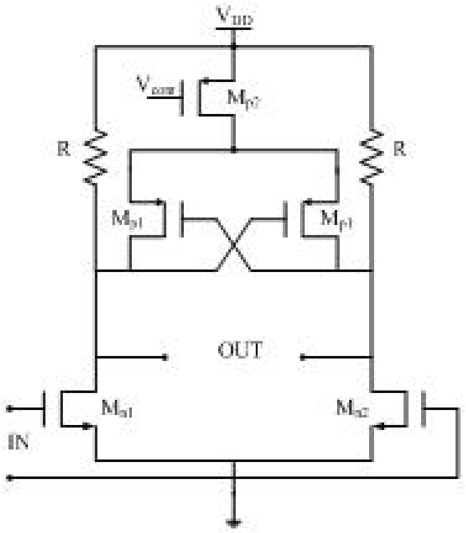


fig.9 modified Lee-Kim cell

Using the Barkhausen criteria, we obtain the oscillation frequency of the VCO [15]:

$$f = \frac{1}{2\pi}\sqrt{\frac{g^2{}_{mn1} - (1/R - g_{mp1})^2}{(C + C_{gdp1})^2 - C^2{}_{gsn1}}} \qquad (3)$$

According to frequency equation mentioned before, the oscillation frequency directly depends on the transconductance of the NMOS transistor Mn1 and the PMOS cross coupled one Mp1. Now, these two kinds of transistors have different temperature behavior. Indeed, according to the constant mobility model [16] expressed in (4), electron and hole mobility varies in temperature as:

$$\mu(T) = \mu_o \left(\frac{T}{T_o} \right)^{-1.5} \qquad (4)$$

As shown in equation 5, gmn(T) and gmp(T) depends both on the mobility and on the threshold voltage. Let us plot in the same graph the temperature behavior of each transconductance gmn1 and gmp1.

As shown in figure 4, each transconductance doesn’t exhibits the same variation in temperature. We can note here that the gm variation of the transistors Mn1 and Mp1 depends both on their own temperature dependence and on the variation versus temperature of the control current provided by Mp2-p4. Since the oscillation frequency is expressed as a function of the difference of gmnl and gmpl, the resulting output value presents significant temperature drift (1291ppm! 0 C).

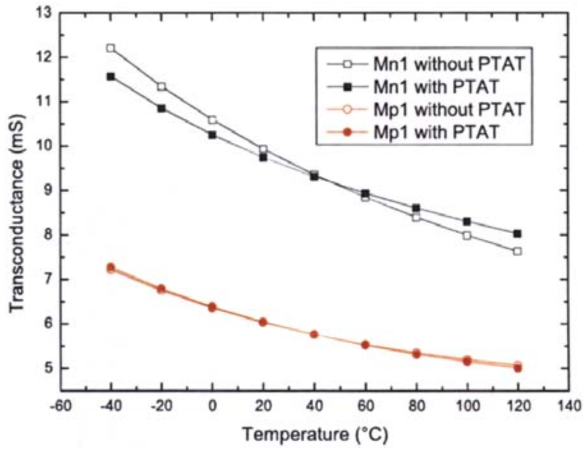


fig.10. The VCO transistors transconductance versus temperature

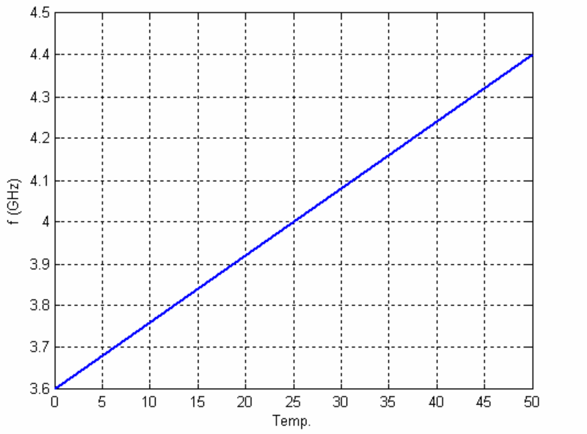


fig.11 frequency deviations vs. temperature variations for modified Lee-Kim delay cell

3 The proposed structure

As shown in Fig. 3, 8, 10, all structures output frequency suffers from temperature variations which doesn't meet most of telecommunication systems specifications and must be compensated for.

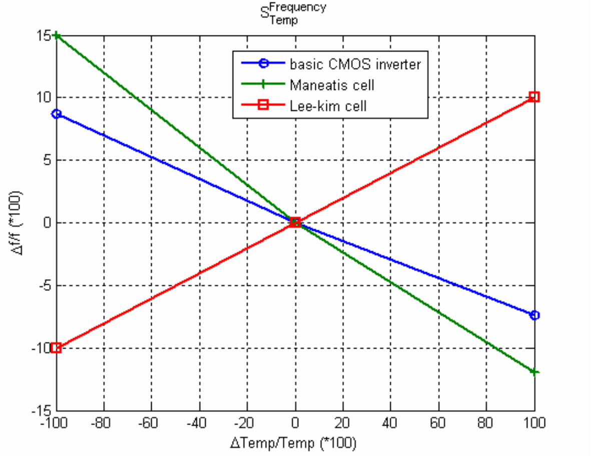
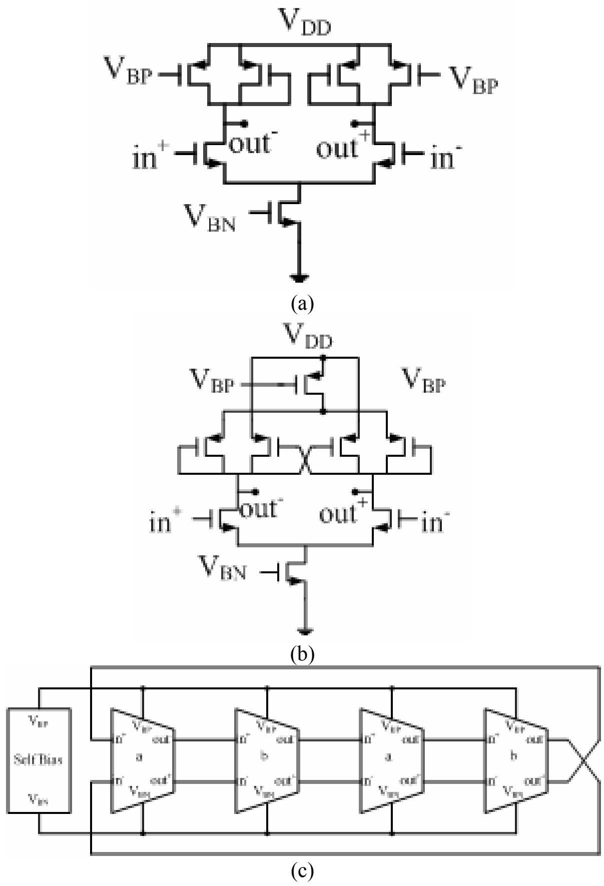


Fig.12 temperature behaviour of mentioned delay cells

By analysing curves, it is apparent that normalized frequency deviations in terms of temperature variations for Maneatis and Modified Lee-Kim cells change oppositely. From this, the idea is to make oscillators independent of temperature by combining the mentioned building blocks as a new oscillator. The definition of what was explained is sketched in the frame of temperature behaviour curves in Fig. 12. This figure gives some insight into behaviour of different delay stages. Most importantly is that of Maneatis and Lee-Kim. Taking into consideration the opposite slope characteristics of the relative frequency deviations in terms of temperature variations of the mentioned inverters , we can conclude that, it is reasonable to design a ring oscillator composed of cascade chain of inverters.

So based on the above idea and considering the profiles in fig. 12, the proposed structure is shown in fig 13. Since temperature behaviour of Maneatis and Lee-Kim cells differ only in sign, the proposed structure uses these structures in the loop for complete compensation. And to exactly eliminate the effect of each stage, even number of stages have been used.



(a)

(b)

(c)

Fig.13: The proposed ring oscillator structure

Our proposed structure is composed of four stages. Two of them are Maneatis cell and the other two are modified Lee-Kim cell. As mentioned before, since the desired cells behave oppositely with respect to temperature variations, these cells neutralize each other. Hence the total frequency deviation with respect to temperature variations is theoretically zero. Simulation results show that the proposed oscillator has a more stable frequency in terms of temperature variations than previous had, as shown in Fig. 15.

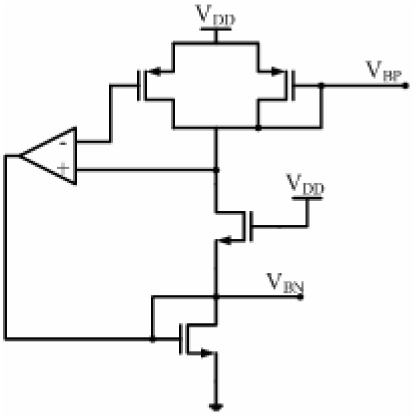


Fig. 14: Self-bias circuit

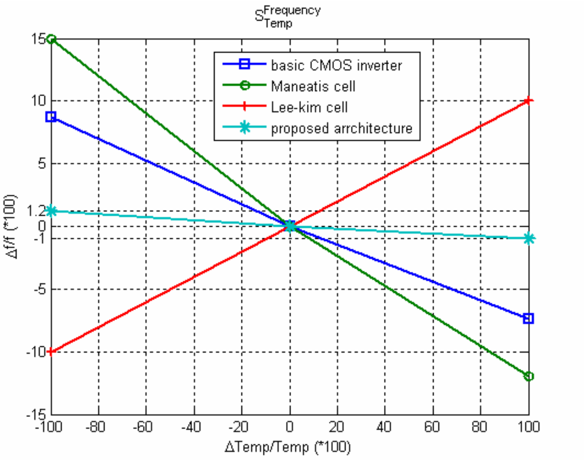


Fig. 15: Relative frequency deviations in terms of temperature variations of the ring

Simulations were performed in HSpice BSMI4 model. As mentioned in [phd] Maneatis cell has the property of reduced oscillation frequency characteristic. We have used (0.5/5) µm channel length/width for Maneatis cell to achieve higher frequencies. For the case of Lee-Kim cell the same dimensions as Maneatis cell were used. For CMOS inverter circuits (0.5/50) µm channel length/width has been used. During simulation, device dimensions kept constant, or else different characteristics would have been achieved.

Frequency variations were normalized to the center frequency of each ring oscillator to make comparison easier.

4 Conclusion

In this paper we considered dependency of different ring oscillators' output frequency upon temperature variations. Finally, simulation results showed that the proposed method increased the frequency stability of ring oscillator in terms of temperature variations. For more research we intend to derive analytical equation to descry.

References:

[1] A. Hajimiri, S. Limotyrakis, T. H. Lee, "Jitter and Phase Noise in ring oscillators," IEEE J. solid-state, vol. 34, NO.6, June 1999.

[2] M. Negahban, R. Behrasi, G. Tsang, H. Abouhossein, and G. Bouchaya, "A two-chip CMOS read channel for hard-disk drive," ISSCC Dig. Tech. papers, pp. 216-217,Feb. 1993.

[3] L. DeVioto, J. Newton, R. Croughwell, J. Bulzacchelli, and F. Benkley, "A 52 and155 MHz clock-recovery PLL," ISSCC Dig. Tech. papers, pp. 142-143, Feb. 1991.

[4] W. R. Braun, "short term frequency instability effects in networks of couple oscillators," IEEE Trans. Communications, vol. com-28, NO 8, Aug. 19980.

[5] G. S. Jovanović, and M. K. Stojčev, "A method for improvement stability of a CMOS voltage controlled ring oscillator," IEEE , published on web.

[6] B. Razavi. Analysis and Design of Analog CMOS integrated Circuits, NewYork, McGraw-Hill, 2001

[7] Z. M. Lin, K. C. Huang, J. D. Chen, and M. Y. Liao, "A CMOS voltage-controlled oscillator with temperature compensated," IEEE, ----.

[8] J. Lee, B. Kim, "A low-noise fast-lock phase-locked loop with adaptive bandwidth control," IEEE J. solid-state circuits, vol. 35, NO. 8, Aug. 2000.

[9] M. Mansuri, and C. K. K. Yang, "A low-power low-jitter adaptive-bandwidth PLL and clock buffer," IEEE Internationl solid state circuits conf., vol. 1, pp. 430-505, 2003.

[10] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased technique," IEEE JSSC , vol. 31, pp. 1723-1732, Nov. 1996.

[11] J. H. Haung, "PLL based multi-phases clock generator," Ph.D thesis, National central Univ., Taiwan, July 2005.

[12] B. Kim, "High Speed Clock Recovery in VLSI Using Hybrid Analog/Digital Techniques", Ph.D. Thesis, Memorandum No. UCB/ERL M90/50, Electronics Research Lab, U.C. Berkeley, 1990.

[13] D. Helman, "A Multi-phase clock generator/parallel-phase sampler in 1 micron CMOS: research project." MS Report, Department of Electrical Engineering and Computer Sciences, U.C. Berkeley, May 1990.

[14] S. Mehta, "Design of GigaHertz CMOS Prescalars", MS Thesis, U.C. Berkeley, May, 1997.

[15] G. Ning, C. Cong, "A Frequency Stabilization Circuit for The Voltage Controlled Ring Oscillator", IEEE ASI, AN: 9808301

[16] YS. Shyu, JC. Wu, "A Process and Temperature Compensated Ring Oscillator", ASICS, 1999. AP-ASIC 99. The first IEEE Asia Pasific Conference on 23-25 Aug. 1999, pp 283-289.