A Low Power Gate Level Full Adder Module

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Abstract—A standard cell based gate level synchronous full adder design is presented in this paper. The main highlight of the article is that the proposed full adder realization is found to be better in terms of power-delay product (PDP), even in comparison with the full adder element that has been made available as part of two commercial standard cell libraries viz. the high-speed 130nm Faraday (UMC) bulk CMOS process technology and the low V, but inherently power optimized 65nm STMicroelectronics bulk CMOS process. The fundamental ripple carry adder (RCA) topology is considered to demonstrate the power efficiency of our full adder module vis-à-vis many other recently proposed full adder module designs.

Keywords—Full adder, Semi-custom design, Low power design, Power-delay product.

I. INTRODUCTION

Integer addition forms an important facet of computer arithmetic and an adder module is fundamental to realize arithmetic circuits in hardware. In fact, addition was found to be the most frequently encountered operation amongst a set of real-time digital signal processing benchmarks [1]. Indeed, the adder module is the critical component found in a processor’s data path, which eventually determines its throughput, as it is present in the ALU. In addition, it is also widely used for address generation in case of cache or memory accesses.

A number of transistor level designs for the full adder have been published in literature: a representative list includes [2] – [10]. These might have been used for defining the full adder functionality as a cell in commercial standard cell libraries; however this only specifies a possibility with respect to cell libraries provided by industrial vendors. Hence, it would be interesting to compare the power/speed/area efficiency of novel full adder designs with the full adders made available as part of commercial cell libraries. This would serve the purpose of underlining the significance of new full adder realizations. In adherence to this approach, novel gate level full adder designs that report better speed performance in comparison with their library counterparts were discussed in our recent works [11] [12]. To the best of our knowledge, such a comparison has not been made in the earlier works and usually the comparison was restricted to the designs of the previously published works. This adds further value to the importance of this research work. In this article, our specific discussion is on the proposition of a new full adder design that exhibits lower power in comparison with their minimum sized library counterparts. This sort of comparison is justified owing to our adoption of minimum sized gates for constructing a power efficient full adder module by following a semi-custom design technique. In particular, the PDP characteristic of the proposed full adder is compared with a similar metric of the full adder cell, which has been made available as part of the 130nm UMC CMOS process [13] and the 65nm STMicroelectronics CMOS process [14]. Based on the simulation results obtained, it becomes evident that our proposed full adder is power efficient than the equivalent gates of the above CMOS standard cell libraries.

The structure of the remaining portion of this paper is as follows. Section 2 mentions our recently proposed delay efficient full adder designs [11] [12], followed by a description of the novel low power full adder block in Section 3. Section 4 discusses the simulation mechanism and presents the results corresponding to both the 130nm and 65nm CMOS processes. We finally make the concluding remarks in the next section.

II. PREVIOUS RELATED WORK

A. XAC Based Full Adder

The full adder design utilizing the XOR gate, AND gate and a complex gate (AO12 cell) of the cell library was referred to as the XAC based full adder in [11], shown in figure 1.

![XAC Based Full Adder](image)

Fig. 1. XAC based full adder realization

B. XOAC Based Full Adder

The full adder constructed using XOR, OR, AND and a complex gate of the cell library was identified as the XOAC based full adder in [12], which is depicted in figure 2. The reason for the lesser latency of this full adder compared to the earlier design is due to the reduced number of XOR gates. However, owing to the increased power dissipation attribute of a XOR3 gate over an XOR2 cell, the delay improvement is nevertheless attained at the expense of more power.
III. PROPOSED FULL ADDER DESIGN

The proposed low power full adder is labeled as the XIMC based full adder, as it utilizes an XOR gate, an inverter, a 2:1 multiplexer and a complex gate (AO22 cell) from the cell library. It is portrayed by figure 3. In the absence of a carry input (i.e. logic ‘0’), the sum output is determined by the logical inequality or mutual exclusiveness of the augend and addend bits. On the other hand, when there is an input carry, the sum output (Sum) is governed by the logical equivalence of the adder inputs viz. \(a\) and \(b\). When both the adder inputs assume logic ‘high’ state, the \(Cout\) signal outputs logic ‘high’, signifying the carry-generate condition. Otherwise, a carry output is produced based on the occurrence of the carry-propagate condition, which is signified by \((a \oplus b)\) being true.

IV. SIMULATION METHODOLOGY AND RESULTS

Firstly, all the individual full adder blocks were described using Verilog in a semi-custom style based on suitable minimum sized components of the respective cell libraries. Five types of adder modules were considered for analysis: i) conventional half adders based full adder realization, ii) full adder cell present in the library, iii) XAC based full adder, iv) XOAC based full adder and v) the proposed XIMC based full adder. Secondly, the full adder blocks were instantiated to form a 32-bit RCA that comprises a simple linear cascade. To maintain uniformity, the inputs of all the different adder implementations were configured with the drive strength of a minimum sized inverter of the corresponding cell library, while the outputs were made to possess FO-4 drive strength. The results mentioned in the tabular columns that follow, purely reflect the power, delay and area metrics of the combinatorial logic and do not account for any sequential components, thereby paving way for a legitimate comparison.

Functional simulation was done using Cadence NC-Verilog and timing and area evaluation were done within the Synopsys PrimeTime environment. Here, ‘timing’ refers to the maximum combinational data path delay and ‘area’ implies the total area occupancy of the non-regenerative logic, along with the provision of the automatic wire load selection feature. This enables appropriate estimated net parasitic to get included as part of the designs whilst performing the simulations. To estimate average power using Synopsys PrimeTime PX, the adders were fed with input sequences in accordance with the input profile of a simple combinational benchmark, \texttt{newcpu}, and the input patterns were fed at a frequency of 125MHz for the 130nm process and 250MHz for the 65nm process.

Firstly, the simulation results corresponding to the best case electrical specification of the 130nm UMC bulk CMOS process will be presented, which would be followed by the simulation results pertaining to a best case PVT corner of the low \(V_T\), 65nm STMicroelectronics CMOS process technology that has been inherently optimized for low power. Table I lists the critical path delay, adder area and total power dissipation of the various 32-bit RCA implementations, with the high-speed 130nm CMOS process as the target technology. The percentage figures mentioned in the 2nd column of the tabular column below signify the relative increase in average power parameter for all the other adders compared to the power consumption value of the XIMC based adder. It can be noticed that the proposed adder is efficient in comparison with even the library’s full adder cell in terms of both power and delay, with the former reporting a reduction in latency compared to the latter by a substantial margin of 22.9\%. Thus, there is no power-delay tradeoff involved for the former in comparison with the latter, which is not the case with our previously proposed full adder designs viz. XAC and XOAC based full adder realizations. This observation clearly corroborates the power advantage of the proposed XIMC based full adder.

Table II gives the power, delay and area parameters of the various adders corresponding to a high-speed corner of the 65nm CMOS process. Since the library is inherently optimized for low power, the XIMC based full adder does not exhibit reduced average power, but only comparable dissipation with respect to the library cell based RCA. But in terms of critical path delay, the former is found to be beneficial leading to a speed improvement of 7.6\% over the latter.

![Diagram](image-url)
Table II

<table>
<thead>
<tr>
<th>Full adder type</th>
<th>Total Power (µW)</th>
<th>Delay (ns)</th>
<th>Area (µm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Half adder based</td>
<td>146.24</td>
<td>1.96</td>
<td>532.48</td>
</tr>
<tr>
<td>Library based</td>
<td>111.58</td>
<td>1.69</td>
<td>299.52</td>
</tr>
<tr>
<td>XAC based</td>
<td>148.37</td>
<td>1.30</td>
<td>465.92</td>
</tr>
<tr>
<td>XOAC based</td>
<td>183.98</td>
<td>1.20</td>
<td>549.12</td>
</tr>
<tr>
<td>XIMC based</td>
<td>115.67</td>
<td>1.57</td>
<td>449.28</td>
</tr>
</tbody>
</table>

The following diagrams highlight the PDP parameter for the various 32-bit RCAs corresponding to the 130nm and 65nm CMOS processes respectively. It can be seen that the proposed full adder features reduced PDP in comparison with the library based full adder, effecting corresponding savings to the tune of 27.2% for the 130nm CMOS process and 3.7% with respect to the 65nm process technology.

![Fig. 4. Power-delay product corresponding to 130nm CMOS process](image)

![Fig. 5. Power-delay product pertaining to 65nm CMOS process](image)

V. CONCLUSION

A novel full adder design was presented in this article. In order to demonstrate the low power advantage enjoyed by the proposed full adder, simulations were performed targeting two commercial standard cell libraries viz. 130nm and 65nm CMOS processes. It is usually customary to target the low speed corner of a cell library, as it would benefit in terms of reduced power consumption owing to minimal supply voltage requirement. However, in order to comment upon the delay metric as well simultaneously, a high-speed corner was chosen for simulation purpose. This also enabled us to study the average power dissipation characteristic of the various full adder modules, as incorporated into a typical carry propagate adder architecture, for a similar, reasonably higher operating frequency. On an average, it was found that the proposed XIMC based full adder achieved a lower PDP in a fair comparison with library based full adders by a considerable value of approximately 16%, based on our experimentations. Future work would deal with the proposition of an energy efficient full adder design.

REFERENCES


