Analysis of the Sensibility of Switched-Capacitor Resonators at Base Band in Single-Bit High-Order $\Sigma\Delta$ Modulators.

J. J. OCAMPO-HIDALGO
Departamento de Electrónica, Universidad Autónoma Metropolitana, Unidad Azcapotzalco.
jjoh@correo.azc.uam.mx

C. AVILÉS-CRUZ
Departamento de Electrónica, Universidad Autónoma Metropolitana, Unidad Azcapotzalco.
caviles@correo.azc.uam.mx

A. FERREYRA-RAMIREZ
Departamento de Electrónica, Universidad Autónoma Metropolitana, Unidad Azcapotzalco.
fra@correo.azc.uam.mx

I. VAZQUEZ-ALVAREZ
Departamento de Electrónica, Universidad Autónoma Metropolitana, Unidad Azcapotzalco.
iva@correo.azc.uam.mx

Abstract: - In order to improve both resolution and stability of single bit high order Sigma-Delta Modulators, quantization noise suppression should be carried out not only at DC but also within the bandwidth of interest. This noise suppression at frequencies different from zero is carried out with the use of resonators. Switched-Capacitor resonators at $f_S/n$ can be designed using integrating or delaying elements. In this work, both resonator structures are analyzed with respect to their robustness against the main imperfections presented in a SC implementation. The effect introduced by the operational transconductance amplifiers non-idealities was analyzed together with the effect of capacitor mismatch.

Key-Words: Analog-digital Conversion, Switched Capacitor Circuits, Sigma-Delta modulation.

1 Introduction
Oversampled A/D converters with noise shaping have become very popular in the last years. They are preferred for high resolution A/D conversion in digital audio, instrumentation and communications. Its circuit implementation is very robust; therefore, they are good candidates to be implemented in deep sub-micrometric and nano-metric CMOS technologies. In the mobile communications scenario, an A/D converter able to reach high values of signal-to-noise ratio (SNR) by using modest oversampling ratios ($OSR$’s) is needed. Another characteristic that should be exhibited by the converter is flexibility, since it has to work in a multi mode environment handling with different intermediate frequencies, channel bandwidths and modulation techniques. Single Bit High Order sigma-delta Loops (SDM) appear to be good candidates to full fill the mentioned needs. They are able to achieve high values of SNR for low $OSR$’s and their circuit implementation is very robust. They also have the interesting characteristic of synthesizing different types of noise transfer functions ($NTF$) by changing the filter loop coefficients without altering the structure of the modulator. In order to improve both resolution and stability of single bit high order SDM’s, quantization noise suppression should be carried out not only at DC but also within the band of interest. This noise suppression at frequencies different from zero is carried out with the use of resonators. Switched Capacitor (SC) resonators at an arbitrary fraction of the sampling frequency ($f_S/n$) can be designed using integrating or delaying elements [1,2,3,4]. In this work, both resonator structures were analyzed with respect to their robustness against the main imperfections presented in a SC implementation. The effect introduced by the operational transconductance amplifiers (OTA’s) non idealities was analyzed.
together with the effect of capacitor mismatch. Due to their importance in the design of bandpass SDM’s, there has been a great interest in analyzing the different existing structures to synthesize resonators at frequencies around $f_S/4$ [5,6], but this is not the case for resonators at frequencies different from one quarter of $f_S$. However, resonators at $f_S/n$ are important for the digitization of wide band signals in current and future wireless communications systems because its conversion is easier to accomplish at baseband or low Intermediate Frequency (IF) than at high IF values situated around $f_S/4$. The conducted study shows the superior performance of the integrator based resonator over delay based structures. The robustness exhibited by this resonator at frequencies within baseband makes it a good candidate for the implementation of wide band ADC’s whose OTA’s encompass moderate voltage gain and a unity gain frequency around four times $f_S$. Such values are not very difficult to reach in current sub micrometric technologies using well known single stage OTA topologies.

The paper is organized as follows, in the next section, both resonators are presented together with the developed models to study the impact of the circuit impairments under question. Section number three shows the simulation results and the comparison. Finally, in section number four some conclusions are given.

2 SC Resonators at $f_S/n$.

A widely used topology of a high order single bit SDM is shown in figure 1 [7]. This SDM Architecture with cascaded elements and feed forward coefficients has the following signal- and noise transfer functions:

$$STF(z) = \frac{\sum_{i=1}^{n} b_i H_i(z)}{1 + \sum_{i=1}^{n} b_i H_i(z) \prod_{i=2}^{n} H_{i-i}(z)}$$

$$NTF(z) = \frac{1}{1 + \sum_{i=1}^{n} b_i H_i(z) \prod_{i=2}^{n} H_{i-i}(z)}$$

If functions $H_i(z)$ have poles and zeros of the form $H(z) = z_i/p_i$ where: $z_i = (z\text{-}zero_i)$ and $p_i = (z\text{-}pole_i)$, equation 2 can be expressed as:

$$NTF(z) = \frac{(z - pole_1)(z - pole_2)\cdots(z - pole_{n})}{p_1 p_2 \cdots p_n + b_1 z_1 p_2 \cdots p_n + b_2 z_2 \cdots p_n + \cdots + b_{n-1} z_{n-1} \cdots p_n + b_n z_n}$$

Equation 3 shows how the poles of the elements present in the forward chain of the architecture set the zeros of the noise shaping function. As mentioned, resonators are used if the poles of an element have to be placed at certain frequency. The literature reports mainly two structures for the design of SC resonators at $f_S/n$ namely, The Integrator Based Resonator [1,2] and The Delay Based Resonator [3,4]. These two structures are going to be presented in this section. A detailed analysis of their robustness against the main OTA non-idealities is also carried out.

2.1.- Integrator Based Resonator: A system level diagram of a SC integrator-based resonator is presented in figure 2. There, the classical lossless discrete integrator structure can be recognized. This arrangement has been used in both BP and LP SDM realizations [8,9]. The transfer function of this configuration is given by:

$$H(z) = \frac{z^{-1}}{1 + (g-2)z^{-1} + z^{-2}}$$

Eq. (4) puts two poles located at the normalized frequency ($\omega_n$) value:

$$\omega_n = \pm \cos^{-1}\left(\frac{2 - g}{2}\right)$$

As it can be observed, parameter $g$, which in turn becomes a capacitor ratio, is used to fix the desired resonant frequency, in principle at any angle ranging from 0 to $\pi$ inside the unitary circle. This has been used by designers to suppress the quantization noise both, at $f_S/4$ or near base band. It is well known that...
the characteristics of real operational amplifiers used in the realization of this resonator cause deviations from this ideal model. Those effects have been subject of extensive research, when this construction is used to implement resonators at $fs/4$. It is not the case for resonators at $fs/n$, useful to reduce quantization noise at base band. Moreover, there is another structure that uses delay elements to create resonators both at $fs/4$ or $fs/n$ which analysis has been ignored, up to the point of writing this work, when used to synthesize resonators at $fs/n$. Next, the mentioned construction is presented.

### 2.2.- Delay Based Resonator:

Proposed in 1991 by Horrocks [3], an arrangement based on delay cells, and capable to produce resonant peaks at different normalized frequencies is presented in the next figure. This resonator has a transfer function from $x(z)$ to $y(z)$ equal to:

$$ H(z) = \frac{g_2 z^{-1} + z^{-2}}{1 - g_1 z^{-1} + z^{-2}} $$

(6)

from (5.19), if $g_1=g_2=0$ the transfer function collapses to $z^2/(1+z^2)$, which is the transfer function of a resonator at $fs/4$. This is in fact a very often used form to synthesize resonant elements at one quarter of the sampling frequency, that has been deeply analyzed because of that interesting and useful property for IF digitization [10],[11]. Horrocks used the same structure for resonators at 0.1$fs$. Later [4], the usage of this array was proposed to produce resonators at 0.0718$fs$ and 0.4282$fs$. There is however a lack of analysis of the sensitivity of this resonator to the imperfections of its SC implementation, when it produces frequencies different from that at $fs/4$, as well as a comparison with the classical integrator based construction used also at $fs/n$. From (6) if $g_2=1$ and the output is taken from the point marked as $v$ in figure 3 it can be shown that the transfer function becomes:

$$ H(z) = \frac{z^{-1}}{1-g_1 z^{-1} + z^{-2}} $$

(7)

Thus, a delay based resonator at $fs/n$, whose central frequency is controlled by a single parameter $g_1$ is shown in figure 4. This resonator has also two complex conjugated poles of radius 1, positioned at normalized frequencies given by:

$$ \omega_n = \pm \cos^{-1}\left(\frac{g_1}{2}\right) $$

(8)

This permits to fix the resonant frequency at any angle between 0 and $\pi$ as well. In order to analyze the effects produced by operational amplifier non-idealities over these pair of resonators, the SC implementation of their building blocks, namely a SC integrator an a SC delay element is going to be reviewed. In the next discussion as well as in the remaining of this work it is assumed that every operational amplifier present in the implementation is an operational transconductance amplifier (OTA). The impairments that will be considered are finite voltage gain ($A_V$), non zero input capacitance ($C_{in}$), finite unity gain frequency ($f_u$) and capacitor mismatch. For the sake of simplicity, their effects were considered separately following an analysis method similar as that found in [13].

### 2.3.- SC Integrator:

The classical non-inverting delayed integrator is exposed in figure 5. The switches are controlled by a two-phase non-overlapping clock generator as shown in the same picture. If it is assumed that the OTA is ideal, it is well known that the transfer function of this circuit is given by:

$$ H(z) = \frac{C_1}{C_2} \frac{z^{-1}}{1 - z^{-1}} $$

(8)

If the OTA used in the integrator is real with finite $A_V$ and non-zero $C_{in}$, when $f_2$ is on, the OTA is connected as depicted in figure 6 and a voltage different from zero appears at node $n$ as indicated in that figure. It can be shown that, the ideal transfer function given in 8 transforms in:
where:

\[
\beta = \frac{C_z}{C_1 + C_2 + C_{in}}
\]  

(12)

If such an integrator is used in the loop of figure 2, a resonator with the following transfer function is constructed:

\[
H(z) = \frac{C_1 \varepsilon_1 z^{-1}}{C_2 (1 - \varepsilon_d z^{-1})}
\]  

(9)

where:

\[
\varepsilon_n = \frac{A_1 \beta}{1 + A_1 \beta}
\]  

(10)

and

\[
\varepsilon_d = \beta \frac{1 + A_1}{1 + A_1 \beta}
\]  

(11)

\[
\beta = \frac{C_2}{C_1 + C_2 + C_{in}}
\]  

(12)

The transfer function of the integrator is:

\[
H(z) = \frac{C_1 (1 - \varepsilon \delta z^{-1})}{C_2 (1 - z^{-1})}
\]  

(14)

Here, the gain error term is:

\[
\varepsilon \delta = e^{-2\pi\beta \delta T_S}
\]  

(15)

Here, \(T_S\) is the time allotted for settling and \(1/2\pi f_u\beta\) is the closed-loop time constant of the integrator. Thus, when this integrator is plugged into the lossless discrete integrator (LDI) loop, the following transfer function is obtained:

\[
H(z) = \frac{z^{-1}(1 - \varepsilon_1 - \varepsilon_2 z^{-1} + \varepsilon_2 z^{-2})}{1 - (g_1 (1 + \varepsilon_1) + \varepsilon_2 - \varepsilon_2 z^{-1} - \varepsilon_2 z^{-2}) - 2z^{-1} + z^{-2}}
\]  

(16)

Here, \(\varepsilon_1\) and \(\varepsilon_2\) refer to the errors introduced by the first and second integrator, respectively. At this point, it is convenient to thin off the SC implementation of the LDI loop. When \(f_1\) is active the first OTA has connected at its input the capacitor needed to implement the feedback coefficient, when computing itself as an integrator gain error [13]. In this case, the transfer function of the integrator is:
the value of $\beta_1$ this capacitor comes into the denominator and lowers it, making the effect of $\epsilon_1$ stronger. However, from equation 5 the required capacitor ratio to implement this coefficient must have a relation of $24.63 \times 10^{-3}$. With a capacitor of 1pF as $C_1$ and $C_2$ this factor produces a capacitance of $24.63 \times 10^{-3}$. The value of $C_{in}$ was chosen to be 80fF as typical for wide transistors working in saturation with a channel length of 0.3μm. Thus, the $\beta$ value of each OTA present in the implementation is given by:

$$\beta_1 = \frac{C_2}{C_1 + C_2 + C_{in} + C_g} = 0.475$$

$$\beta_2 = \frac{C_2}{C_1 + C_2 + C_{in}} = 0.480$$

These parameters indicate that, the reduction in $\beta_1$ is about 1.0% with respect to that of $\beta_2$, this allowed to use the same values of $f_u$ for both OTA’s in the simulations of the model given in equation 5.26 and performed with MIDAS. Simulation results are given in figure 8.

The last non-ideal effect examined for this resonator was capacitor mismatch. SC circuits are very robust against variations in the absolute value of their required capacitances, because their parameters are controlled by capacitor ratios, rather than the values of a single element. For this reason the values observed in the deviation of the resonant frequency in the next results are very small, however this is also a metric that should be considered when looking for the best alternative presented for the implementation of a high performance SC system. To evaluate the sensitivity to capacitor mismatch owned by this pair of circuits, Montecarlo simulations were conducted using the CADENCE environment. In order to look for a closed value in the resonant frequency, a clock frequency of 160 MHz was used in the simulations. This produces a resonant peak at 4MHz if the factor of 0.025 times $f_s$ is maintained. Figure 9 shows the resulting histogram of the central frequency after 1000 Montecarlo simulations applied to a periodic AC analysis (PAC) in the SpectreRF simulator. The obtained mean frequency value was 4.0192 MHz and the standard deviation was found as 10.0942 kHz. The models used in the simulation were provided by EUROPRACTICE for the technology AMS035.

2.4.- SC Delay Element: A single-capacitor sample and hold circuit that adds a delay to the input signal is presented in figure 10. If the circuit is constructed with ideal elements, the transfer function is given by:

$$H(z) = z^{-1}$$

(17)

In the single-capacitor sample and hold circuit, finite

$$H(z) = \delta z^{-1}$$

(18)

where:
\[
\delta = \frac{A_v \beta}{1 + A_v \beta}
\]

\[
\beta = \frac{C_s}{C_s + C_{in}}
\]

If this circuit is embedded in the loop of figure 4, the transfer function of a delay based resonator whose OTA’s have finite \(A_v\) and non-zero \(C_{in}\) turns in:

\[
H(z) = \frac{\delta z^{-1}}{1 - \delta g_1 z^{-1} + \delta_2 z^{-2}}
\]

After equation (21) it can be concluded that the effects of limited voltage gain and input capacitance different of zero in the two-delay loop are similar as in the LDI loop. Here \(Q\) degradation and deviation of the resonant frequency is observed as well. The model given in the last equation was also used in simulations performed with \textit{MIDAS} for the same values of voltage gain as in the LDI loop and the same resonant frequency. These results are shown in figure 11. It is useful to compare equations (21) and (13). In (13) terms \(e_{d1,2}\) lead to a partial cancellation of the error introduced by \(e_{m1,2}\). This is not the case in the last equation, where the deviation of the central frequency given by the coefficient of \(z^{-1}\) directly affects the parameter \(g_1\) with no cancellation. This in part explains the large deviation experimented by the central frequency and displayed in figure 11.

Another source of error in the delay cell is incomplete settling of the op. amp. due to finite \(f_u\). Finite gain-bandwidth product of the OTA’s used in figure 4 introduces a gain error in the sample and hold circuit given by:

\[
H(z)_m = (1-\gamma)z^{-1}
\]

where the gain error term \(\gamma\) is given by:

\[
\gamma = e^{-2\pi f_u T_s}
\]

Thus, when a band-limited OTA is used in a delay based resonator loop the actual transfer function becomes:

\[
H(z) = \frac{z^{-1}(1-\gamma_1)}{1-[g_1(\gamma_1-1)]z^{-1}+(\gamma_1\gamma_2-\gamma_1-\gamma_2)z^{-2}}
\]

Finite \(f_u\) introduces degradation both in the \(Q\) factor of the resonator as well as in the resulting resonant frequency. With help of \textit{MIDAS}, the last model was simulated for different values of \(f_u\), the results can be seen in picture 12. The values used for \(f_u\) were different for every OTA present in the implementation. They were taken to fix the curves in the window. As observed the required value of \(f_u\) is on the order of three to 2 times bigger in order to maintain reasonable deviations of the central frequency. This is a direct consequence of the reduction experimented by \(\beta\) in the SC implementation as discussed before. The much bigger value of the capacitor required to fix the frequency, lowering the value of \(\beta\), would require a very high current if the displayed values of \(f_u\) should be reached. This in turn conducts to contradictory demands if a high voltage gain should be maintained in that OTA. Thus, the design of the input OTA in a delay based resonator presents a very difficult constraint.

Finally the effect of capacitor mismatch is discussed. Here, as the only parameter controlling the position of the poles of the resonator is \(g_1\), variations in this

![Fig. 11. Effect of \(A_v\) and \(C_{in}\) in a delay based resonator.](image1)

![Fig. 12. Effect of \(f_u\) in a delay based resonator.](image2)
capacitor directly translate in changes of the resonant frequency. The Montecarlo simulation results for the system of figure 4 are presented in the histogram depicted in figure 13. From 1000 Montecarlo simulations the following results were obtained: Mean at 3.99296MHz, standard deviation: 78.6143kHz.

3 Conclusion

In this work, two SC resonators at f_s/n aimed to accomplish noise suppression at baseband in high order single bit SDM’s were presented and analyzed. The conducted study shows the superior performance of the integrator-based resonator over delay-based structures. As mentioned, up to the moment of writing this thesis such an analysis for SC resonators at f_s/n was not found in the literature. The sensitivity displayed by the LDI loop with respect to f_o is not very satisfactory, this gives an open field for research since digitization of wide-band signals is of great importance for up-coming communication services. The use of N-Path techniques should be reviewed for implementing resonators at frequencies f_s/n. Such techniques were not reviewed in this work because of the resulting extension of the paper.

References: