Modified Sigma-Delta Converter and Flip-Flop Circuits Used for Capacitance Measuring

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Abstract: - The paper brings new information about small capacitance measuring system based on modified sigma-delta converter (MSDC) with compensated loop based on phase locked loop (PLL). The system use of the 2 current sources and can be modified for other electrical or non-electrical quantity which will break the value symmetry in circuit, e.g. light intensity can be also measured with photodiode connected parallel to current source. Measuring system can work in open loop (direct sigma-delta converter) or closed loop (PLL). The system has the voltage and digital output and in closed loop can be supposed as a voltage controlled oscillator which is locked to input clock frequency. The simple flip-flop sensor for capacitance, or some other measuring is also described. In this paper, theoretical principle of the system, simulation and experimental results are shown.

Key-Words: Capacitance, measuring, phase locked loop, oscillator, sigma-delta converter, flip-flop sensor.

1 Introduction
Electronic systems for capacitance measuring are usually based on principle which transformed capacitance into an active electrical parameter, such as voltage, current or frequency. Transformation of capacitance into a voltage is typical for bridge methods. An oscillator system may be used as a transducer capacitance into frequency. In this case is measured a frequency change. However, in small capacitive change will reflect into small frequency change and the practical usage of this method is limited if capacitance is within the range a few pF.

Another method is based on principle that capacitance is measured as changes the time constant of a derivative element and by this way is also changed a filtered DC component. However, this method is relatively inaccurate therefore can be really used only for informative measurement. Summarizing properties of the above mentioned methods it follows that low-cost are suitable only for measurement capacitances within the range up to a few nF. Precise measurement systems can measure capacitances within the range up to a few pF however the problem is their relatively high cost. The aim of this paper is to show a new simple method for measurement capacitances within the range a few pF.

2 Principle of measuring system
The block diagram of the Σ-∆ (sigma-delta) measuring system with compensating loop is shown in Fig. 1. When the switch (closed/open loop) is open, the system work as conventional Σ-∆ converter [1, 2, 3, 4, 5, 6, 7].

![Block diagram of MSDC measuring system](image)

**Fig. 1.** Block diagram of MSDC measuring system. C1 - measured capacitance, C2 – fixed capacitance, Co1; Co2 - comparators, CLK - stable clock, PD - phase detector, LP - lowpass filter, i1 - fixed current source, i2 - voltage controlled current source, S1; S2 - switches.

Voltage on C1 is given (for \( i_1 = \text{constant} \)) by (1):

\[
V_{C1}(k) = \frac{1}{C_1} i_1 T_{CLK} + V_{C2}(k-1)
\]

and voltage on C2 is given by (2):

\[
V_{C2}(k) = \frac{1}{C_2} i_2 n T_{CLK} + V_{C1}(k-1)
\]

where \( T_{CLK} \) is clock period and \( n \) is integer value. For \( C_1 < C_2 \) is given by (3):

\[
n = \text{ceil}(C_1/C_2)
\]
where \( \text{ceil}(x) \) converts a numeric value to an integer by returning the smallest integer greater than or equal to its argument. E.g. \( \text{ceil}(9/3) = 3 \), but \( \text{ceil}(9.01/3) = 4 \).

When the switch (closed/open loop) is closed, the system works as a phase locked loop. In this case, the different values of \( C_1 \) and \( C_2 \) are compensated for the changing of \( i_2 \). It is important to note, that for equally spaced output pulses (system used as oscillator), additional pulses are generated by control logic.

It is important to note, that instead of variable \( C_i \), variable can be used \( i_1 \), or constant \( i_1 \) and variable current source in parallel with \( i_1 \) e.g. photodiode for light intensity measurement.

**Fig. 2. a) The MSDC simplified block diagram (only \( C_1 \) is affected) is equivalent to conventional \( \Sigma-\Delta \) converter, b) with zero input voltage and different reference values of voltage sources \( \pm V_{r1}, \pm V_{r2} \). Int - integrator, Comp - clocked comparator.**

**Fig. 3. \( \Sigma-\Delta \) converter with zero input voltage and different reference values of voltage sources (Fig. 2 b)) is equivalent to \( \Sigma-\Delta \) converter with the bias input voltage \( V_B \) and \( \pm V_{re} \) reference voltage.**

**3 Output frequency determination**

For evaluation of MSDC output frequency (in open loop), the equivalent circuit scheme was derived. It can be derived, that for MSDC with \( C_1 \) is changed, equivalent conventional \( \Sigma-\Delta \) converter with zero input voltage and different reference values of voltage sources can be used (Fig. 2 a) and b)) and this converter (Fig. 2 b)) is equivalent to \( \Sigma-\Delta \) converter with input bias voltage \( V_B \) and \( \pm V_{re} \) reference voltage (equivalent reference voltage). Equivalent reference voltage \( V_{re} \) is given by:

\[
V_{re} = \frac{|V_{r1}| + |V_{r2}|}{2} = \frac{C_1 + C_2}{2} \tag{4}
\]

and input bias voltage \( V_B \) is:

\[
V_B = \frac{|V_{r1}| - |V_{r2}|}{2} = \frac{C_1 - C_2}{2} \tag{5}
\]

where \( V_{r1} > V_{r2} \) and \( C_1 > C_2 \). Output frequency for equivalent \( \Sigma-\Delta \) converter with input bias voltage \( V_B \) and \( \pm V_{re} \) reference voltage is given by (6):

\[
f_O = \frac{f_{CLK} (1 - V_B / V_{re})}{2} \quad \text{[Hz, V]} \tag{6}
\]

After substitute (4) and (5) in (6), the MSDC output frequency (in open loop) is:

\[
f_O = \frac{f_{CLK} C_2}{(C_1 + C_2)} \quad \text{[Hz, F]} \tag{7}
\]

or for \( i_1 \) and \( i_2 \) output frequency is:

\[
f_O = \frac{f_{CLK} i_2}{(i_1 + i_2)} \quad \text{[Hz, A]} \tag{8}
\]

From (7) and (8) is shown, that MSDC output frequency is nonlinearly dependent on capacitance (or current) changes. Graph of the relative output frequency on capacitance value change is shown in Fig. 4.

In closed loop (phase locked loop), the \( i_2 \) is changed, so that change in \( C_1 \) or \( i_1 \) is compensated.

**Fig. 4. Graph of the relative output frequency \((f_{CLK} = 1)\) in dependence on capacitance \((C_1 - C_2)/C_2\) change in open loop system.**

**4 MSDC simulation results**

Simulations were performed to confirm the results of mathematics analysis. These results were obtained programming of MSDC equations. The MSDC has also been simulated in system level by SIMULINK (MATLAB). Simulation results (time diagram) of open loop system for \( C_1 \) value step change are shown in Fig. 5. For open loop output evaluation, the output frequency of MSDC can be measured. Closed loop results are...
displayed in Fig. 6. In booth time diagrams, additional pulses are generated so that output pulses are equally spaced (output pulses = c) + d) in Fig. 6). Simulation results for step change of $C_1$ (or in $i_i$) is shown in Fig. 7, response on sinusoidal changes is shown in Fig. 8. For this simulation, simple EX-OR phase decoder and 3-order Butterworth low-pass filter were used (9):

$$F(s) = \frac{1}{s^3 + 2s^2 + 2s + 1} \quad (9)$$

Analog output of the MSDC is on the low-pass filter output. Digital output can be derived on the phase detector output by means of counter and digital filter. The closed loop of MSDC can be improved by using a sequential phase detector and charge pump, which has a "Neutral" position. When the loop is phase-locked, there is a very little phase error, and booth of the sequential phase detector will be low. Hence, at phase-lock, the loop filter is connected to an open circuit that does not generate noise.

![Fig. 5. Open loop system time diagram. a) voltage on $C_1$, b) $f_{CLK}/2$ pulses, c) pulses generated by Co1 comparator, d) additional pulses generated by logic.](image1)

![Fig. 6. Closed loop (PLL) system time diagram. a) voltage on $C_1$, b) $f_{CLK}/2$, c) pulses generated by Co1 comparator, d) additional pulses generated by logic.](image2)

![Fig. 7. Step response of MSDC (closed loop). a) input step change, b) voltage on lowpass filter output, voltage on $C_1$, d) pulses generated by Co1 comparator and correction logic (narrow pulse is added by correction logic).](image3)

![Fig. 8. Sinusoidal response of MSDC (closed loop). a) input signal, b) voltage on lowpass filter output, c) voltage on $C_1$, d) pulses generated by Co1 comparator and correction logic (2 narrow pulses are added by correction logic).](image4)

![Fig. 9. The basic connections of flip-flop sensor - simplified circuit with bipolar transistors](image5)
5 Flip-flop sensor

Another simple possibility for capacitance measuring based on switching-compensation principle is flip-flop circuit. The standard flip-flop sensor (FF) consisting of 2 transistors and 2 resistor and additional parts (Fig. 9) [8, 9, 10]. Instead of conventional load resistor it is possible to use light-dependent resistor, magnetoresistor, piezoresistor etc. The principle of measurement is based on the fact, that the measured non-electrical quantity breaks the value symmetry of the inverters of the FF. Measured quantity can be compensated by the compensating voltage $V_C$ (or current) so that symmetry is recovered. The analog and digital FF auto-compensative system is shown on Fig. 10 and 11 and 12 and 13 respectively. Instead of simple transistors, the fast analog switches were used [11]. In Fig. 14 and 15, the simulations are shown, in Fig. 16 and 17 experimental time diagrams are displayed. Assume, that $C_1 > C_2$, while the other parameters are identical, therefore voltage $V_2$ increases faster than $V_1$ and therefore when reach the Co2 comparator voltage, S1 is switched on and pulse is generated by means of OS2 one-shot. This pulse is processed in amplifier and integrator and compensating voltage $V_C$ is decreasing so that symmetry is recovered after several cycles. The compensating voltage $V_C$ can be computed from (10):

$$V_C \approx \frac{R(C_1 - C_2)}{C_1 + C_2} I_S \approx \frac{R \Delta C}{2C_S} I_S$$

where $R = R_1 + R_2$ and $I_S = I_1 + I_2$ (currents through $R_1$ and $R_2$). When the symmetry in FF is restored, the pulses on one-shots outputs (OS1 and OS2) appear alternately. This is shown in Fig. 14, 16 and 17.

Fig. 12. FF with analog feedback,
Co - comparator, OS - one-shot, S1; S2 - analog switches, D/A - digital-analog converter.

Fig. 13. FF with digital/analog feedback.
Co - comparator, OS - one-shot, S1; S2 - analog switches, D/A - digital-analog converter.

Fig. 14. a) Input step change, b) Compensating voltage, c) OS1 pulses, d) OS2 pulses
Fig. 15. The projection of state space trajectories. Voltage on C1 and C2. Flip-flop sensor with digital/analog feedback (Fig. 13).

Fig. 16. Measured time diagrams during no symmetry, \( C_1 < C_2 \), 1- voltage on C1, 2- voltage on C2, 3- Co2 (comparator) voltage.

Fig. 17. Time diagrams - symmetry recovered, 1- voltage on C1, 2- voltage on C2, 3- compensating voltage.

Fig. 18. Experimental result. Output voltage (compensating voltage) as a function of capacitor C1 value change.

6 Conclusions
Non-expensive measuring capacitance within the range of few pF is more and more important because of using e.g. micromachined ultrasound transducers in a wide variety of applications such as medical imaging, acoustic vision, proximity detection etc. Some advantages of capacitive sensors are:

Excellent linearity over entire dynamic range when Area is changed (since stray electric field are small). The system responds to average displacement of a large area of a moving electrode. Freedom of electrode materials and geometry for demanding environments and applications. Fractional change in capacitance can be made large. Capacitive sensors can be made to respond to displacements in one direction only. The forces exerted by the measuring apparatus are electrostatic, and usually small enough so that they can be disregarded. Capacitors are noiseless: excellent S/N ratio can be obtained.

In this paper, a two new method for non-electrical quantities, especially capacitance were presented. The first one is based on modified sigma-delta converter with compensated loop based on phase locked loop. This system can work in open or closed loop and has a fast response, but is more expensive and complicated. The second system is based on flip-flop sensor with auto-compensating possibility. This system is simple and can be simply integrated, but it hasn't a fast response. Both systems is possible to use for capacitance measuring in range of few pF, and are capable to give output information in analog or digital version.

The systems were mathematically solved, simulated and partly experimentally developed. The results of simulations and measuring are also presented in this paper.
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References