A CMOS Radio Frequency Receiver for Bluetooth Applications

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Abstract: - In this paper, a 2.4GHz radio frequency (RF) CMOS receiver based on all active devices for Bluetooth applications is presented. In this receiver, it is integrated with a low noise amplifier (LNA), a mixer, and a voltage controlled oscillator (VCO). The LNA design is used a differential output configure and high-Q active inductors to obtain low noise figure (NF) and high enough power gain. In the mixer design, a high linearity topology and low power consumption are designed. The VCO circuit based on high-Q active inductors and cross-coupled architecture is applied. The integration of the LNA, the mixer, and the VCO construct all active devices Bluetooth receive. Using TSMC 0.18um process, the receiver can be operated in 2.4GHz frequency for Bluetooth applications. Simulation results show that the receiver have the conversion gain of 16.2dB, the sensitivity of -101.5dBm, the noise figure of 2.5dB, the 1dB compression of -26.5dBm, and the IIP3 of -19.7dBm, respectively. The power consumption of the proposed receiver is about 42mW at 1.8V power supply.

Key-Words: - CMOS, Receiver, Low noise Amplifier, Mixer, Voltage Controlled Oscillator, and Bluetooth.

1 Introduction

In the recent years, the increasing demand of wireless transceivers with low cost, low power and small size, some research has been concentrating on single-chip solution. The CMOS processing is the most promising technology as RF circuits and digital circuits can be embedded together on the same chip.

Most of the previous reports in CMOS RF front-end circuits were implemented by using on-chip passive spiral inductors to achieve better matching, higher power gain, and lower power consumption [1-5]. However, the low quality-factors of an on-chip passive spiral inductor cause the degrading of the gain/bandwidth performance. Furthermore, obtaining high quality factor of a spiral inductor often requires additional processing steps to compensate the quality factor and these additional processing steps also require extra cost [6, 7]; moreover the inductance value is dependent on the size of the inductor [8]. The die area of an integrated passive inductor is usually larger than other components.

An alternative method called active inductor uses the CMOS active devices as an inductor, where the equivalent inductive impedance can be implemented. The above disadvantages of passive spiral inductors can be overcome by using an active inductor. The quality-factor and the inductance value are high enough to overcome the value exhibited by conventional spiral inductors. Depending on the chosen topology, the loss of an active inductor caused by the active devices can be greatly reduced and the area of an active inductor is independent of the desired inductance values [9-12]. Most of the active inductor circuits were applied in LNA and VCO produced impressive results [13-17]. In this paper, we will demonstrate a CMOS RF receiver front-end based on a high-quality active inductor that employs the heterodyne architecture with a single intermediate frequency (IF) for 2.4GHz Bluetooth application.

2 Bluetooth Receiver

The proposed block diagram of the RF front-end for Bluetooth receiver is shown in Figure 1. A RF signal of 2.4GHz goes from the antenna to a high-gain and low noise amplifier to obtain high enough gain and low noise figure. It is then down converted by using a high linearity mixer and a voltage controlled oscillator, produced 2.41GHz to an IF of 10 MHz. Since a low IF is chosen to relax the requirement of IF filters and image rejection [18].

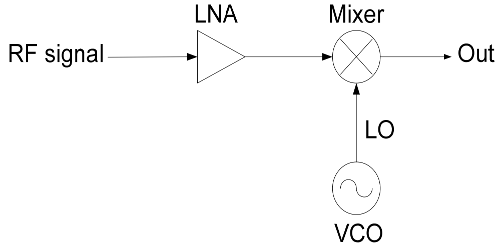

Fig.1 Block diagram of proposed receiver

According to the specification of Bluetooth system, the Bluetooth receiver must be met the regulations to satisfy the received quality. Thus, the sensitivity and the noise figure (NF) of the Bluetooth receiver must smaller than -70dBm and 8dB, respectively. The conversion gain, the 1dB compression, and the input third intercept point (IIP3) are great than 16dB, -26dBm, and -19dBm, respectively. The specifications of Bluetooth applications are summarized in Table 1.

Table 1 Specifications of Bluetooth applications

	Specifications
RF frequency (GHz)	2.4
LO frequency (GHz)	2.41
Supply voltage	1.8 V
Sensitivity (dBm)	< -70
Noise Figure (dB)	< 8
Conersion Gain dB	>16
1dB-Compression (dBm)	> -26
IIP3 (dBm)	> -19

3 High-Q Active Inductor Modeling

In order to achieve required specifications in a single-chip solution for the front-end of Bluetooth receiver, the proposed receiver is used high-Q active inductors to meet the specifications and reduce chip area.

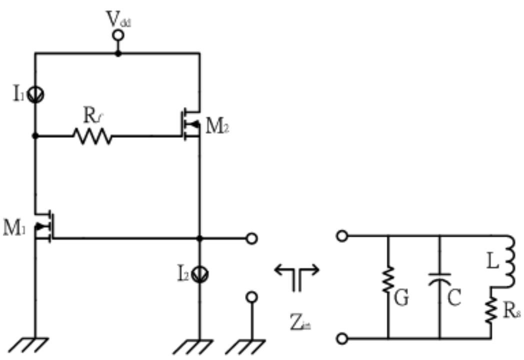

Fig. 2 Proposed high-Q active inductor

Figure 2 shows the proposed high-Q active inductor and input equivalent impedance that is applied throughout the design. The Q-value and the inductance of the active inductor are improved with feedback resistor (R_f). The characteristics of the improved active inductor are higher than that of the one without R_f. The comparisons between improved active inductor and original active inductor are shown in Table 2.

Table 2 Comparisons between improved active inductor and original active inductor

	Original	Improved
Q-Value	1.4	1E8
Loss (Ω)	8	1.2E-8
Inductance (nH)	2	5.8
Power Consumption (mW)	3	2.5

4 Proposed Bluetooth Receiver

The proposed Bluetooth RF front-end receiver, as shown in Fig. 1, includes a LNA, a mixer, and a VCO. The LNA based on high-Q active inductors and differential configuration is designed to obtain lower noise and higher power gain, respectively. The VCO is proposed with high-Q active inductors and cross-coupled configuration to achieve low phase noise. The mixer is used high linearity structure to obtain higher enough linearity. A description of each functional unit is provided as follows.

4.1 Low Noise Amplifier

An active inductor, shown in Fig. 2, is applied in the LNA to obtain low constant power consumption and low noise figure. In the Fig. 3, the LNA circuit consists of the differential amplifier, single input and differential output. Large gain and low noise figure can be obtained. In this LNA, the left-handed side is a common gate, a common source, an active inductor, and a buffer. The right-handed side has a common source, an active inductor, and a buffer. In the common-gate configuration, transistors M_1 and M_2 are employed as the input stage for input impedance matching. The input impedance (Z_{in}) of this amplifier can be approximated as Eq. (1).Where g_{mi}, g_{dsi}, and C_{gsi} are the transconductance, the output conductance, the gate-drain capacitance, and the gate-source capacitance of correspondence transistors, respectively. Hence, the input matching of the amplifier can be easily achieved by setting $1/g_{m2}$. The high-Q active inductors act as loads and common-source configuration to achieve high gain and inverse phase. Then inverse waveform is obtained from differential output port. $M_6 \sim M_9$ are the transistors of the buffer for output match.

$$Z_{in} \approx \frac{1}{(g_{ds1} + g_{m2} + j\omega C_{gs2} + j\omega C_{gd1})} \approx \frac{1}{g_{m2}} \qquad (1)$$

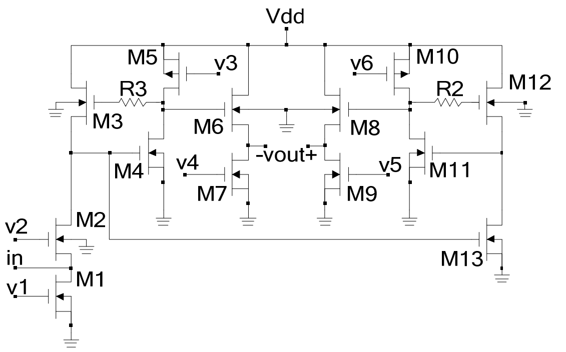

Fig. 3 Proposed low noise amplifier

A large gain of differential output is obtained from V_{out+} and V_{out-} because of the phase difference is 180° in the differential output. But the noise of the differential outputs is in phase. If the noise of differential outputs is closer, the noise will be very small. The characteristics of proposed amplifier are shown in Table 3.

Table 3 Characteristics of proposed LNA

	Proposed LNA
Technology	0.18-um CMOS
RF Frequency GHz	2.4
Supply Voltage	1.8V
S11 (dB)	-17.7
S22 (dB)	-13.2
Noise Figure (dB)	0.77
Gain (dB)	21.6
1dB-Compression (dBm)	-19.1
IIP3 (dBm)	-12.2
Power Consumption (mW)	11.2

4.2 Down Conversion Mixer

In a mixer design, the Gilbert-cell mixer commonly used for frequency conversion in most wireless communication systems. The Gilbert-cell topology has the linearity problems due to the number of stacked transistors. In order to solve the linearity problem, using parallel transistor in transconductance stage and the common-gate configuration to increase the linearity. In additional, a simple buffer is applied in the IF output to increase conversion gain. The down-conversion mixer is also obtained low noise figure and enough conversion gain.

The proposed low power direct conversion mixer shown in Fig. 4. To validate the characteristics of the mixer are summarized in Table 4.

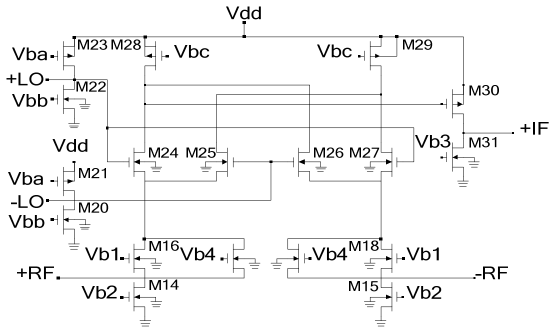

Fig. 4 Proposed Mixer

Table 4 Characteristics of the mixer

	Proposed Mixer
Technology	0.18-um CMOS
RF Frequency (GHz)	2.4
Supply Voltage	1.8V
Conversion Gain (dB)	9.9
1dB-Compression (dBm)	-16
IIP3 (dBm)	-5.2
Power Consumption (mW)	6.4

4.3 Voltage Controlled Oscillator

The main consideration of the VCO is expected to obtain low constant power consumption, wide tuning-range and low phase noise. The proposed VCO design uses a cross-coupled connection, which the cross-coupled connection generates a positive feedback loop for providing negative resistance, called a negative impedance converter (NIC), shown in Fig. 5. The NIC configuration compensates the loss of the active inductor in the LC tank to produce lossless LC tank.

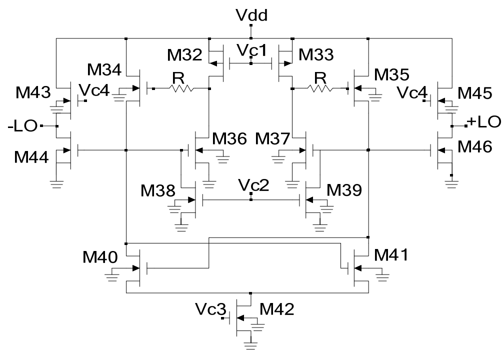

Fig. 5 Proposed voltage controlled oscillator

Table 5 Performance of proposed VCO

	Proposed VCO
Technology	0.18um CMOS
RF Frequency (GHz)	2.4
Supply Voltage	1.8V
Output Power (dB)	-6.6
Phase Noise@1MHz (dBc/Hz)	-81
Power Consumption (mW)	24.4

Two active inductors are acting as the equivalent inductance in the oscillator. Without varactors are employed in this oscillator. The oscillator frequency modulation function can be achieved by using the resistors of the active inductor. To provide adjustable frequency range, the feedback resistance R_f is added to tune the desired oscillator frequency. The performances of proposed VCO are summarized in Table 5.

5 Simulation Results of the Receiver

After careful design and simulation, the RF front-end receiver is designed by using TSMC 0.18-um technology to develop the Bluetooth receiver. The proposed receiver has a fairly good performance as compared to the conventional ones. In Fig. 6 shows the conversion gain, which is under 16.2dB in 2.4GHz. Fig. 7 displays the 1dB-compression of -26.5dB. By the Eq. (2) and the Eq. (3), the noise figure of the receiver can be calculated, which about 2.5dB. The sensitivity of the receiver is derived by the Eq. (4); the value is around -101.5dBm. The input third intercept (IIP3) can be obtained by the Fig. 8 and the Eq. (5). The value of the IIP3 is about -19.7dBm. From the simulation results of the receiver, the characteristics of the proposed receiver are satisfied the specifications for Bluetooth applications. The comparisons with other literatures are shown in Table 6, which the performance is better than other works.

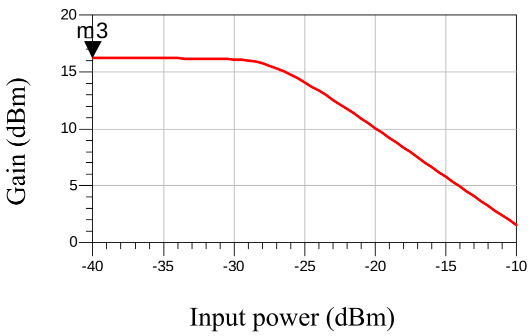

Fig. 6 Conversion gain of proposed receiver

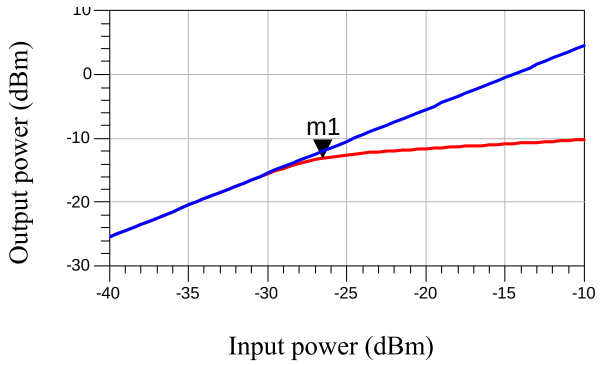

Fig. 7 1dB-compression of proposed receiver

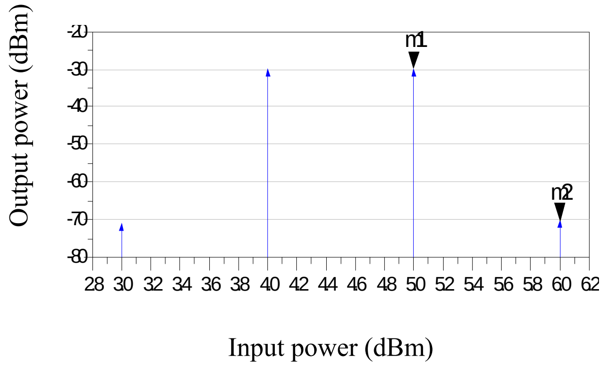

Fig. 8 Harmonic of proposed receiver

Table 6 Comparisons with other literatures

	Chiu [19]	Shen [20]	This work
RF frequency (GHz)	2.4	2.4	2.4
Technology	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS
Supply Voltage (V)	1.8	1.8	1.8
Sensitivity (dBm)	-70	---	-101.5
Noise Figure (dB)	8	4.8	2.5
Gain (dB)	16	28.4	16.2
1dB-Compression (dBm)	-26.5	-35	-26.5
IIP3 (dBm)	-19	-22.7	-19.7
Power Consumption (mW)	---	55.3	42

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} = 1.08 + \frac{15.2}{21.35} = 1.79dB \quad (2)$$

$$NF_{total} = 10\log(F_{total}) \approx 2.5dB \quad (3)$$

$$\begin{aligned} &NoiseFloor@290K + Noise\ in\ 10MHz\ BW \\ &+ Receiver\ Noise = -174 + 70 + 2.5 = -101.5dBm \end{aligned} \quad (4)$$

$$IIP3\big|_{dBm} = \frac{\Delta P\big|_{dB}}{2} + P_{in}\big|_{dBm} = \frac{40.6}{2} + (-40) = -19.7dBm \quad (5)$$

6 Conclusions

The proposed Bluetooth receiver based on all active devices not only can obtain required characteristics; it can also reduce the chip-area using active inductors. The receiver have the conversion gain of 16.2dB, the sensitivity of -101.5dBm, the noise figure of 2.5dB, the 1dB compression of -26.5dBm, and the IIP3 of -19.7dBm, respectively. The power consumption of the proposed receiver is about 42mW at 1.8V power supply.

References:

[1] J. Y. C. Chang and A. A. Abidi, A 750 MHz RF Amplifier in 2-um CMOS, *VLSI Cir. Dig. Tech. Papers*, 1992, pp. 111-112.

[2] A. N. Karanicolas, A 2.7 V 900 MHz CMOS LNA and Mixer, *ISSCC Dig. Teach. Papers*, 1996, pp. 50-51.

[3] A. Rofougaran *et al.*, A 1 GHz CMOS RF Front-end IC with Wide Dynamic Range, *ESSCIR,* 1995, pp. 250-253.

[4] J. Carols and M. S. J. Steyaert, A 1.5 GHz Highly Linear CMOS Down Conversion Mixer, *IEEE Journal of Solid-State Circuits*, Vol. 30, 1995, pp. 736-742.

[5] M. Rofougaran *et al.*, A 900Hz CMOS RF Power Amplifier with Programmable output, *VLSI Circuits Dig. Tech. Papers*, 1994, pp. 133-134.

[6] A. Worapishet, M. Chongcheawchamnan, and S. Srisathit, Broadband amplification in CMOS technology using cascaded single-stage distributed amplifier, *Electronics Letts.*, Vol. 38, 2002, pp. 675 –676.

[7] J. Y. C. Chang, A. A. Abidi, and M. Gaitain, Large Suspended Inductors on Silicon and Their use in a 2-um CMOS RF Amplifier, *IEEE Electronics Device Lett.,* Vol. 14, 1993, pp. 246-248.

[8] H. M. Greenhouse, Design of Planar Rectangular Microelectronic Inductors, *IEEE Trans. Parts, Hybrids, and Packaging,* Vol. PHP-10, 1974, pp.101-109.

[9] S. Lucyszyn and I. D. Robertson, Monolithic Narrow-Band Filter Using Ultrahigh-Q Tunable Active Inductor, *IEEE Trans. on Microwave Theory and Tech.*, Vol. 42, No. 12, 1994, pp. 2617-2622.

[10] S. Hara, T. Tokumitsu, T. Tanaka, and M. Aikawa, Broad-Band Monolithic Microwave Active Inductor and Its Application to Miniaturized Wide-Band Amplifier, *IEEE Trans. on Microwave Theory and Tech.*, Vol. 37, No. 12, 1988, pp. 1920-1924.

[11] H. Hayashi, M. Muraguchi, Y. Umeda, and T. Enoki, A High-Q Broad-Bad Active Inductor and Its Application to a Low-Loss Analog Phase Shifter, *IEEE Trans. on Microwave Theory and Tech.*, Vol. 44, No. 12, 1996, pp. 23669-2374.

[12] S. Hara, T. Tokumitsu, and M. Aikawa, Lossless Broad-Band Monolithic Microwave Active Inductor, *IEE Trans. on Microwave Theory and Tech.*, Vol. 37, No. 12, 1989, pp. 1979-1983.

[13] W. Zhuo, J. Pineda de Gyvez, and E. Sanchez-Sinencio, Programmable Low Noise Amplifier with Active Inductor Load, *IEEE International Symposium on Circuits and Systems,* Vol. 4, 1998, pp.365-368.

[14] U. Yodprasit, J. Ngarmnil, Q-Enhancement Technique for RF CMOS Active Inductor, *IEEE ISCAS Circuits and systems,* Vol. 5, 2000, pp. 589-592.

[15] V. L. Belini and M. A. Romero, Design of Active Inductor using CMOS Tchnology, *IEEE Proceeding of the 15th Symposium on Integrated Circuits abd Syetems Design* 2002, pp. 296-301.

[16] Y. Chang, J. Choma, and J. J. Wills, A 900MHz Active Inductor LNA with A Band pass Filter, *SSMSD'99' Symposium on Mixed-Signal Design,* 1999, pp.33-36.

[17] Y. Wu, M. Ismail, and H. Olsson, CMOS VHF/RF CCO based on active inductors, *Electron Lett.,* Vol. 37, 2001, pp. 472-473,

[18] Ying-Che Chung, etc., A Multi-Band RF Front-End Receiver for Bluetooth, WCDMA, and GPS Applications, IEEE Conference, 2004, pp. 1175-1177.

[19] Yung-Ming Chiu, Design of 2.4GHz and 5.7GHz CMOS RFICs for IEEE 802.11 WLAN application, Department of electrical engineering, National cheng kung university, 2003, pp. 107-109.

[20] Jia-Shian Shen, Analog front-end circuit design for a 2.4/5.2Ghz dualband RF receiver, Department of electrical engineering, Tatung University, 2004, pp. 55-57.