Implementation of a Fast Frequency Hopping Spread Spectrum modulator with System Generator on a FPGA

SANTIAGO T. PÉREZ, JESÚS B. ALONSO, CARLOS M. TRAVIESO, MIGUEL A. FERRER, JOSÉ F. CRUZ
Departamento de Señales y Comunicaciones
Universidad de Las Palmas de Gran Canaria
Campus Universitario de Tafira, S/N, 35017, Las Palmas de Gran Canaria, Las Palmas
SPAIN
{sperez, jalonso, ctravieso, mferrer}@dsc.ulpgc.es, jcruz@pas.ulpgc.es.

Abstract: - This work is based on a previous FFHSS (Fast Frequency Hopping Spread Spectrum) transceiver designed for wireless optical communications. The core of the transmitter is a discrete DDS (Direct Digital Synthesizer). In the first prototype the DDS control and the digital synchronization signal were generated using a PLD (Programmable Logic Device), besides a discrete external filter was necessary to eliminate high frequency components of digital synchronization signal and generated analog synchronization signal. The FFHSS and analog synchronization signals were emitted by two separated optical devices to avoid adding them with discrete analog circuits. The objective of this work is redesign the modulator over a FPGA (*Field Programmable Gate Array*) using System Generator from Xilinx and analyse the performances of this design methodology.

Key-Words: - spread spectrum, modulator, System Generator, Xilinx, Simulink, FPGA, VHDL, floating point, fixed point.

1 Introduction

The company Xilinx is one of the most extended manufacturer of FPGA (Field Programmable Gate Array) [1]. Xilinx offers System Generator [2] that is one design tool on Simulink of Matlab. This allows the fast design of systems using block diagrams, and its simulation even before the compilation. The compilation generates the files necessary for the Integrated System Environment (ISE) [3] of Xilinx for FPGA, where the description of the circuit is obtained in a standard hardware description language. These languages are Verilog and VHDL (Very High Speed Integrated Circuit Hardware Description Language) [4]. In ISE it is possible to compile the hardware description language files, and simulate the system behavioral or timing analysis. Afterwards the program file can be generated for the chosen device, this file can be download from the computer to the board which include the FPGA. Finally the performance of the design system must be checked with electronic measure equipment.

2 Design methodology

When System Generator is installed some Blocksets are included in Simulink. Each block is configured opening its dialog window, this permits fast and flexible designs. The designer does not perceive the signals as bits, instead the bits are grouped in signed or unsigned fixed point format. The operators force them to change automatically to the appropriate format. A block is not a hardware circuit necessarily, it relates with others to generate the appropriate hardware. The designer can include blocks described in a hardware description language, finite state machine flow diagram, Matlab files, etc. The System Generator simulations are bit and cycle accurate, this means results seen in simulation exactly match the results seen in hardware. The Simulink signals are shown as floating point values, which make easier to interpret them. The System Generator simulations are faster than traditional hardware description language simulators, and the results are easier to analyze. Otherwise the VHDL or Verilog code is not portable to others FPGA manufacturers, because System Generator uses Xilinx primitives which take advantage of the device characteristics. One of the objectives of this work is to analyze this design methodology.

3 Modulator design and simulation

This work is based on a previous designed transceiver [5] for Fast Frequency Hopping Spread Spectrum

(FFHSS) [6] for wireless optical communications [7]. The core of the transmitter was a discrete Direct Digital Synthesizer (DDS) [8]. In the first prototype the DDS control signals and digital synchronization signal were generated using a Programmable Logic Device (PLD). Besides an external discrete filter was necessary to eliminate the high frequency components of digital synchronization signal and get an analog synchronization signal. The FFHSS and synchronization signals were emitted by two separated optical emitters to avoid summing them with discrete analog circuits. In the receiver the signals were separated by discrete filters, the synchronization is reached after adjust a discrete circuits chain. The synchronization of the receiver makes possible to demodulate the FFHSS signal with two discrete DDS as local oscillators. These two DDS are the same type as the transmitter. In the receiver the control of these DDS is made with the same PLD type as the transmitter. The demodulator is a double branch structure of discrete circuits, each branch is formed by a mixed and an envelope detector.

The present work consists in redesign the FFHSS modulator and the generation of synchronization signal with System Generator. The block diagram of the designed system is in Fig. 1. It is formed by an internal data generator, a code generator, and two DDS to generate the FFHSS and synchronization signals. An external clock of 180 MHz is needed for the system.

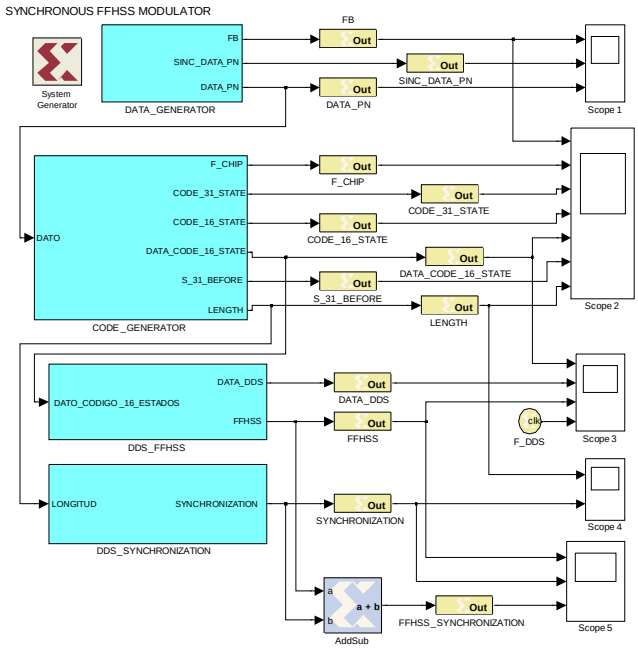

Fig. 1. Block diagram of synchronous FFHSS modulator designed with System Generator.

The internal data generator avoids using an external data source, it was designed using a Linear Feedback Shift Register block (LFSR) as pseudorandom generator of 15 bits length at 500 kilobits per second. The code generator is a pseudorandom LFSR of 31 states. The code rate is called chip frequency, its value is 1,5 Megachips per second, so three codes are generated by each data bit. In the two pseudorandom generators a pulse is generated each time the sequence begins, this provides a high quality periodic signal to synchronize the oscilloscope. In Fig. 2 the data synchronization pulse, the pseudorandom data, the code synchronization pulse and the code signal are shown after Simulink simulation. A five bits code is obtained with the four most significant bits of the pseudorandom code generator and the data bit as most significant bit. For each group of five bits a frequency is generated according with Table 1. The five bits are transformed to the format of the DDS input block of Xilinx. In Fig. 3 the five bits DDS input and the FFHSS signals are shown with Simulink. The DDS clock is the system clock (180 MHz), therefore with an external filter a pure senoidal signal can be synthesized until a bit less than 90 MHZ.

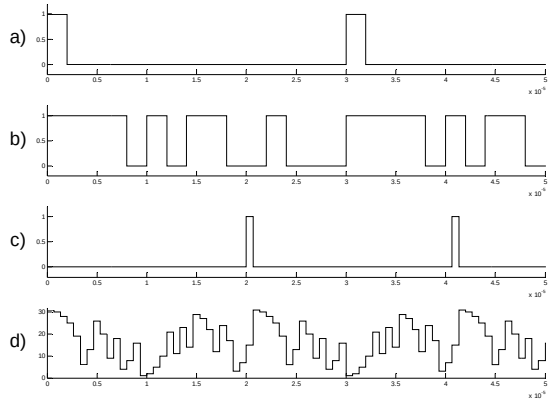

Fig. 2. a) Data synchronization pulse, b) pseudorandom data, c) code synchronization pulse, d) pseudorandom code in floating point format.

Code	Frequency (MHz)	Code	Frequency (MHz)
00000	24,384	10000	48,960
00001	25,920	10001	50,496
00010	27,456	10010	52,032
00011	28,992	10011	53,568
00100	30,528	10100	55,104
00101	32,064	10101	56,640
00110	33,600	10110	58,176
00111	35,136	10111	59,712
01000	36,672	11000	61,248
01001	38,208	11001	62,784
01010	39,744	11010	64,320
01011	41,280	11011	65,856
01100	42,816	11100	67,392
01101	44,352	11101	68,928
01110	45,888	11110	70,464
01111	47,424	11111	72,000

Table 1. Transmitted frequencies for the FFHSS signal.

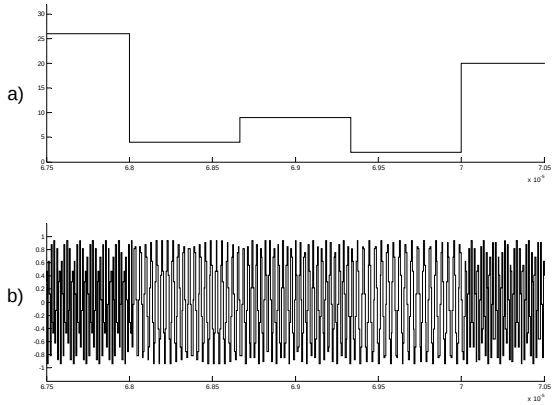

Fig. 3. a) Five bits DDS input, b) FFHSS signal in floating point format.

In the pseudorandom code generator a square signal with high level duration and low level duration marks the pseudorandom code length. This square signal modulates in phase to a 9 MHz carrier (see Fig. 4). The phase modulated signal carries information about the beginning of the pseudorandom code and its chip frequency because its carrier is a multiple of 1,5 MHz. Finally, the FFHSS signal and the synchronization signal are added like in Fig. 5.

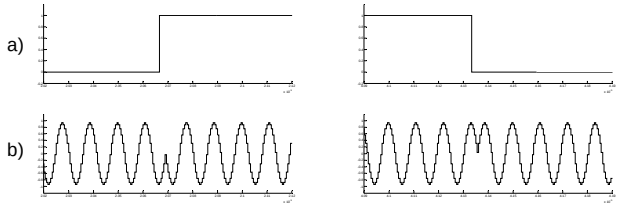

Fig. 4. a) Square signal of periodic twice the pseudorandom code length, b) synchronization signal in floating point format.

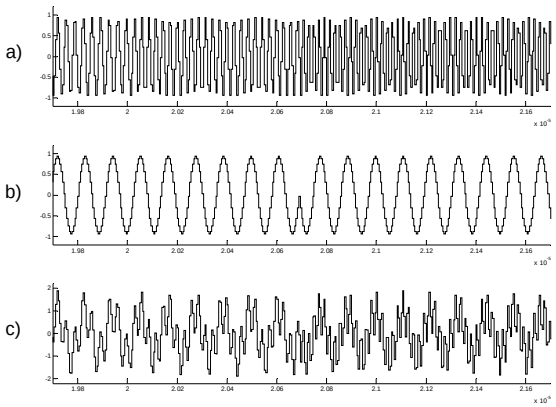

Fig. 5. a) FFHSS signal, b) synchronization signal, c) the above signals added together.

After the system has been simulated with Simulink it can be compiled with System Generator. The chosen device is a Virtex4 FPGA, and the hardware description language is VHDL. A project is then generated for ISE, which include the structural description of the system using several files. The syntax of the VHDL files can be checked, and the synthesis and behavioral simulation of the system can be done (see Fig. 6). After that, the implementation of the design allows the timing simulation of the modulator (see Fig. 7). Lastly, the programming file is generated for the chosen FPGA.

It must be noted that data and chip rates were changed softness from the prototype values, where the clock of the discrete DDS and the PLD clock were independents, and one frequency was not multiple of the another one. For the Virtex4 device chosen a master clock must exist, the rest of the clocks are generated by frequency division, the data and chip rates were changed to reach this condition. Others FPGA devices allow in its clocks generator block an integer multiplication factor, which join with the division factor form a rational number as multiplication factor.

In the moment of writing this document Xilinx does not offer boards with enough performance for digital to analog conversor (DAC). The design needs at least a 7 bits DAC, its rate conversion must reach 180 megasamples per second (MSPS), which is the sample rate of the transmitted signal. It can be verified that several boards exist for the proposed system with enough performances, these boards have been developed for companies which are specialized in FPGA kits. These kits include the necessary FPGA or even better, several 14 bits DAC at 480 MSPS. Three DAC are necessary is besides the FFHSS and synchronization signal are monitored. Another solution is to connect two boards, one of them with the FPGA and the other with the DAC stage. Choosing the hardware platform is proposed for future development because there are a lot of possibilities and the cost must be evaluated.

4 Conclusions

With this design methodology the typical advantageous features of using programmable digital devices are reached. Repeating a design consists in reprogramming the FPGA in chosen board, without designing printing circuit boards with discrete circuits. The alternative prototype reduces the number of external discrete components, the integration is improved and the adjusting of analog circuits is avoided.

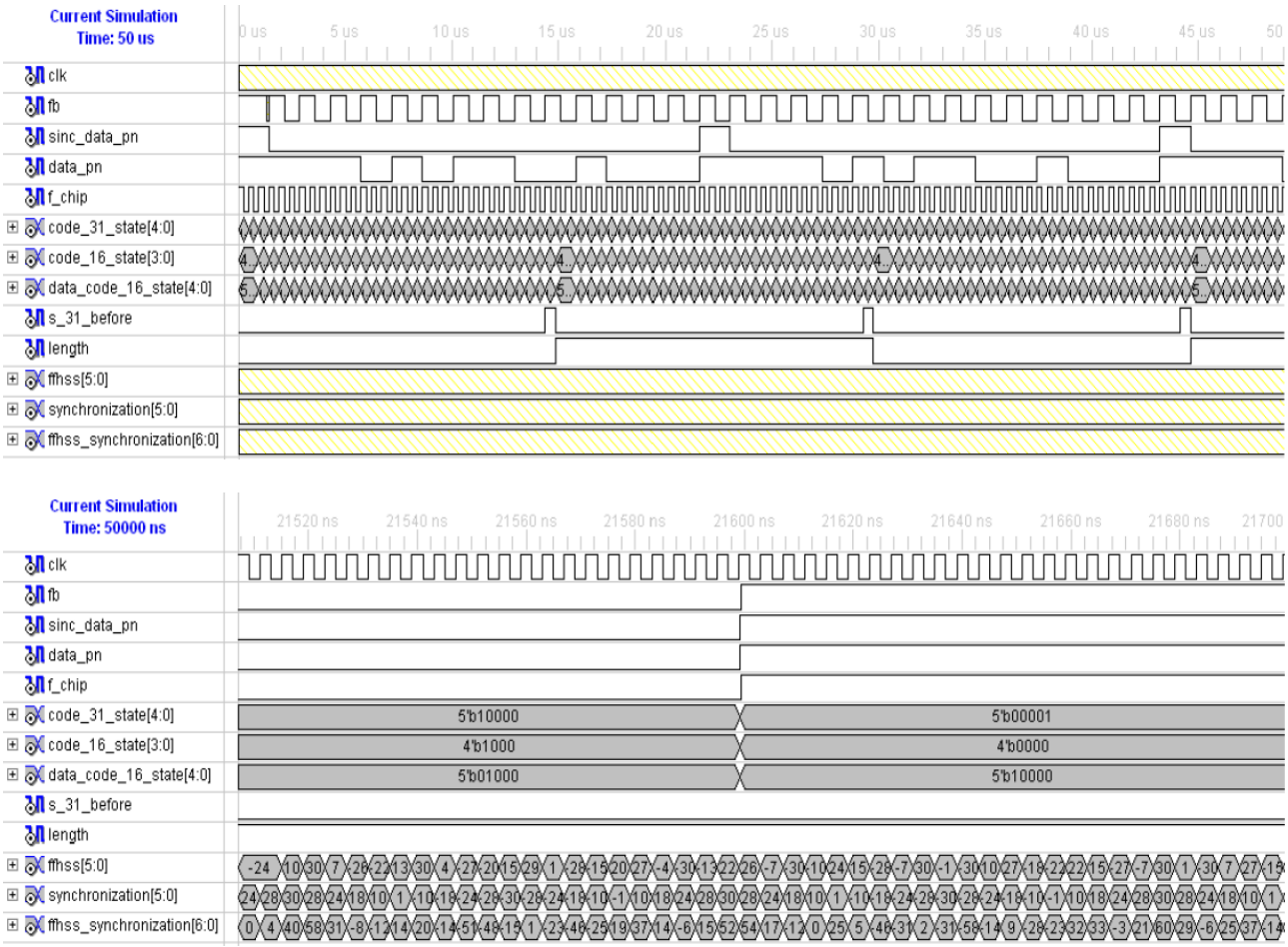

Fig. 6. Behavioral simulations of synchronous FFHSS modulator using ISE.

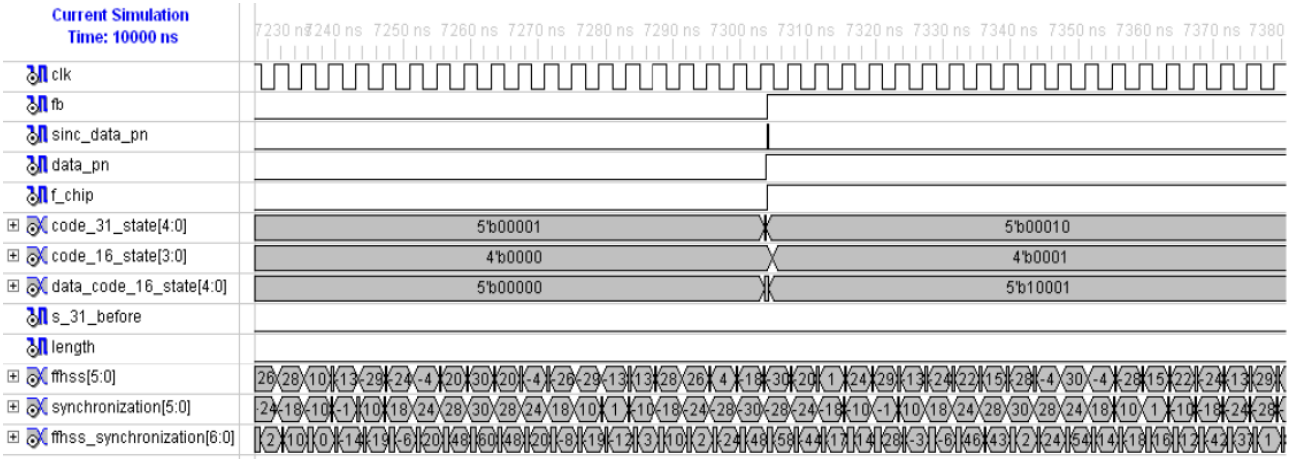

Fig. 7. Timing simulation of synchronous FFHSS modulator using ISE.

The design and simulation times are decreased, consequently the time to market is minimizing. It is important to note that electronic devices are short-lived, and reaching late to the market involves economic losses. The using tool permits great flexibility; in others words, the design parameters can be changed and new performance can be checked in several minutes. The Simulink simulations are easy to run, and the signals are shown in floating point format which make easier its analysis. These simulations are possible even before the compilation of the System Generator blocks to obtain the hardware description language files. The hardware description languages are Verilog and VHDL.

In the system designed with System Generator the FFHSS and synchronization signals are added in

fixed point format, even a weighted adder can be used. The flexibility allows to change the DDS parameters and check its performance. It can be included also an inverse sync filter that compensates variations in amplitude of the sinusoidal signal generated by the sampling and retention in the DDS output. The files obtained in this design occupy about 23.000 lines of VHDL code. The ISE software provides a power estimator that indicates a dissipation of 0,34 watts in the FPGA, and an estimated temperature of 29,8 degrees centigrade. This represents a power savings of 86% with respect the initial prototype. The FPGA core is supplied with 1,2 volts and the input-outputs pins support the LVCMOS 2,5 volts standard (Low Voltage Complementary Metal Oxide Semiconductor). The occupation rate of hardware in the FPGA is about 1% for logical resources and 20% for input-output pins, however the occupation rate for pins can be reduced until 10% if internal signals are no checked. The timing simulation demonstrates that 250 MSPS can be reached.

The design of the receiver is proposed as future work, all its blocks can be included in a FPGA: splitting filters, synchronization recovery and two branches demodulator. With System Generator is possible to simulate the transceiver, its performance can be tested in presence of additive white gaussian noise, which is available in System Generator. Moreover, it is possible to simulate the transmission through a channel with interference, distortion and others spread spectrum signals using different codes.

References:

[1] Scott Hauck, André DeHon, *Reconfigurable Computing*, Elsevier, 2008.

[2] http://www.xilinx.com/tools/sysgen.htm

[3] http://www.xilinx.com/tools/webpack.htm

[4] Volnei A. Pedroni, *Circuit Design with VHDL*, The MIT Press, 2004.

[5] Santiago T. Pérez, José A. Rabadán, Francisco A. Delgado, José R. Velázquez, Rafael Pérez, *Design of a synchronous Fast Frequency Hopping Spread Spectrum transceiver for indoor Wireless Optical Communications based on Programmable Logic Devices and Direct Digital Synthesizers*, XVIII Conference on Design of Circuits and Integrated Systems, pages: 737-742, Ciudad Real, Spain, 2003.

[6] Marvin K. Simon, Jim K. Omura, Robert A. Scholtz, Barry K. Levitt, *Spread Spectrum Communications Handbook*, McGraw-Hill Professional, 1994.

[7] Joseph M. Kahn, John R. Barry, *Wireless Infrared Communications*, Proceedings of the IEEE, Vol. 85, no. 2, 1997.

[8] http://www.analog.com/static/imported-files/data_sheets/AD9851.pdf