# A Multi-Level Switching Amplifier with Improved Power Efficiency for Analog Signals with High Crest Factor

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*Abstract:* - This paper describes a new multi-level switching amplifier concept, targeting increased power efficiency for analog signals with a very high crest factor. Interesting application fields include audio power amplifiers or line drivers in ADSL and VDSL equipment. Calculations prove its superior power efficiency compared to conventional class-D switching amplifiers as well as linear class-AB and class-G amplifiers. A silicon implementation of a multi-level switching ADSL line driver chip is currently in progress.

*Key-Words:* - Switching amplifier, multi-level architecture, high power efficiency, self-oscillating amplifier, pulse width modulation, audio amplifier, xDSL line driver.

## 1 Introduction

Linear class-AB amplifiers are undoubtedly the most obvious choice when analog signals have to be handled with a high degree of accuracy. There are, however, certain applications where these linear class-AB amplifiers suffer from a very poor power efficiency due to the high crest factor (defined as the ratio of the peak value to the rms value) of the analog signal. Typical examples are audio signals or ADSL-VDSL signals, which normally behave like a "noisy" low-amplitude signal with sporadic high-amplitude peaks or bursts. While the supply voltage is determined by the high-amplitude part of the signal in order to preserve signal purity over the whole dynamic range, the average power efficiency will predominantly depend on the low-amplitude part of the signal, resulting in disappointingly low values of the efficiency, typically in the range from 10% to 15%. An interesting approach to solve this problem is to use switching amplifiers instead. Since the output transistors in switching amplifiers no longer act as linear amplifying components but merely as solid-state switches, the power efficiency can be increased considerably. This paper presents an original type of switching amplifier, aiming at maximum power efficiency for analog signals with a very high crest factor.

## 2 Amplifier architecture

The best known switching amplifier is the class-D amplifier, also often referred to as a class-S amplifier. A basic single-ended version of such a class-D switching amplifier is shown in Fig. 1.

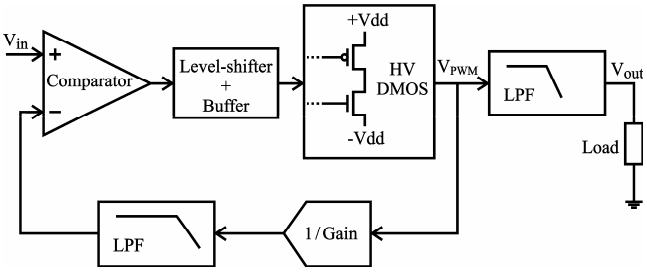


FIGURE 1. BLOCK DIAGRAM OF A SINGLE-ENDED CLASS-D SWITCHING AMPLIFIER.

The binary high-voltage output signal is fed back through an attenuator and low-pass filter before being compared to the analog input signal. The comparator then decides which of the 2 output transistors should be activated in an attempt to compensate the detected difference between the fed-back output signal and the analog input signal. When the control loop is properly designed, it turns out that this circuit behaves like a self-oscillating switching amplifier in which the binary output signal $V_{PWM}$ represents a Pulse-Width-Modulated (PWM) approximation of the amplified analog input signal, while the oscillation frequency depends on the loop dynamics, mainly the low-pass loop filter characteristics. Sending this binary output signal through a low-loss LC low-pass filter, having a cut-off frequency well below the switching frequency, will produce the desired amplified analog signal into the load [1].

There are of course numerous variations to the circuit of Fig. 1. Some of them are synchronized to a fixed-frequency clock signal instead of relying on the asynchronous self-oscillating behavior of the amplifier in Fig. 1. Other implementations employ a balanced output configuration instead of a single-ended one. Fig. 2 depicts a balanced alternative to the circuit of Fig. 1, exhibiting improved linearity as the even harmonics of the switching frequency are very effectively suppressed in a perfectly symmetrical architecture. Another advantage of a balanced configuration is that the supply voltage can be halved for a given signal amplitude.

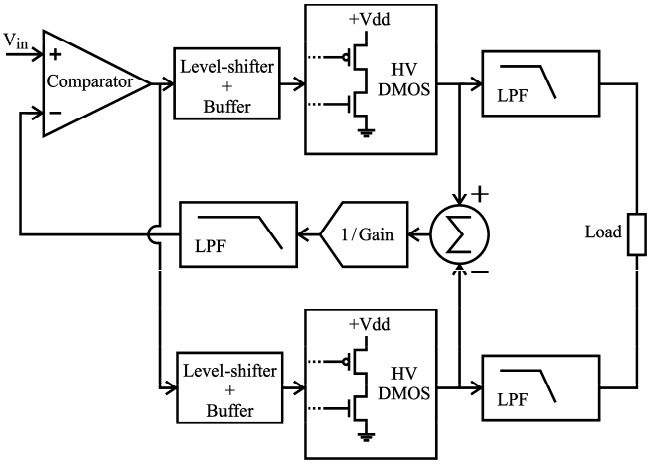


FIGURE 2. BLOCK DIAGRAM OF A BALANCED CLASS-D SWITCHING AMPLIFIER.

Although the switching amplifiers from Fig. 1 and Fig. 2 offer excellent power efficiency from a theoretical point of view, reality can be quite different. The binary output signal is constantly switching with high amplitude (between –Vdd and +Vdd in the circuit of Fig. 1, or between ground and +Vdd in the circuit of Fig. 2), resulting in a strong output current component at switching frequency. The high amplitude of this output current component, determined by the input impedance of the low-loss LC low-pass filter, will produce considerable power dissipation in the output transistors due to their non-zero on-state resistance. For analog signals with a very high crest factor, this dissipation in the output transistors can be much more important than the average useful signal power in the load, yielding rather low values of power efficiency. Also the significant dynamic power losses, caused by the continuous charging and discharging of parasitic capacitances at high switching frequency and high switching amplitude, have a negative impact on the global power efficiency. Both effects make very clear that the power efficiency can only be improved by reducing the amplitude of the switching output signal. However, in order to maintain the necessary dynamic range for the analog signal with high crest factor, the switching levels of the output stage must be made adjustable to the instantaneous signal amplitude. The resulting circuit is a multi-level switching amplifier.

Very few examples of multi-level switching amplifiers can be found in literature. They employ a multi-cell architecture based on the "flying battery" concept, where rechargeable batteries or "super capacitors" are needed to power the series connection of several switching cells [2]. In contrast to those very sophisticated designs, this paper proposes a less complex alternative architecture, employing fixed supply voltages instead of "flying batteries". A simplified block diagram of this novel multi-level switching amplifier is depicted in Fig. 3.

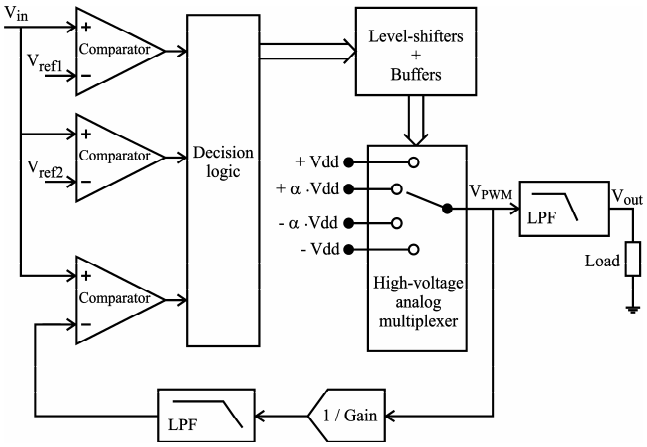


FIGURE 3. BLOCK DIAGRAM OF A MULTI-LEVEL SWITCHING AMPLIFIER.

This amplifier is also based on the self-oscillating principle as in the class-D switching amplifier of Fig. 1, but this time the classic binary push-pull output stage has been replaced by a 4-input multiplexer, consisting of 4 bidirectional high-voltage analog switches that can be implemented as symmetrical DMOS devices. This high-voltage analog multiplexer produces a 4-level PWM approximation of the analog input signal. An important logic block in the circuit decides between which of the 4 supply voltage levels the multiplexer should switch in order to minimize the power losses. To that purpose, a set of comparators constantly monitors the instantaneous input signal strength. When the signal amplitude is very low, the decision logic selects the supply voltages $-\alpha \cdot Vdd$ and $+\alpha \cdot Vdd$, the fraction $\alpha$ being a number much smaller than 1. When the comparators detect a high signal strength, on the other hand, the decision logic will bring the supply voltages –Vdd and +Vdd into action. One could say that this novel multi-level switching amplifier resembles a discrete version of the linear

class-G amplifier, which is basically a linear class-AB amplifier where the output stage is powered by a much lower supply voltage when the input signal shows low amplitudes.

There are still several options regarding the operation of the decision logic. From the point of view of power consumption, the switching strategy illustrated in Fig. 4 is undoubtedly the best choice (for typical values of Vdd = 25V, $\alpha$ = 0.2, and an amplifier gain of 10).

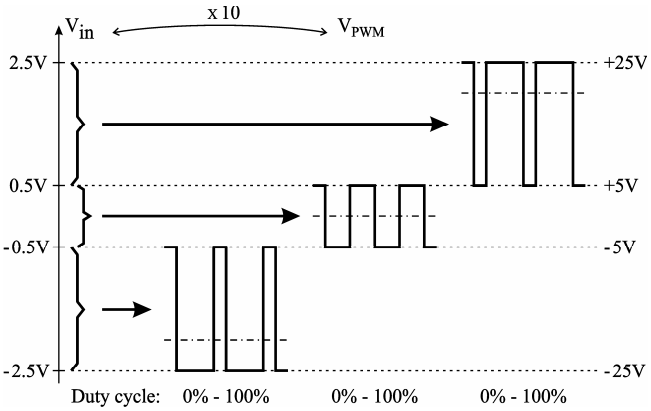


FIGURE 4. BASIC SWITCHING STRATEGY FOR A MULTI-LEVEL SWITCHING AMPLIFIER.

Depending on the signal strength, the decision logic always selects the supply voltages that result in minimum switching amplitude. There is, however, an important drawback: When the input signal passes one of the comparator reference levels, the duty ratio of the switching output signal suddenly changes from 0 to 100%, or vice versa. Detailed circuit simulations have shown that this results in improper behavior of the self-oscillating loop. As a consequence, the accuracy of the filtered output signal in the load deteriorates significantly. It is therefore advisable to use the improved switching strategy of Fig. 5 instead.

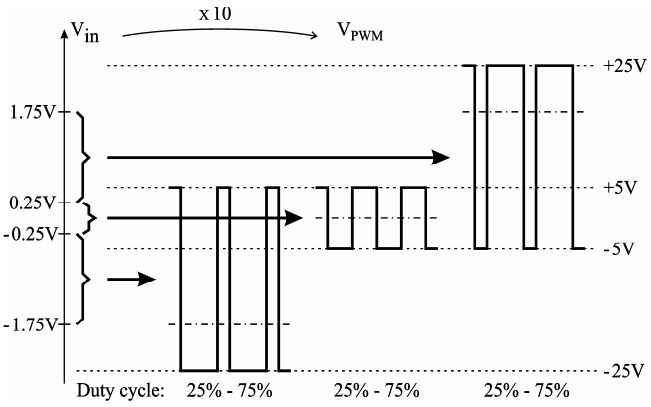


FIGURE 5. IMPROVED SWITCHING STRATEGY FOR A MULTI-LEVEL SWITCHING AMPLIFIER.

At high signal strength, the switching amplitude is somewhat larger than in the case of Fig. 4, yielding a slightly reduced power efficiency, but for the chosen circuit parameters the duty ratio no longer leaves the 25% to 75% range, no matter what the instantaneous input signal amplitude may be. The feedback loop now operates properly within the whole dynamic range, and therefore, the switching strategy of Fig. 5 is definitely the best trade-off between power efficiency and signal purity.

## 3 Power efficiency calculation

In order to estimate the power efficiency of the multi-level switching amplifier and to allow a comparison with other amplifier types, the simplified model of Fig. 6 will be used for the high-voltage analog multiplexer in the output stage of the amplifier.

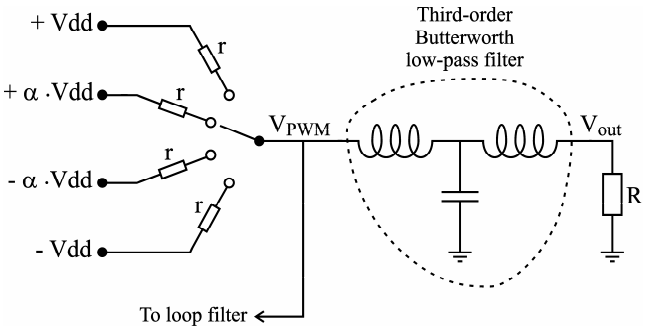


FIGURE 6. SIMPLIFIED MODEL OF THE HIGH-VOLTAGE ANALOG MULTIPLEXER TO CALCULATE THE POWER EFFICIENCY OF A MULTI-LEVEL SWITCHING AMPLIFIER.

Each bidirectional analog switch in the multiplexer is modeled by a small resistor with value r, representing the on-state resistance of the symmetrical DMOS devices. In that way, we can fairly easily calculate the power losses caused by the switching current flowing through the DMOS transistors. It is important to note that the dynamic power losses, caused by the continuous charging and discharging of parasitic capacitances, will be neglected in this analysis.

Assuming that a DC input signal is applied to the amplifier, the switching output signal $V_{PWM}$ can be written as follows:

$$V_{PWM}(t) = V_{DC} + \sum_{n=1}^{\infty} a_n \cdot \cos\left(\frac{2\pi n t}{T_S}\right)$$

In this expression, the first term corresponds to the amplified DC signal in the load resistance R, while the second term represents the Fourier series of the AC part in the switching waveform, $T_s$ being the switching period. Knowing that in a real circuit

implementation the on-state resistance r of the DMOS switches should be much smaller than the load resistance R, we can say in a first-order approximation that $V_{PWM}$ will be switching between supply voltage levels $V_A$ and $V_B$, where the precise values of $V_A$ (–Vdd or $-\alpha\cdot$Vdd) and $V_B$ ($+\alpha\cdot$Vdd or +Vdd) are selected by the decision logic according to the switching strategy of Fig. 5. The Fourier coefficients are then given by the formula:

$$a_n = \frac{2(V_B - V_A)}{\pi n} \cdot \sin\left(\frac{\pi n \tau}{T_S}\right) \quad ; \quad n = 1, \cdots, \infty$$

The pulse duration $\tau$ will depend on the input signal strength and the selected supply voltage levels according to the following expression for the duty ratio of $V_{PWM}$:

$$\frac{\tau}{T_S} = \frac{V_{DC} - V_A}{V_B - V_A}$$

This leads to a very good first-order approximation for the total average power dissipation in the bidirectional switches in the high-voltage analog multiplexer:

$$\overline{P_{r,tot}} = r \cdot \left(\frac{V_{DC}}{R}\right)^2 + \frac{r}{2} \cdot \sum_{n=1}^{\infty} \frac{{a_n}^2}{\left|Z_{in}(n\omega_S)\right|^2}$$

The first term represents the effect of the DC current flowing from the multiplexer to the load, while the second term reflects the effect of the switching current. The amplitudes of the harmonics in this switching current depend on the amplitudes of the corresponding harmonics in the $V_{PWM}$ waveform as well as on the input impedance of the low-loss LC low-pass filter. In case a third-order Butterworth low-pass filter is adopted, this input impedance is given by:

$$\left|Z_{in}(\omega)\right|^2 = R^2 \cdot \frac{1 + \left(\frac{\omega}{\omega_C}\right)^6}{1 + \frac{4}{9}\cdot\left(\frac{\omega}{\omega_C}\right)^2 + \frac{4}{9}\cdot\left(\frac{\omega}{\omega_C}\right)^4}$$

The angular cut-off frequency $\omega_c$ should of course be chosen much below the angular switching frequency $\omega_s$. We now define the power efficiency $\eta$ as the ratio between the useful DC output power in the load and the total power delivered by all supply voltages to the multiplexer and the load:

$$\eta = \frac{P_R}{P_R + \overline{P_{r,tot}}} = \frac{\frac{{V_{DC}}^2}{R}}{\frac{{V_{DC}}^2}{R} + \overline{P_{r,tot}}}$$

This leads to the following expression for calculating the power efficiency in the multi-level switching amplifier:

$$\eta = \frac{1}{1 + \frac{r}{R} + \frac{r \cdot R}{2{V_{DC}}^2} \cdot \sum_{n=1}^{\infty} \frac{{a_n}^2}{\left|Z_{in}(n\omega_S)\right|^2}}$$

Note that this formula applies to DC excitation of the amplifier. When other types of input signals are considered (sine wave, audio, ADSL,…), the global power efficiency can be estimated by repeating a similar calculation using the probability density function of the signal under consideration. Such a quasi-static approximation implies that the switching frequency is much higher than the signal bandwidth.

Some interesting results, based on these formulas, are gathered in Figs. 7, 8 and 9. These data correspond to the following system parameters: Vdd = 25V , $\alpha$ = 0.2 , gain = 10 , R = 10 · r , $\omega_s = 5 \cdot \omega_c$. Fig. 7 compares the power efficiency of the multi-level switching amplifier and the class-D switching amplifier, the latter employing exactly the same system parameters except for the fact that the supply voltage levels of $-\alpha\cdot$Vdd and $+\alpha\cdot$Vdd are not present of course.

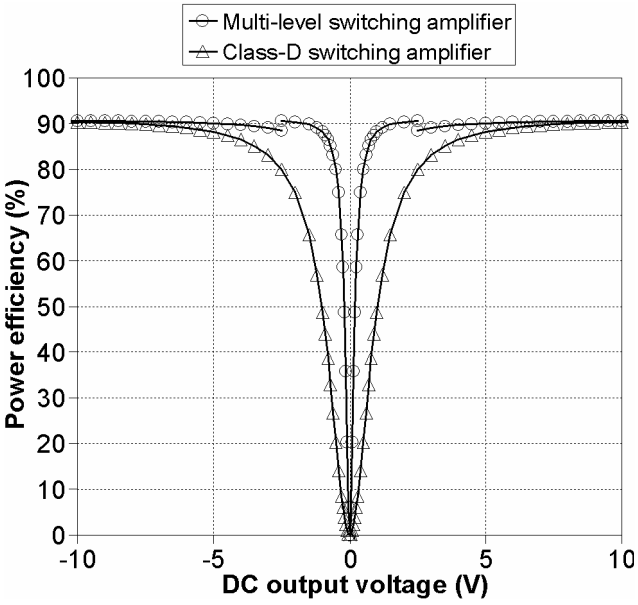


FIGURE 7. POWER EFFICIENCY: COMPARISON BETWEEN MULTI-LEVEL AND CLASS-D SWITCHING AMPLIFIERS.

At small signal amplitudes, which is the most important part when the amplifier is intended for signals with a very high crest factor, the superior performance of the multi-level switching amplifier is very clear. At 1V output voltage, the multi-level switching amplifier exhibits 88% efficiency against 49% for the class-D switching amplifier! At 2V output voltage, the difference is still 90% against 75%. At higher signal amplitudes, the difference almost disappears because the effect of the switching current, having a smaller amplitude in the multi-level version, becomes negligible compared to the effect of the DC current, which is exactly the same in both switching amplifiers. Also note the small discontinuity at 2.5V output voltage for the multi-level switching amplifier due to the change in one of the supply voltages that are selected by the decision logic according to the switching strategy of Fig. 5.

Fig. 8 compares the performance of the multi-level switching amplifier and an ideal linear class-G amplifier, the latter employing exactly the same 4 supply voltage levels. This time the performance of the multi-level switching amplifier is superior over the whole range, except for output voltage levels in the neighborhood of –5V and +5V, when the linear class-G amplifier operates very close to the $-\alpha \cdot Vdd$ and $+\alpha \cdot Vdd$ supply voltages.

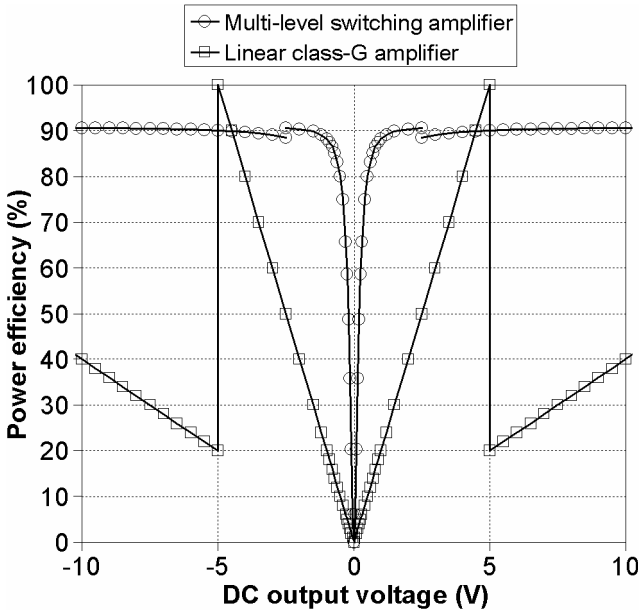


FIGURE 8. POWER EFFICIENCY: COMPARISON BETWEEN A MULTI-LEVEL SWITCHING AMPLIFIER AND AN IDEAL LINEAR CLASS-G AMPLIFIER.

Finally, Fig. 9 compares the power efficiency of all relevant linear and switching amplifiers in the range of small signal amplitudes. From this graph it's clear that the multi-level switching amplifier is definitely the best choice when it comes to amplifying analog signals with a very high crest factor!

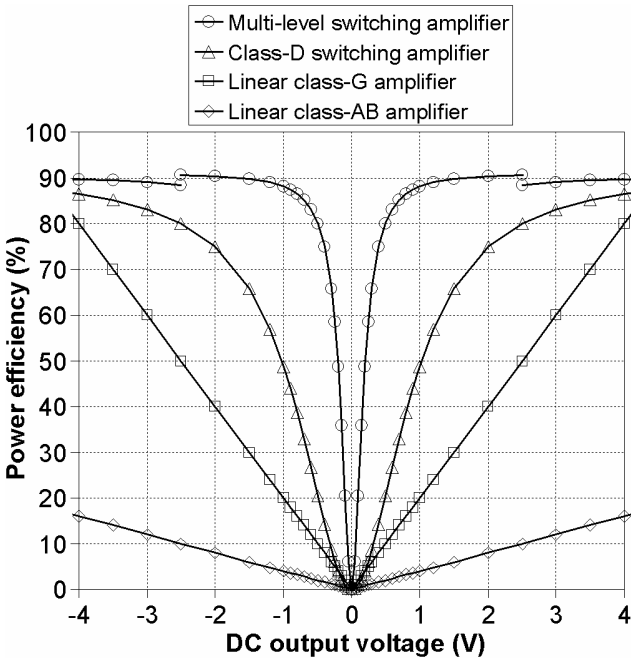


FIGURE 9. POWER EFFICIENCY: COMPARISON BETWEEN DIFFERENT TYPES OF SWITCHING AND LINEAR AMPLIFIERS.

## 4 Switching frequency rejection ratio

Despite the presence of the LC low-pass filter at the amplifier output, having a cut-off frequency far below the switching frequency, it cannot be avoided that some of the high-frequency content related to the switching frequency and its harmonics reaches the load. Although the resulting additional power losses in the load are normally negligible compared to the high-frequency dissipation in the output transistors, the residual switching frequency content in the load signal must be minimized in several applications (e.g. in xDSL line drivers) in order to comply with system requirements regarding signal distortion or EMC specifications.

A figure of merit that is often used in switched-mode systems to describe the residual high-frequency content in the load is the so-called Switching Frequency Rejection Ratio (SFRR), defined as the ratio of the useful signal power to the residual switching power in the load:

$$\mathrm{SFRR} = 10 \cdot \log\left(\frac{\text{useful output power in load}}{\text{residual switching power in load}}\right)$$

Under DC excitation, employing the Fourier series expansion of the multi-level switching waveform at

the multiplexer output, the expression for the SFRR becomes:

$$\mathrm{SFRR} = 10 \cdot \log \left( \frac{\frac{V_{DC}{}^2}{R}}{\frac{1}{2R} \cdot \sum_{n=1}^{\infty} a_n{}^2 \cdot |H(n\omega_S)|^2} \right)$$

Herein, H(ω) represents the voltage transfer function of the LC low-pass filter at the amplifier output. In case a third-order Butterworth low-pass filter is used, the voltage transfer function H(ω) is given by the following formula:

$$|H(\omega)|^2 = \frac{1}{1 + \left( \frac{\omega}{\omega_C} \right)^6}$$

Based on these equations, Fig. 10 compares the calculated SFRR of the multi-level switching amplifier and a conventional class-D switching amplifier. The following system parameter set was used during the calculations: Vdd = 25V , $\alpha = 0.2$ , $\omega_s = 5 \cdot \omega_c$ . Apparently, there is a SFRR improvement of about 15dB at low signal amplitudes in the case of the new multi-level switching amplifier. This means that a lower-order LC low-pass filter can be used compared to a class-D switching amplifier in order to meet given distortion or EMC requirements, without increasing the switching frequency or reducing the signal bandwidth.

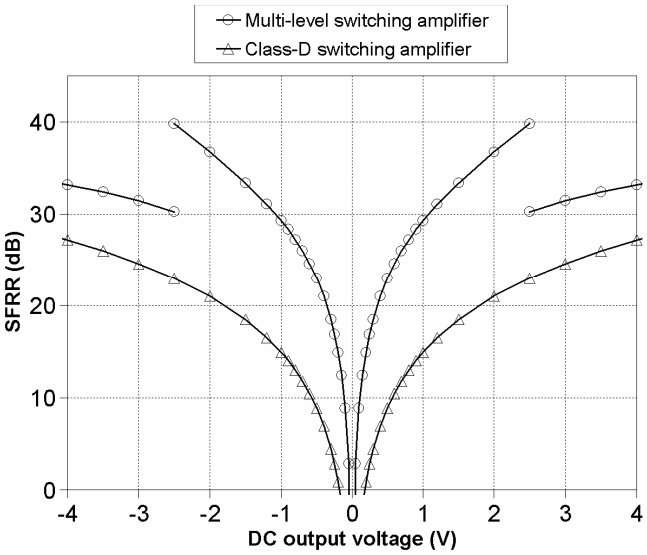


FIGURE 10. SFRR: COMPARISON BETWEEN MULTI-LEVEL AND CLASS-D SWITCHING AMPLIFIERS.

# 5 Practical circuit implementation

The proposed multi-level switching amplifier concept is currently being implemented in a central-office ADSL line driver chip. This design will be submitted to the MPW (Multi-Project Wafer) service of Europractice in May 2009 for integration in the 50V 0.35µm I3T50 smart power technology of ON Semiconductor. Experimental results on this new multi-level switching ADSL line driver will be presented at a next WSEAS conference.

# 6 Conclusion

A novel multi-level switching amplifier concept, aiming at improved power efficiency for analog signals with a very high crest factor, was presented. Calculations have proven its superior performance in terms of power efficiency compared to conventional class-D switching amplifiers as well as linear class-AB and class-G amplifiers. This new concept is currently being implemented in an advanced central-office ADSL line driver chip.

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