Abstract: Load characteristics of harmonic and unbalance cannot be expressed in the traditional apparent power and power factor which only consider the fundamental and three-phase balanced sinusoidal conditions. This paper utilizes the Xilinx Spartan-3 FPGA (XC3S1500 - 4FG676) chip to develop the platform to implement the calculation methods of apparent powers and power factors. This paper discussed the effective power and power factor, the arithmetic power and power factor, and the fundamental power and power factor. ModelSim is used at first to simulate the calculation of apparent powers and power factors to ensure the accuracy of timing and function. Research results show that the designed chip can compute accurately the apparent powers and power factors considering the effects of nonsinusoidal and unbalanced conditions.

Key-Words: FPGA, SoC, Power Factor, Harmonic, Unbalanced Power System.

1 Introduction

The value of power factor generally is an important penalty factor in the revenue of electricity customers. However, the traditional power factor definition always assumes that the load condition is sinusoidal. The effects of load unbalance and harmonic distortion are neglected. It has been reported that if traditional electro-mechanical meters are used in circumstances of nonsinusoidal and three-phase unbalanced voltages or currents, the errors can reach 20%~30%[1]. In recent years, there are many discussions regarding the power definitions and calculations [2-7]. Several definitions are given in the IEEE Std. 1459, such as effective apparent power, arithmetic apparent power, and vector apparent power.

Since harmonic pollution, load unbalance, and reactive power fluctuation could affect the power factor values of customers, six different definitions of power factor values have been investigated for the same recorded measurement data of customers in [8]. The different results of calculation are dependent on the load characteristics. In [9], it is shown that the currently used apparent power definitions, namely the Arithmetic VA and the Vector VA, both lack an important property.

Since good definitions of apparent powers and power factors may well reflect the practical situations of threephase unbalanced and non-sinusoidal circuits, the effective power, effective power factor, arithmetic power, and arithmetic power factor are investigated in this paper. The calculation algorithms will be implemented by using a FPGA-based chip. The effects of nonsinusoidal and unbalanced conditions are considered.

2 Power Factor Definition

2.1 Single-phase system

For a single-phase load under sinusoidal condition, the instantaneous voltage and current are, respectively,

\[ v(t) = \sqrt{2} V \sin(\omega t + \alpha) \]  
\[ i(t) = \sqrt{2} I \sin(\omega t + \beta) \]
Hence the apparent power, active power, and reactive power are, respectively,

\[ S = VI \]  
\[ P = V I \cos \theta \]  
\[ Q = VI \sin \theta \]  

where \( \theta = \alpha - \beta \) is the phase angle difference between voltage and current.

\[ \text{PF} = \frac{P}{S} = \frac{P}{\sqrt{P^2 + Q^2}} \]  

When a single-phase system is under non-sinusoidal situation, the instantaneous voltage and current values can be

\[ v(t) = V_x + \sqrt{2} \sum_{h=1}^{\infty} V_h \sin(h0t + \alpha_h) \]  
\[ i(t) = I_x + \sqrt{2} \sum_{h=1}^{\infty} I_h \sin(h0t + \beta_h) \]  

where

\( V_x \) = average voltage
\( I_x \) = average current
\( V_h \) = rms values of harmonic voltages
\( I_h \) = rms values of harmonic currents
\( \alpha_h \) = phase angles of harmonic voltages
\( \beta_h \) = phase angles of harmonic currents

The root mean squared (rms) values are given by

\[ V_{\text{rms}} = \sqrt{\sum V_i^2} \]  
\[ I_{\text{rms}} = \sqrt{\sum I_i^2} \]  

The apparent power, active power, and reactive power are

\[ S = V_{\text{rms}} I_{\text{rms}} \]  
\[ P = \sum V_i I_i \cos(\alpha_i - \beta_i) \]  
\[ Q_S = \sum V_i I_i \sin(\alpha_i - \beta_i) \]  

Then the power factor is defined as

\[ \text{PF} = \frac{P}{S} = \frac{P}{\sqrt{P^2 + Q_S^2}} \]  

Because \( S \neq \sqrt{P^2 + Q_S^2} \). There is a definition of the distortion power as

\[ D_n = \sqrt{S^2 - P^2 - Q_S^2} \]  

2.2 Three single-phase system

(1) Arithmetic apparent power and arithmetic power factor are, respectively

\[ S_A = S_R + S_S + S_T = V_R I_R + V_S I_S + V_T I_T \]  
\[ \text{PF}_{A} = \frac{P}{S_A} \]  

(2) Effective apparent power and effective power factor are, respectively

\[ S_e = 3V_e I_e \]  
\[ \text{PF}_{e} = \frac{P}{S_e} \]  

2.3 In a three-phase four-wire system

Effective current

\[ I_e = \sqrt{\frac{I_{R1}^2 + I_{S1}^2 + I_{T1}^2}{3}} \]  

Effective voltage

\[ V_e = \sqrt{\frac{1}{18} \left[(V_{R1}^2 + V_{S1}^2 + V_{T1}^2) + \left(V_{R1}^2 + V_{S1}^2 + V_{T1}^2\right)\right]} \]  

2.4 In a three-phase three-wire system

Effective current

\[ I_e = \sqrt{\frac{I_{R1}^2 + I_{S1}^2 + I_{T1}^2}{3}} \]  

Effective voltage

\[ V_e = \sqrt{\frac{V_{R1}^2 + V_{S1}^2 + V_{T1}^2}{9}} \]  

The fundamental apparent power and fundamental power factor are, respectively

\[ S_{f1} = S_{R1} + S_{S1} + S_{T1} = V_{R1} I_{R1} + V_{S1} I_{S1} + V_{T1} I_{T1} \]  
\[ \text{PF}_{f1} = \frac{P}{S_{f1}} \]  

There are three definitions for the average power factor

(a) average arithmetic power factor

\[ \text{PF}_{a} = \frac{\int P(t)dt}{\int S_A(t)dt} \]  

(b) average effective power factor

\[ \text{PF}_{e} = \frac{\int P(t)dt}{\int S_e(t)dt} \]  

(c) the average fundamental power factor

\[ \text{PF}_{f} = \frac{\int P(t)dt}{\int S_f(t)dt} \]  

2.5 Evaluate of harmonic and unbalance load

The effective voltage and current of fundamental components of the three-phase four-wire system are given by

\[ V_{el} = \sqrt{\frac{1}{18} \left[(V_{R1}^2 + V_{S1}^2 + V_{T1}^2) + \left(V_{R1}^2 + V_{S1}^2 + V_{T1}^2\right)\right]} \]  
\[ I_{el} = \sqrt{\frac{I_{R1}^2 + I_{S1}^2 + I_{T1}^2}{3}} \]  

Those of the three-phase three-wire system are given by

\[ V_{el} = \sqrt{\frac{V_{R1}^2 + V_{S1}^2 + V_{T1}^2}{9}} \]
The fundamental effective apparent power is
\[ S_{el} = 3V_{el}I_{el} \]  
(32)

The nonfundamental effective apparent power is
\[ S_{N} = \sqrt{S_{N}^2 - S_{el}^2} \]  
(33)

The normalized nonfundamental effective apparent power is
\[ \bar{S}_{N} = \frac{S_{N}}{S_{el}} \]  
(34)

The normalized fundamental unbalanced apparent power is
\[ \bar{S}_{u} = \frac{S_{u}}{S_{el}} \]  
(35)

3. Structure of Simulation System

3.1 Matlab Simulation Structure

The simulation block to generate the test data is developed by using Simulink and Sim Power Systems, which work together with the MATLAB [10]. The simulation model is shown in Fig. 1. There are four given loading cases in investigating the three-phase system as shown in Table 1 and Table 2, based on the properties of fundamental powers and harmonic currents.

Fig. 1 Three-phase four-wire simulation model

3.2 Matlab simulation procedures

1. The 220V (line-to-line) symmetrical three-phase voltage source block is used.

2. The three-phase loads are composed of series RLC load blocks and the harmonic current source blocks. The series RLC load blocks can be assigned the fundamental active and reactive powers. Then it is to use the sim command to adjust unbalance level and harmonic level.

3. The instantaneous line-to-line voltages and line currents of the three-phase cases can be obtained by the measurement blocks. The sampling rate is 3840 sample/second.

4. Then the instantaneous voltages and current values are sent to calculate the values of apparent power and power factors. Because float-point calculations need large RAM capacity and long operation time, the instantaneous voltage and current values are mapped to integral values. The procedures are as follows:

   (1) Normalizing to per-unit values

   - The rms value of the voltage is 220V and that of the fundamental current is 41.45A in case 1, so that all instantaneous values are divided by the rms value.

   (2) Then all per-unit values are multiplied by 1000 to increase the effective bit number in FPGA.

   (3) The calculation error by FPGA is defined as

\[ \varepsilon(\%) = \frac{\text{given value(Matlab)} - \text{calculated value(FPGA)}}{\text{given value(Matlab)}} \times 100 \]  
(39)

3.3 FPGA Simulation Structure

In calculation of the fundamental components, the FIR filter is used to obtain the fundamental frequency components and reject harmonic components. The impulse response of the filter is computed by Matlab.
4 Calculation Results

Figs. 4-6 show the trend of $\text{PF}_e$, $\text{PF}_A$ and $\text{PF}_{A1}$ versus $U_{1S}$ and $e_{N_S}$. The utilization conditions of FPGA are given in TABLES 3-5. Some observations can be obtained.

(a) In Case 1, the three-phase system is balanced and without harmonic loads. The power factor values are given in TABLE 6. So the values of three power factors are the same.

(b) In Case 2, the three-phase system is unbalanced but with harmonic loads. The distortion power is zero. Because $\text{PF}_A$ and $\text{PF}_{A1}$ do not drop with $U_{1S}$, they do not reflect the unbalance degree. Only $\text{PF}_e$ drops with of $U_{1S}$, so that it can reflect the effect of unbalance degree. The analytical results reveal that $\text{PF}_e = \text{PF}_A = \text{PF}_{A1}$.

(c) Case 3 considers the effects of harmonic distortion. The analytical results reveal that since $\text{PF}_{A1}$ only considers the fundamental components, the harmonic distortion is disregarded. Therefore, the values are equal to those in Case 1. The analytical results reveal that $\text{PF}_e = \text{PF}_A = \text{PF}_{A1}$. The higher the harmonic distortion is, the less $\text{PF}_A$ and $\text{PF}_{A1}$ are.

Case 4 simultaneously considers the effects of harmonic distortion and unbalance. Some power factor values are given in TABLE 7. The analytical results reveal that $\text{PF}_e = \text{PF}_A = \text{PF}_{A1}$.

TABLE 3 Utilization conditions of FPGA in calculating effective power factor

<table>
<thead>
<tr>
<th>Logic Utilization</th>
<th>Used</th>
<th>Available</th>
<th>Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slice Flip Flops</td>
<td>3646</td>
<td>26624</td>
<td>13%</td>
</tr>
<tr>
<td>LUTs</td>
<td>3640</td>
<td>26624</td>
<td>13%</td>
</tr>
<tr>
<td>Slices</td>
<td>2771</td>
<td>13312</td>
<td>20%</td>
</tr>
<tr>
<td>IOBs</td>
<td>232</td>
<td>487</td>
<td>47%</td>
</tr>
<tr>
<td>MULT18×18</td>
<td>19</td>
<td>32</td>
<td>59%</td>
</tr>
<tr>
<td>Clk</td>
<td>1</td>
<td>8</td>
<td>12%</td>
</tr>
</tbody>
</table>

Global Timing Constraints

| Period     | 13.421(ns) |
| Offset in  | 4.899(ns)  |
| Offset out | 8.896(ns)  |
TABLE 4 Utilization conditions of FPGA in calculating arithmetic power factor

<table>
<thead>
<tr>
<th>Logic Utilization</th>
<th>Used</th>
<th>Available</th>
<th>Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slice Flip Flops</td>
<td>2880</td>
<td>26624</td>
<td>100%</td>
</tr>
<tr>
<td>LUTs</td>
<td>2763</td>
<td>26624</td>
<td>100%</td>
</tr>
<tr>
<td>Slices</td>
<td>2143</td>
<td>13312</td>
<td>166%</td>
</tr>
<tr>
<td>IOBs</td>
<td>203</td>
<td>487</td>
<td>41%</td>
</tr>
<tr>
<td>MULT18×18</td>
<td>15</td>
<td>32</td>
<td>46%</td>
</tr>
<tr>
<td>Clk</td>
<td>1</td>
<td>8</td>
<td>12%</td>
</tr>
</tbody>
</table>

Global Timing Constraints

TABLE 5 Utilization conditions of FPGA in calculating fundamental power

<table>
<thead>
<tr>
<th>Logic Utilization</th>
<th>Used</th>
<th>Available</th>
<th>Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slice Registers</td>
<td>24902</td>
<td>26624</td>
<td>93%</td>
</tr>
<tr>
<td>LUTs</td>
<td>19371</td>
<td>26624</td>
<td>72%</td>
</tr>
<tr>
<td>Slices</td>
<td>13001</td>
<td>13312</td>
<td>97%</td>
</tr>
<tr>
<td>IOBs</td>
<td>203</td>
<td>487</td>
<td>41%</td>
</tr>
<tr>
<td>MULT18×18</td>
<td>18</td>
<td>32</td>
<td>56%</td>
</tr>
<tr>
<td>Clk</td>
<td>1</td>
<td>8</td>
<td>12%</td>
</tr>
</tbody>
</table>

Global Timing Constraints

TABLE 6 Power factor values in Case 1

<table>
<thead>
<tr>
<th></th>
<th>PF_e</th>
<th>PF_A</th>
<th>PF_{A1}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Matlab</td>
<td>0.9496</td>
<td>0.9496</td>
<td>0.9496</td>
</tr>
<tr>
<td>FPGA</td>
<td>0.9504</td>
<td>0.9520</td>
<td>0.9498</td>
</tr>
<tr>
<td>Error(%)</td>
<td>-0.084</td>
<td>-0.253</td>
<td>-0.021</td>
</tr>
</tbody>
</table>

5 Conclusion

The calculation of apparent powers and power factors are implemented in FPGA considering the effects of harmonic and unbalanced conditions. A lot of algorithms are written into IP on FPGA. The calculation results of power factors have the average error about 0.35%. In the FPGA chip utilization rates, the calculation procedures of fundamental power factor are the highest, and the calculation method of arithmetic the lowest. In calculating time of the procedures of the arithmetic factor is the fastest. The results reveal that the FPGA chip can be used to calculate the power factor values accurately.

References:


### TABLE 7 Some power factor values in Case 4

<table>
<thead>
<tr>
<th>$\bar{S}_{1U}$ (%)</th>
<th>$\bar{S}_{eN}$ (%)</th>
<th>$PF_e$</th>
<th>$\varepsilon(%)$</th>
<th>$PF_A$</th>
<th>$\varepsilon(%)$</th>
<th>$PF_{A1}$</th>
<th>$\varepsilon(%)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>100</td>
<td>0.6693</td>
<td>0.6688 - 0.194</td>
<td>0.6693</td>
<td>0.6701 - 0.120</td>
<td>0.9496</td>
<td>0.9498 - 0.021</td>
</tr>
<tr>
<td>10</td>
<td>100</td>
<td>0.6676</td>
<td>0.667 - 0.090</td>
<td>0.6689</td>
<td>0.6694 - 0.075</td>
<td>0.9496</td>
<td>0.9486 0.105</td>
</tr>
<tr>
<td>20</td>
<td>100</td>
<td>0.6626</td>
<td>0.6622 - 0.091</td>
<td>0.6680</td>
<td>0.6696 - 0.240</td>
<td>0.9496</td>
<td>0.9512 - 0.168</td>
</tr>
<tr>
<td>30</td>
<td>100</td>
<td>0.6546</td>
<td>0.654 - 0.092</td>
<td>0.6660</td>
<td>0.6672 - 0.120</td>
<td>0.9496</td>
<td>0.9502 - 0.063</td>
</tr>
<tr>
<td>40</td>
<td>100</td>
<td>0.6439</td>
<td>0.643 - 0.140</td>
<td>0.6643</td>
<td>0.6657 - 0.211</td>
<td>0.9496</td>
<td>0.9484 0.126</td>
</tr>
<tr>
<td>50</td>
<td>100</td>
<td>0.6308</td>
<td>0.630 - 0.127</td>
<td>0.6616</td>
<td>0.6626 - 0.151</td>
<td>0.9496</td>
<td>0.9516 - 0.211</td>
</tr>
<tr>
<td>60</td>
<td>100</td>
<td>0.6158</td>
<td>0.615 - 0.130</td>
<td>0.6584</td>
<td>0.6588 - 0.061</td>
<td>0.9496</td>
<td>0.9499 - 0.032</td>
</tr>
<tr>
<td>70</td>
<td>100</td>
<td>0.5995</td>
<td>0.599 - 0.083</td>
<td>0.6548</td>
<td>0.6561 - 0.199</td>
<td>0.9496</td>
<td>0.9485 0.116</td>
</tr>
<tr>
<td>80</td>
<td>100</td>
<td>0.5821</td>
<td>0.581 - 0.189</td>
<td>0.6506</td>
<td>0.6516 - 0.154</td>
<td>0.9496</td>
<td>0.9514 - 0.190</td>
</tr>
<tr>
<td>90</td>
<td>100</td>
<td>0.5641</td>
<td>0.564 - 0.018</td>
<td>0.6460</td>
<td>0.6475 - 0.232</td>
<td>0.9496</td>
<td>0.9500 - 0.042</td>
</tr>
<tr>
<td>100</td>
<td>100</td>
<td>0.5459</td>
<td>0.545 - 0.165</td>
<td>0.6410</td>
<td>0.6411 - 0.016</td>
<td>0.9496</td>
<td>0.9496 0.000</td>
</tr>
</tbody>
</table>

| Error($) | 0.120 | Error($) | -0.143 | Error($) | -0.098 |

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